CONTROL DATA

60462210

AT478-A/B, AT481-A/B
IOU AND ASSOCIATED EQUIPMENT

BOARD TYPES:

KR KX
JX KZ
JY LX
JZ LZ
KA

L4 DIAGRAMS

VOLUME 2, BOOK 3 OF 3

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (08-20-86)	Preliminary release.
B (11-07-86)	Manual released and revised to include ECO 47746.
C (11-07-86)	Manual revised to include FCO 48197.
D (11-07-86)	Manual revised to include ECO 48326.
E (11-07-86)	Manual revised to include ECO 48400. This edition obsoletes all previous editions. This publication has been divided into two volumes (publication numbers 60462210 and 60463540).
F (06-15-87)	Manual revised to include ECO 48318, changes both versions of JA-01, -02, -06, -11, and -12.
G (06-15-87)	Manual revised to include ECO 48478, changes JK-01, -07, and -20.
H (06-15-87)	Manual revised to include ECO 48479, changes JZ(22113019)-01, -08 through -13, -22, -25, and -28 and deletes JZ(53575518)-01 through -29; ECO 48330, changes JD-01 and -05, JL-01 and -10, JQ-01 and -17, JR(53575515)-01 and -10, JR(22105675)-01, -09, and -10, both versions of JS-01 and -23, JT-01 and -08, JW(53575537)-01 and -17, and JX(53575512)-01 and -05. This edition also adds KX-01 through -21, KZ-01 through -22 LZ-01 through -23, and LX-01 through -13; and changes A-1 and A-2. ECO 48628, changes KZ-01, -02, -18, and -21; and ECO 48633, changes JK-01 and -22.
J (01-15-88)	Manual revised to include ECO 48633, affected diagrams (JK-01 and -22) included in revision H edition.
K (01-15-88)	Manual revised to include FCO 48632, changes both versions of JE/JV-01 and -04 through 07. This edition also includes ECOs 48483 and 48860. ECO 48483 changes JG (53575506) -01 and -09. ECO 48860 changes both versions of JF-01, 14, and 17; JE/JV (22105672) -01, 15, and 17; both versions of JC/JU-01, -19, and -22.
L (01-15-88)	Manual revised to include FCO 48862, changes KX-01, -05, -08, -09, -13, and -15; KZ-01, -16, and -18. This edition also includes ECOs 48855 and 49123. ECO 48855 changes LX-01, -08, -09, -11, and -12; LZ-01 and -21. ECO 49123 changes JQ-01, -03, -11, -12, -13, and -16; JM-01 and -26.
M (08-05-88)	Manual revised to include FCO 49637. Also includes ECOs 49486, 49487, and 49505. Changes pages 4-57, 4-75, 4-85, 4-97, 4-141, 4-153 through 4-157, 4-159, 4-171 through 4-175, 4-199, 4-212, 4-217, and 4-219 in book 1; 4-431, 4-432, 4-473 through 4-502, 4-527, 4-540, 4-555, 4-557, 5-576, 4-595, 4-597, 4-608, and 4-616 in book 2; 4-725, 4-726, 5-755, 4-776, 4-783, 4-804, 4-841, 4-868, 4-927, 4-935, and 4-936 in book 3.
N (08-05-88)	Field Change Order 49705. No change to manual.
P (08-05-88)	Manual revised to include ECO 49723. Changes pages 4-660 in book 2; A-1 and A-2 in book 3. Pages 4-660.1 through 4-660.12 in book 2 are added.

Publication No.
60462210

REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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this manual.

REVISION RECORD

REVISION	DESCRIPTION

Publication No.
60462210

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AT478-A	01	-	Released
	02	47441	
	03	47450	
	04	ECO 47840	
	05	47727	
	06	47740	
	07	47748	
	08	48197	
	09	48326	
	10	48400	
	11	48318	
	12	48478	
	13	48631	
	14	48632	
	15	ECO 48404	
AT478-B	01	-	Released
AT481-A	01	-	Released
	02	ECO 47840	
	03	47748	
	04	48326	
	05	48400	
	06	48318	
	07	ECO 48494	
	08	48632	
	09	ECO 49485	
AT481-B	01	-	Released
AT482-A	01	-	Released
	02	ECO 49485	
	03	ECO 49494	
AT482-B	01	-	Released
AT490-A	01	-	Released
	02	48479	
	03	ECO 49485	
	04	ECO 49484	
AT490-B	01	-	Released
AT497-A	01	-	Released
	02	ECO 49485	
	03	49637	
	04	ECO 49494	
AT497-B	01	-	Released
AT498-A	01	-	Released
	02	48862	
	03	ECO 49485	
	04	ECO 49494	
AT498-B	01	-	Released
AT501-A	01	-	Released
AT501-B	01	-	Released
AT501-C	01	-	Released
AT509-A	01	-	Released
AT510-A	01	-	Released

PREFACE

This manual contains the multi-level diagram set for:

- AT478-A Non-Concurrent Input/Output Unit (NIO)
- AT478-B Non-Concurrent Input/Output Unit (NIO)
- AT481-A 1st Concurrent PP Increment Input/Output Unit (CIO)
- AT481-B 1st Concurrent PP Increment Input/Output Unit (CIO)
- AT482-A 2nd Concurrent PP Increment Input/Output Unit (CIO)
- AT482-B 2nd Concurrent PP Increment Input/Output Unit (CIO)
- AT490-A Intelligent Standard Interface (ISI) Channel Adapter
- AT490-B Intelligent Standard Interface (ISI) Channel Adapter
- AT497-A Intelligent Peripheral Interface (IPI) Channel Adapter
- AT497-B Intelligent Peripheral Interface (IPI) Channel Adapter
- AT498-A Direct Memory Access (DMA) Enhanced C170 Channel Adapter
- AT498-B Direct Memory Access (DMA) Enhanced C170 Channel Adapter
- AT501-A CYBER 990 Secondary I4 Conversion Kit
- AT501-B CYBER 840/850/860 Secondary I4 Conversion Kit
- AT501-C CYBER 992 Secondary I4 Conversion Kit
- AT509-A I4 to PIP3 CM Interface
- AT510-A I4 to 8XX/990 CM Interface

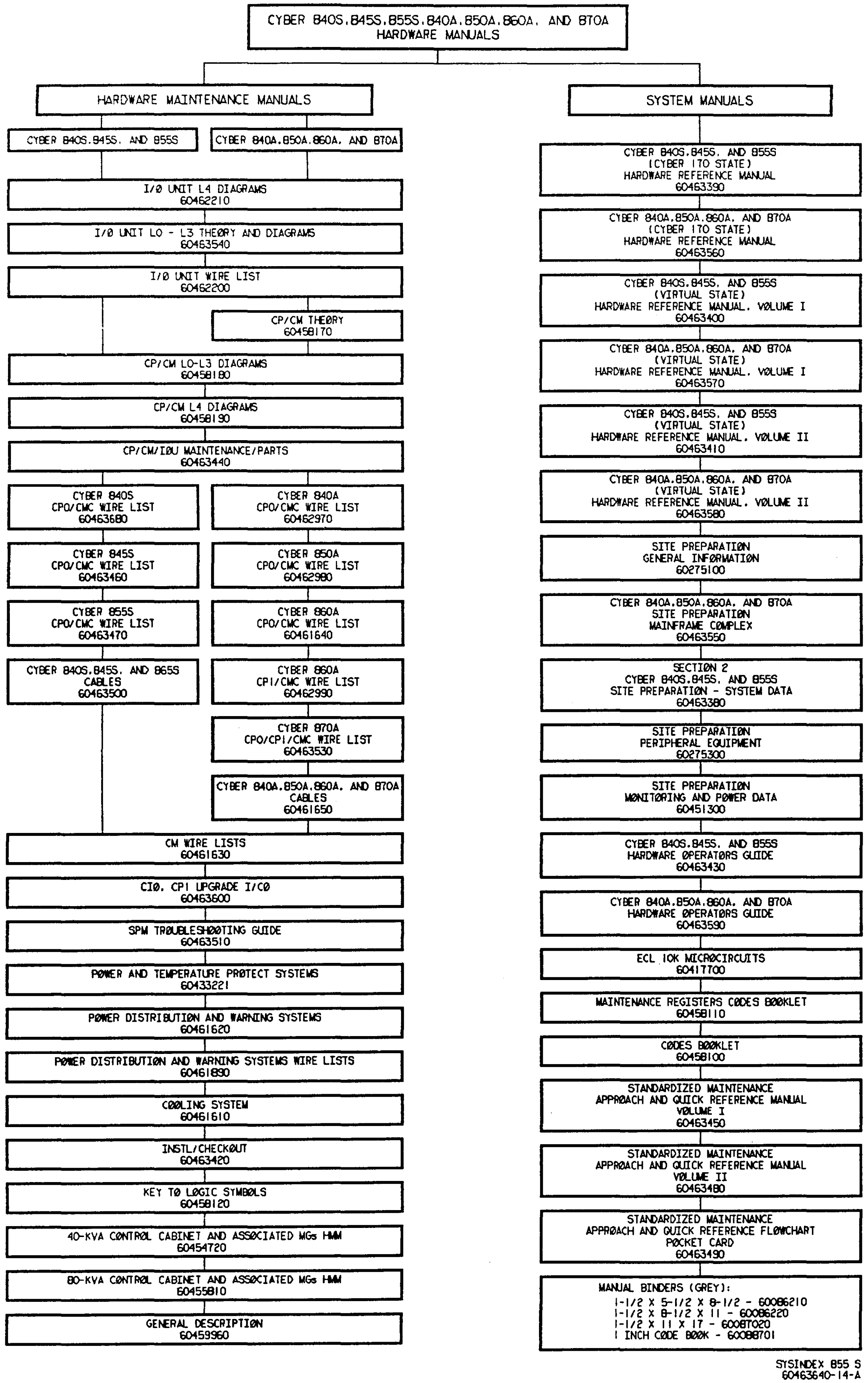
Level 4 diagrams consist of logic diagrams for each board in panels A through D. Where a board is used in more than one location, the signal names (both English names and the six-character identifiers used in the wire list) shown on the level 4 diagram apply to the first occurrence of that board only. The first occurrence is the location that is listed first on the board's level 4 diagram cover sheet. Most pins on multi-occurrence boards have a parallel function that can be determined by referring to the wire list and to level 2 diagrams.

CAUTION

Some boards have two layouts, both of which are used and supported. The two layouts for each of these boards are included in this manual. It is important to check the board number in your unit and compare it to the board master (B/M) number on the appropriate level 4 diagram to be sure they match.

The System Publication Indexes on the following page include other manuals that are applicable to the equipment.

SYSTEM PUBLICATION INDEX


CYBER 840S,845S,855S,840A,850A,860A, AND 870A HARDWARE MANUALS
HARDWARE MAINTENANCE MANUALS
CYBER 840S,845S, AND 855S
CYBER 840A,850A,860A, AND 870A
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CYBER 840S,845S, AND 865S CABLES 60463500
CYBER 860A CPI/CMC WIRE LIST 60462990
CYBER 870A CPO/CPI/CMC WIRE LIST 60463530
CYBER 840A,850A,860A, AND 870A CABLES 60461650
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CIO, CPI UPGRADE I/CO 60463600
SPM TROUBLESHOOTING GUIDE 60463510
POWER AND TEMPERATURE PROTECT SYSTEMS 60433221
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POWER DISTRIBUTION AND WARNING SYSTEMS WIRE LISTS 60461890
COOLING SYSTEM 60461610
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80-KVA CONTROL CABINET AND ASSOCIATED MGs HMM 60455810
GENERAL DESCRIPTION 60459960
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SITE PREPARATION MONITORING AND POWER DATA 60451300
CYBER 840S,845S, AND 855S HARDWARE OPERATORS GUIDE 60463430
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ECL 10K MICROCIRCUITS 60417700
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CODES BOOKLET 60458100
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE MANUAL VOLUME I 60463450
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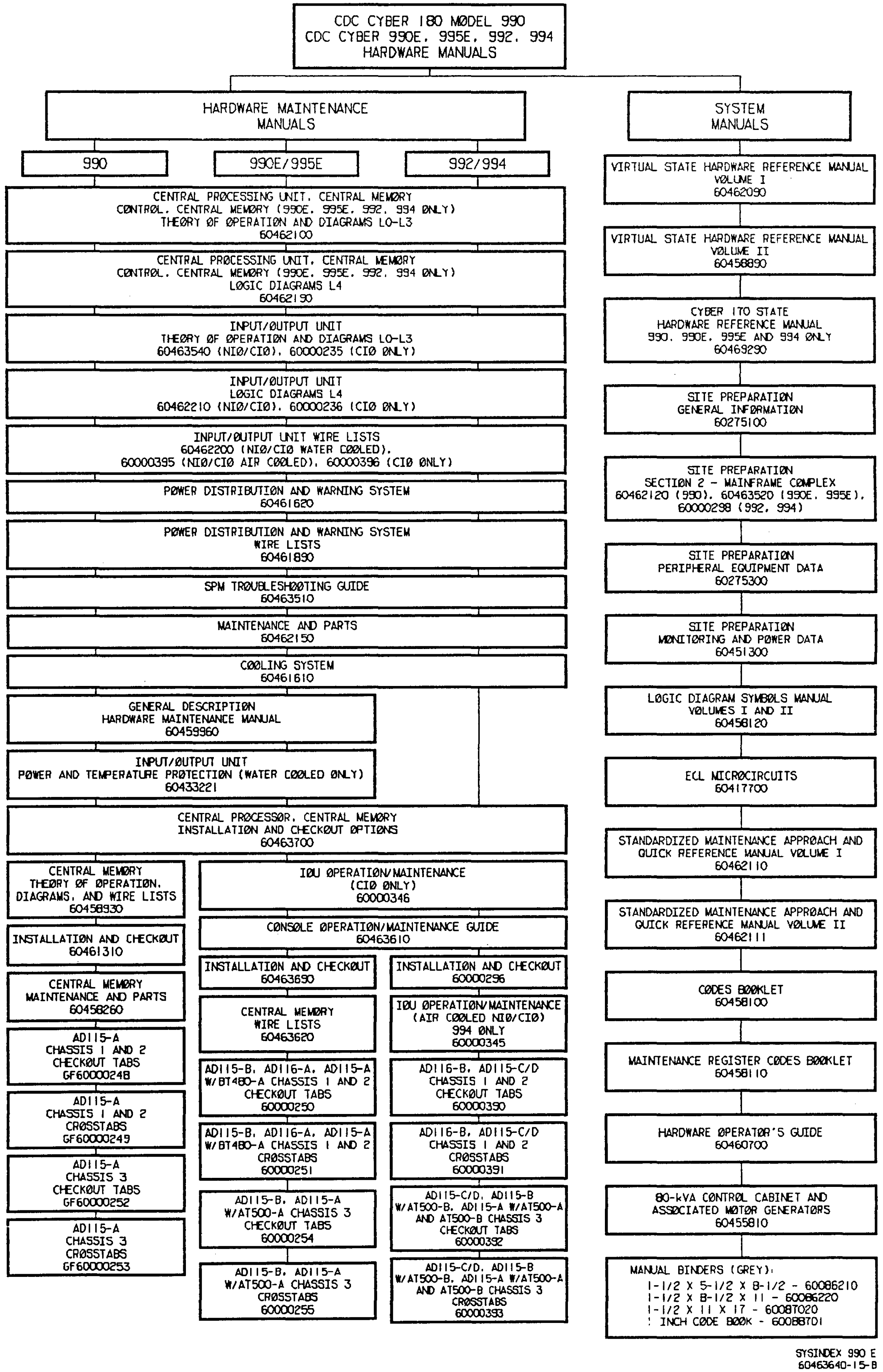
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE FLOWCHART POCKET CARD 60463490
MANUAL BINDERS (GREY):
1-1/2 X 5-1/2 X 8-1/2 - 60086210
1-1/2 X 8-1/2 X 11 - 60086220
1-1/2 X 11 X 17 - 6008T020
1 INCH CODE BOOK - 60088701
SYSINDEX 855 S
60463640-14-A

SYSTEM PUBLICATION INDEX


CDC CYBER 180 MODEL 990 CDC CYBER 990E, 995E, 992, 994 HARDWARE MANUALS
HARDWARE MAINTENANCE MANUALS
990
990E/995E
992/994
CENTRAL PROCESSING UNIT, CENTRAL MEMORY CONTROL, CENTRAL MEMORY (990E, 995E, 992, 994 ONLY) THEORY OF OPERATION AND DIAGRAMS LO-L3 60462100
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VIRTUAL STATE HARDWARE REFERENCE MANUAL VOLUME II 60458890
CYBER 170 STATE HARDWARE REFERENCE MANUAL 990, 990E, 995E AND 994 ONLY 60469290
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SITE PREPARATION SECTION 2 - MAINFRAME COMPLEX 60462120 (990), 60463520 (990E, 995E), 60000298 (992, 994)
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80-kVA CONTROL CABINET AND ASSOCIATED MOTOR GENERATORS 60455810
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1-1/2 X 8-1/2 X 11 - 60086220
1-1/2 X 11 X 17 - 6008T020
1 INCH CODE BOOK - 600887D1
SYSINDEX 990 E
60463640-15-B

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2. LEVEL 2 DIAGRAMS 2-1
3A. LEVEL 3 DIAGRAMS 3A-1
3B. 170 DMA LEVELS 0-3 3B-1
3C. IPI LEVELS 0-3 3C-1

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A ABBREVIATIONS A-1

VOLUME 2

4. LEVEL 4 DIAGRAMS①

BOOK 1

Panel A

JA† 53575500. 4-1
JA† 22105670. 4-15
JC/JU 53575502. 4-29
JC/JU 22105671. 4-57
JD 4-85
JE/JV 53575504. 4-101
JE/JV 22105672. 4-121
JF 53575505. 4-141
JF 22105620. 4-159
JG 53575506. 4-177
JG 22105673. 4-199
JH 53575507. 4-221
JH 22105679. 4-251
JJ 53575508. 4-281
JJ 22105674. 4-305

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① Two sets of logic diagrams are provided for a board that has two layouts. The appropriate logic diagram set has a board master (B/M) number that matches the printed wiring board (PWB) number of the board.

†Also in panel C.

BOOK 2

Panel A

JQ 4-329
JR 53575515. 4-351
JR 22105675. 4-363
JS† 53575516. 4-375
JS† 22130333. 4-403
JT† 4-431
HR 4-660.1

Panel B

CQ 4-447
HK/JK 4-473
JL 4-503
JM 4-527
JW†† 53575537. 4-555
JW 22105621. 4-595
KB†† 4-635
KR (Diagrams are located in book 3)

BOOK 3

Panels C and D

KR††† 4-661
JX 53575512. 4-695
JX 22105623. 4-725
JY 53575513. 4-755
JY 22105622. 4-783
JZ 4-841
KA 22127690. 4-871
KA 22105610. 4-877
KX 4-883
KZ 4-905
LX 4-927
LZ 4-941

APPENDIX

A PANEL MAPS A-1

---

†Also in panel D.
††Also in panels C and D.
†††Also in panel B

1KRH RGTR BOARD

REVISION HISTORY B/M 41653131			
DATE	REV	DESCRIPTION OF CHANGE	INIT
11/01/85	A	CLASS A RELEASE OF LOGIC DIAGRAMS WITH ECO #46886 INSTALLED.	DRF
01/30/86	B	ECO #47441 INSTALLED, PG.33 .	LHJ
07/07/86	C	ECO #47746 ADDS B/M NO. TO SHT 1.	LHJ
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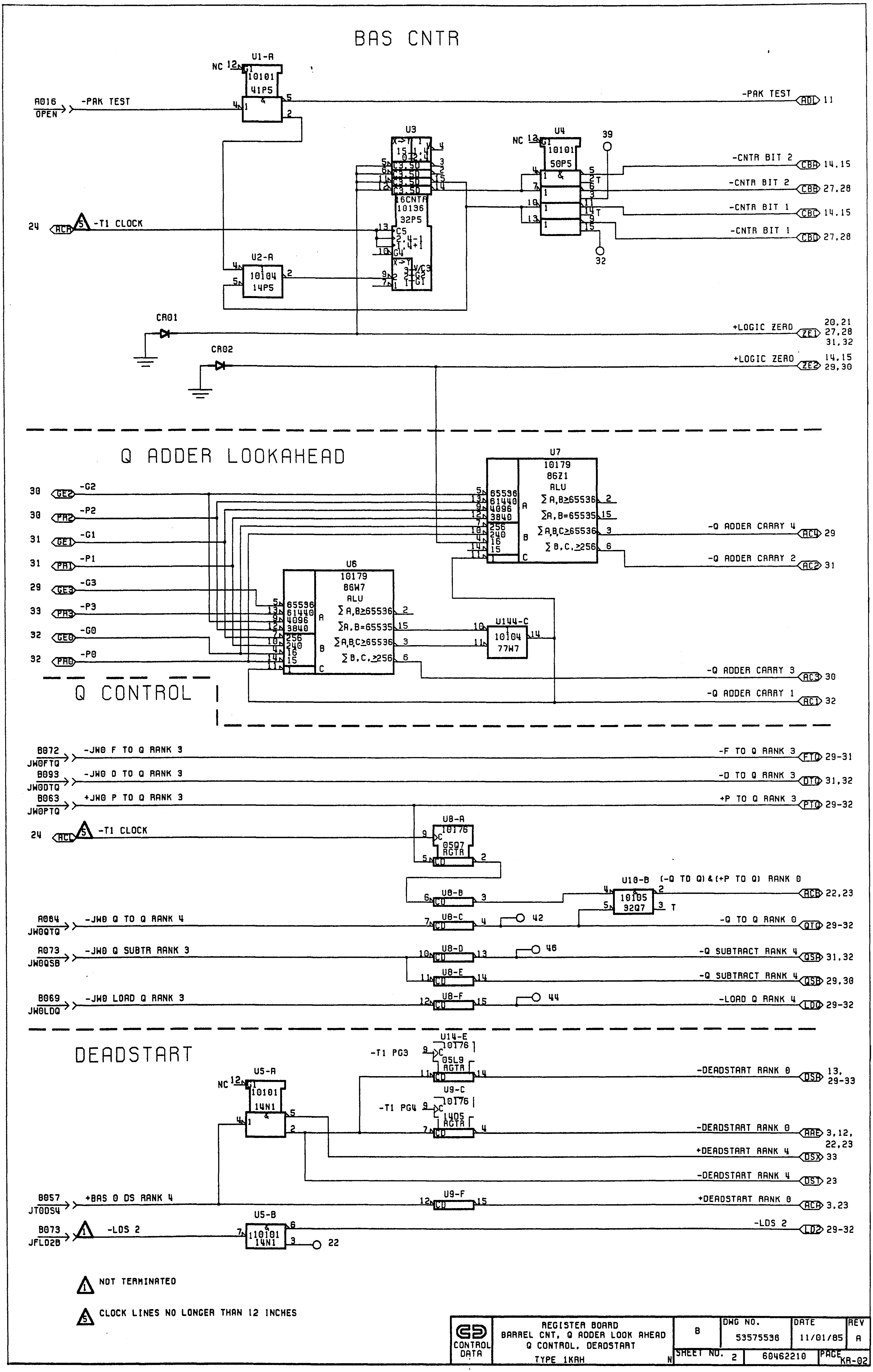
DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	D R FORD	12/04/85
PUBS	R K BONDE	12/04/85
APP	D R FORD	12/04/85

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: B15,B13,B11,B09,D25,C25

CONTROL DATA	REVISION HISTORY TYPE 1KRH	B	DWG NO. 53575536	DATE 07/07/86	REV C
		N	SHEET NO. 1	60462210	PAGE KR-01

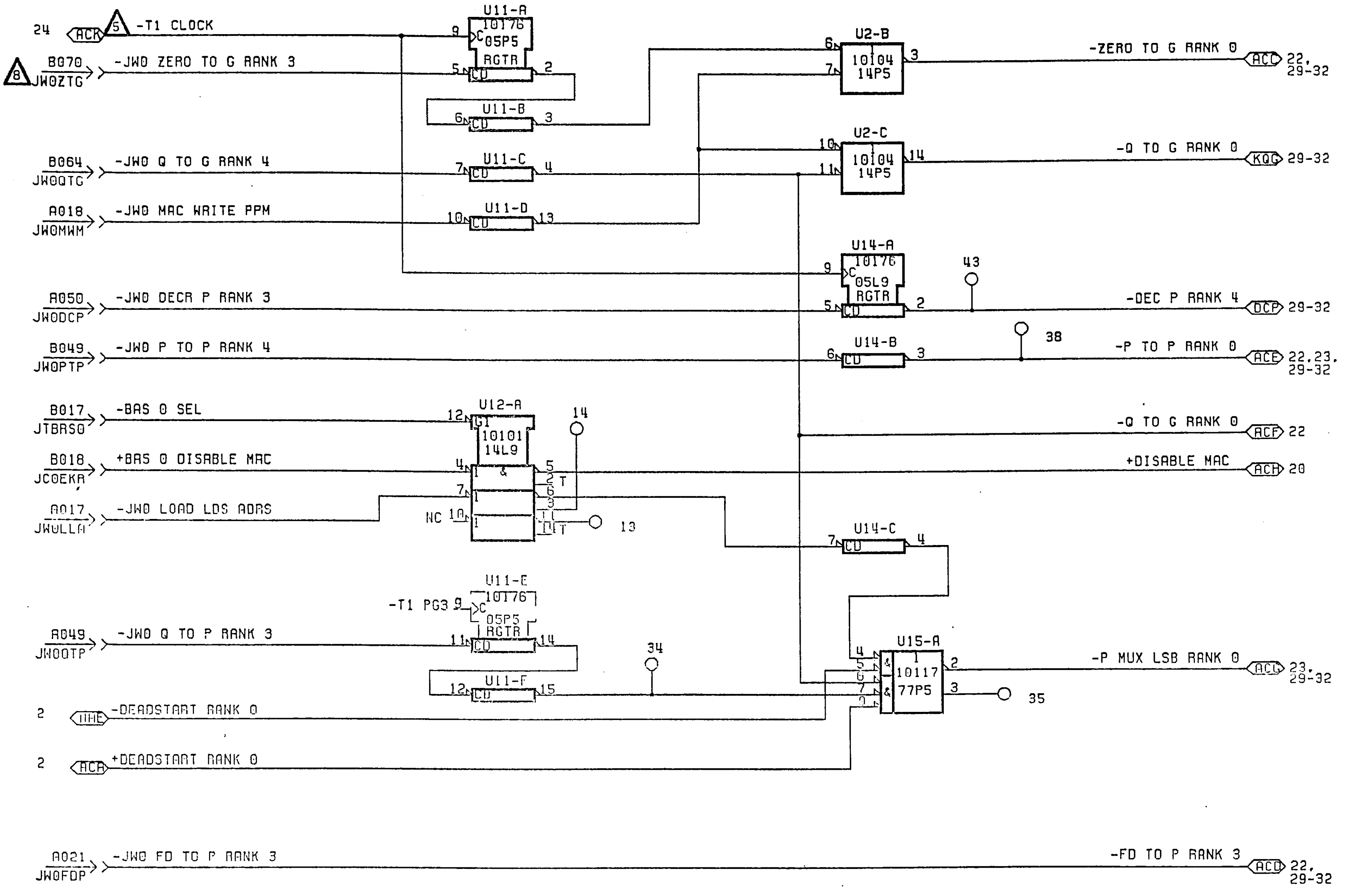


1 NOT TERMINATED

5 CLOCK LINES NO LONGER THAN 12 INCHES

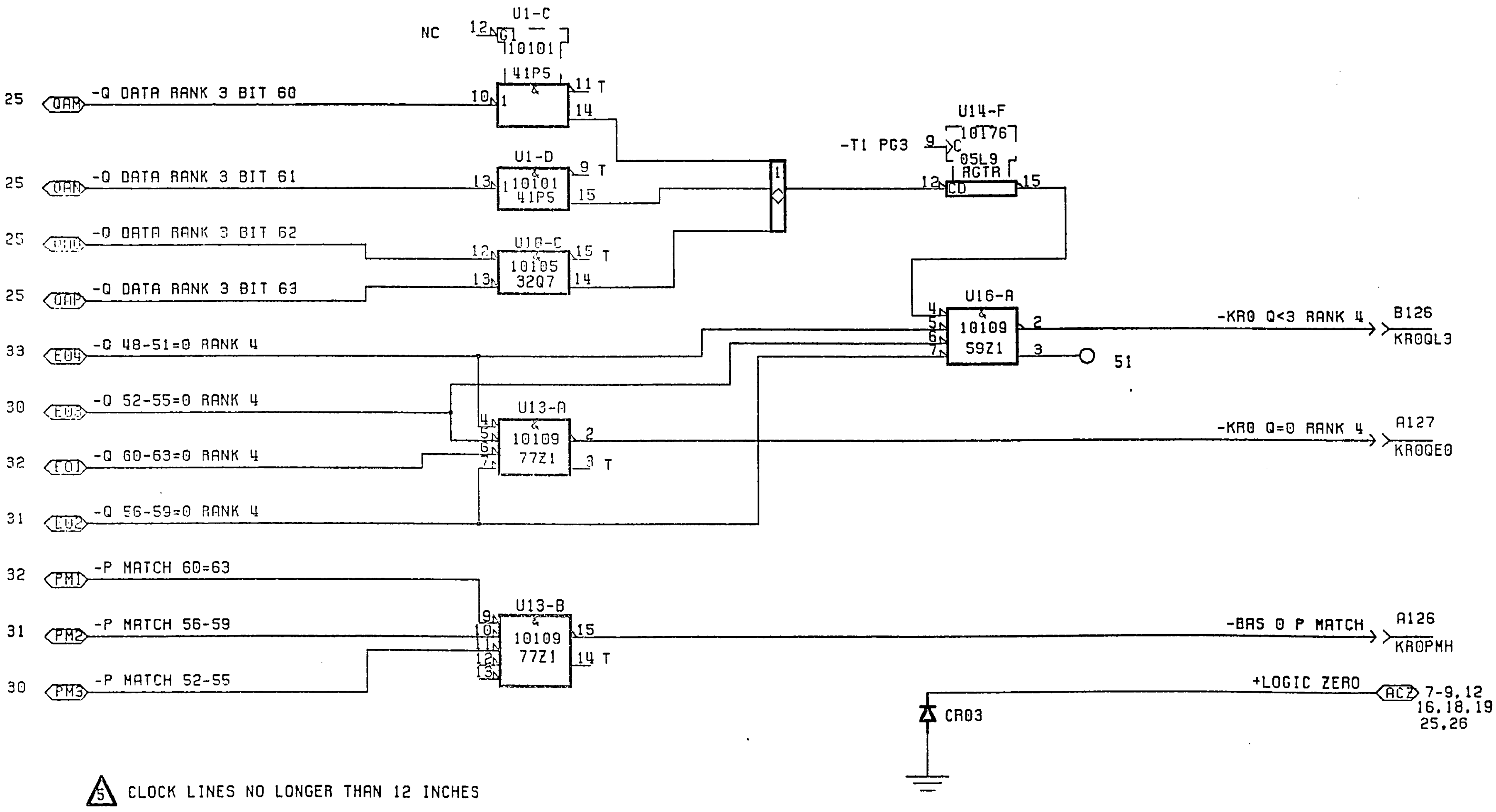
CONTROL DATA	REGISTER BOARD BARREL CNT, Q ADDER LOOK AHEAD Q CONTROL, DEADSTART TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 2	60462210	PAGE KA-02	

P MUX LSB



24 ACR -T1 CLOCK
B070 JW0ZTG -JW0 ZERO TO G RANK 3
B064 JW0QTG -JW0 Q TO G RANK 4
A018 JW0MWM -JW0 MAC WRITE PPM
A050 JW0DCP -JW0 DECR P RANK 3
B049 JW0PTP -JW0 P TO P RANK 4
B017 JTBRS0 -BAS 0 SEL
B018 JCOEKA +BAS 0 DISABLE MAC
A017 JW0LLA -JW0 LOAD LDS ADRS
A049 JW0QTP -JW0 Q TO P RANK 3
2 ANE -DEADSTART RANK 0
2 ACR +DEADSTART RANK 0
A021 JW0FDP -JW0 FD TO P RANK 3
U11-A 10176 05P5 RGTR
U11-B
U11-C
U11-D
U11-E 10176 05P5 RGTR
U11-F
-T1 PG3
U2-B 10104 14P5
U2-C 10104 14P5
U14-A 10176 05L9 RGTR
U14-B
U14-C
U12-A 10101 14L9
NC
U15-A 10117 77P5
43
38
14
13
34
35
-ZERO TO G RANK 0 ACC 22, 29-32
-Q TO G RANK 0 KQG 29-32
-DEC P RANK 4 DCP 29-32
-P TO P RANK 0 ACE 22,23, 29-32
-Q TO G RANK 0 ACF 22
+DISABLE MAC ACH 20
-P MUX LSB RANK 0 ACL 23, 29-32
-FD TO P RANK 3 ACD 22, 29-32

Q=0, P MATCH

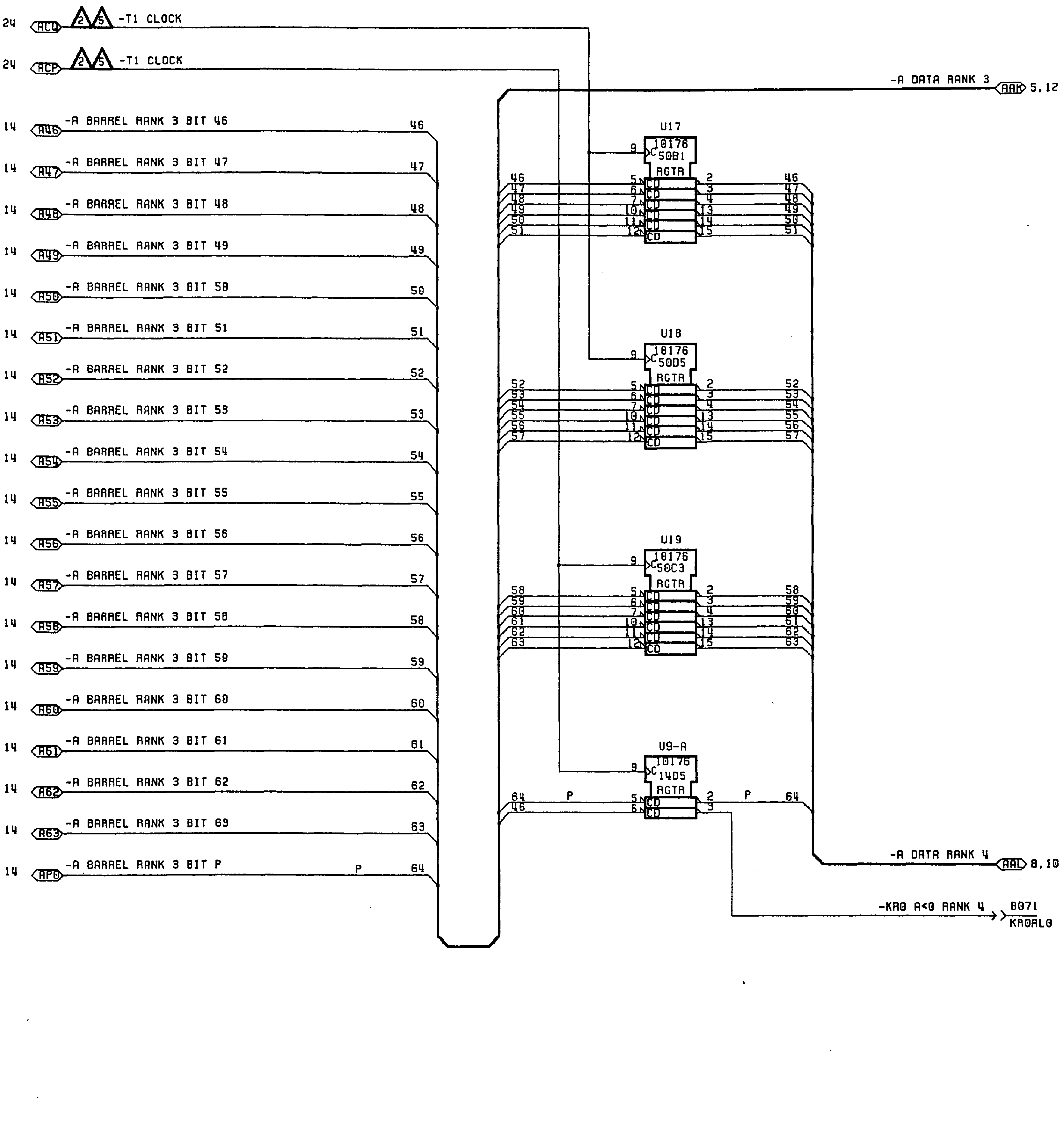


⚠5 CLOCK LINES NO LONGER THAN 12 INCHES

⚠8 MAKE SURE THIS PIN IS
NO LONGER CONNECTED
AS A +5 VOLT SOURCE

CONTROL DATA	REGISTER BOARD P MUX LSB Q=0, P MATCH TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
			SHEET NO. 3	60462210	PAGE KR-03

A RGTR RANK 4

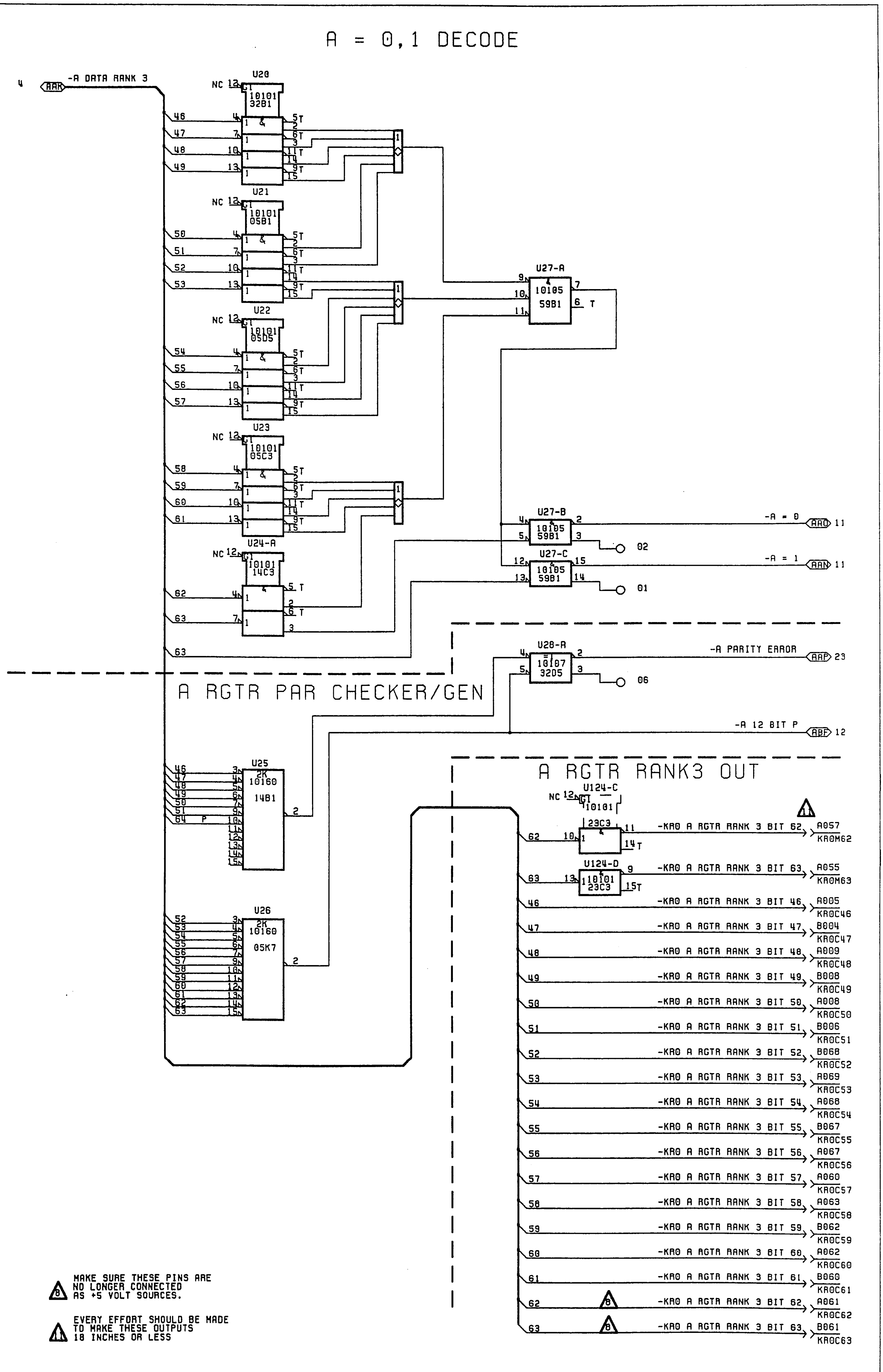


24 ACQ 2 5 -T1 CLOCK
24 ACP 2 5 -T1 CLOCK
-A DATA RANK 3 AAK 5,12
14 A46 -A BARREL RANK 3 BIT 46
14 A47 -A BARREL RANK 3 BIT 47
14 A48 -A BARREL RANK 3 BIT 48
14 A49 -A BARREL RANK 3 BIT 49
14 A50 -A BARREL RANK 3 BIT 50
14 A51 -A BARREL RANK 3 BIT 51
14 A52 -A BARREL RANK 3 BIT 52
14 A53 -A BARREL RANK 3 BIT 53
14 A54 -A BARREL RANK 3 BIT 54
14 A55 -A BARREL RANK 3 BIT 55
14 A56 -A BARREL RANK 3 BIT 56
14 A57 -A BARREL RANK 3 BIT 57
14 A58 -A BARREL RANK 3 BIT 58
14 A59 -A BARREL RANK 3 BIT 59
14 A60 -A BARREL RANK 3 BIT 60
14 A61 -A BARREL RANK 3 BIT 61
14 A62 -A BARREL RANK 3 BIT 62
14 A63 -A BARREL RANK 3 BIT 63
14 AP0 -A BARREL RANK 3 BIT P
P
U17 10176 50B1 RGTR
U18 10176 50D5 RGTR
U19 10176 50C3 RGTR
U9-A 10176 14D5 RGTR
C
CD
9
5 6 7 10 11 12
2 3 4 13 14 15
46 47 48 49 50 51
52 53 54 55 56 57
58 59 60 61 62 63
64 P
-A DATA RANK 4 AAL 8,10
-KA0 A<0 RANK 4 B071 KA0AL0

△2 ROUTE CLOCK TO THESE CHIP LOCATIONS LAST

△5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD A REGISER RANK 4 TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 4	60462210	PAGE KA-04	

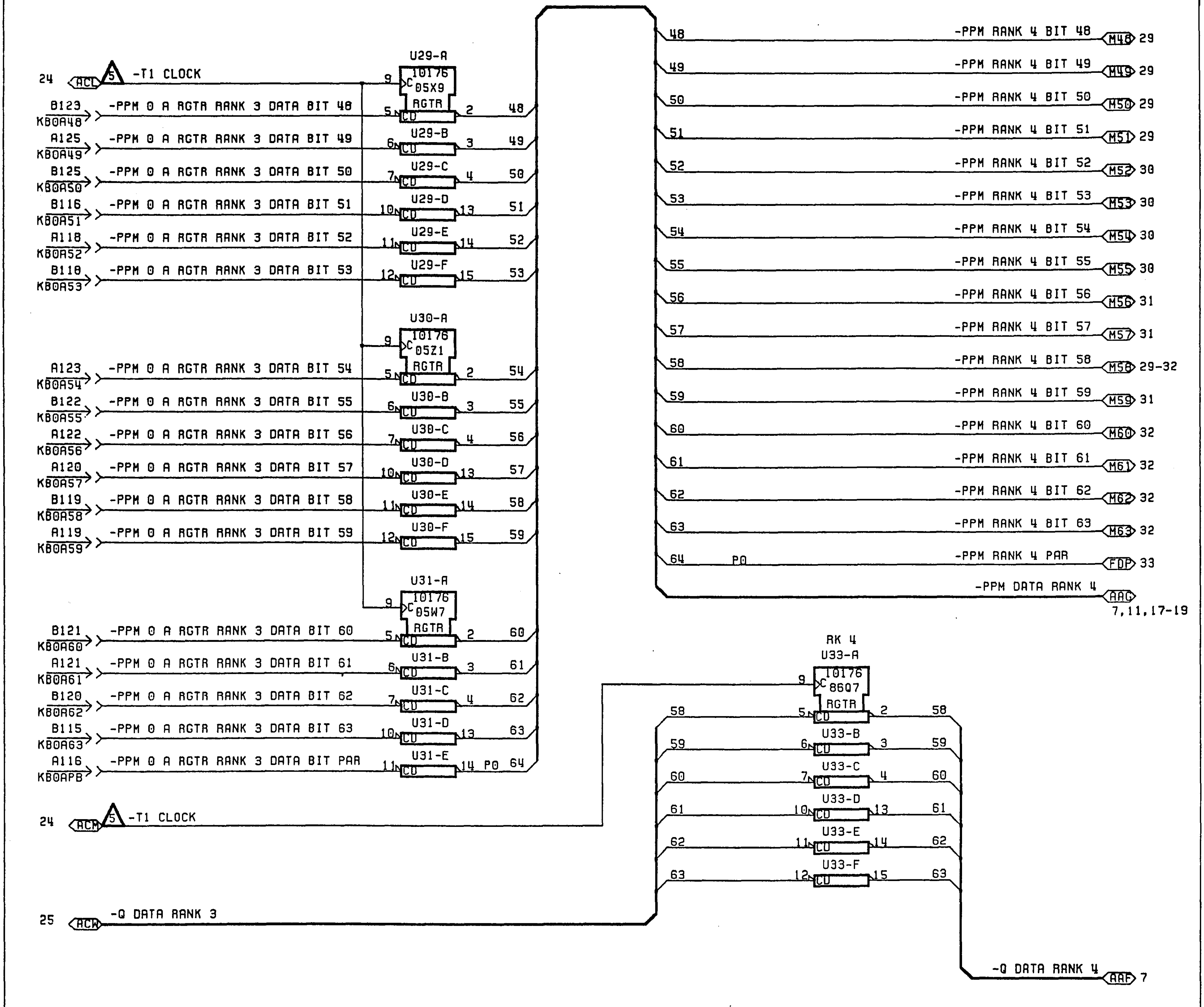

A = 0,1 DECODE
4 AAH -A DATA RANK 3
U20 10101 32B1
U21 10101 05B1
U22 10101 05D5
U23 10101 05C3
U24-A 10101 14C3
NC 12 G1
46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
U27-A 10105 59B1
U27-B 10105 59B1
U27-C 10105 59B1
-A = 0 AA0 11
-A = 1 AA1 11
02
01
U28-A 10107 32D5
-A PARITY ERROR AAP 23
06
-A 12 BIT P ABP 12
A RGTR PAR CHECKER/GEN
U25 2K 10160 14B1
64 P
U26 2K 10160 05K7
A RGTR RANK3 OUT
U124-C 10101 23C3
U124-D 10101 23C3
-KA0 A RGTR RANK 3 BIT 62 A057 KA0M62
-KA0 A RGTR RANK 3 BIT 63 A055 KA0M63
-KA0 A RGTR RANK 3 BIT 46 A005 KA0C46
-KA0 A RGTR RANK 3 BIT 47 B004 KA0C47
-KA0 A RGTR RANK 3 BIT 48 A009 KA0C48
-KA0 A RGTR RANK 3 BIT 49 B008 KA0C49
-KA0 A RGTR RANK 3 BIT 50 A008 KA0C50
-KA0 A RGTR RANK 3 BIT 51 B006 KA0C51
-KA0 A RGTR RANK 3 BIT 52 B068 KA0C52
-KA0 A RGTR RANK 3 BIT 53 A069 KA0C53
-KA0 A RGTR RANK 3 BIT 54 A068 KA0C54
-KA0 A RGTR RANK 3 BIT 55 B067 KA0C55
-KA0 A RGTR RANK 3 BIT 56 A067 KA0C56
-KA0 A RGTR RANK 3 BIT 57 A060 KA0C57
-KA0 A RGTR RANK 3 BIT 58 A063 KA0C58
-KA0 A RGTR RANK 3 BIT 59 B062 KA0C59
-KA0 A RGTR RANK 3 BIT 60 A062 KA0C60
-KA0 A RGTR RANK 3 BIT 61 B060 KA0C61
-KA0 A RGTR RANK 3 BIT 62 A061 KA0C62
-KA0 A RGTR RANK 3 BIT 63 B061 KA0C63
8
11

8 MAKE SURE THESE PINS ARE NO LONGER CONNECTED AS +5 VOLT SOURCES.

11 EVERY EFFORT SHOULD BE MADE TO MAKE THESE OUTPUTS 18 INCHES OR LESS

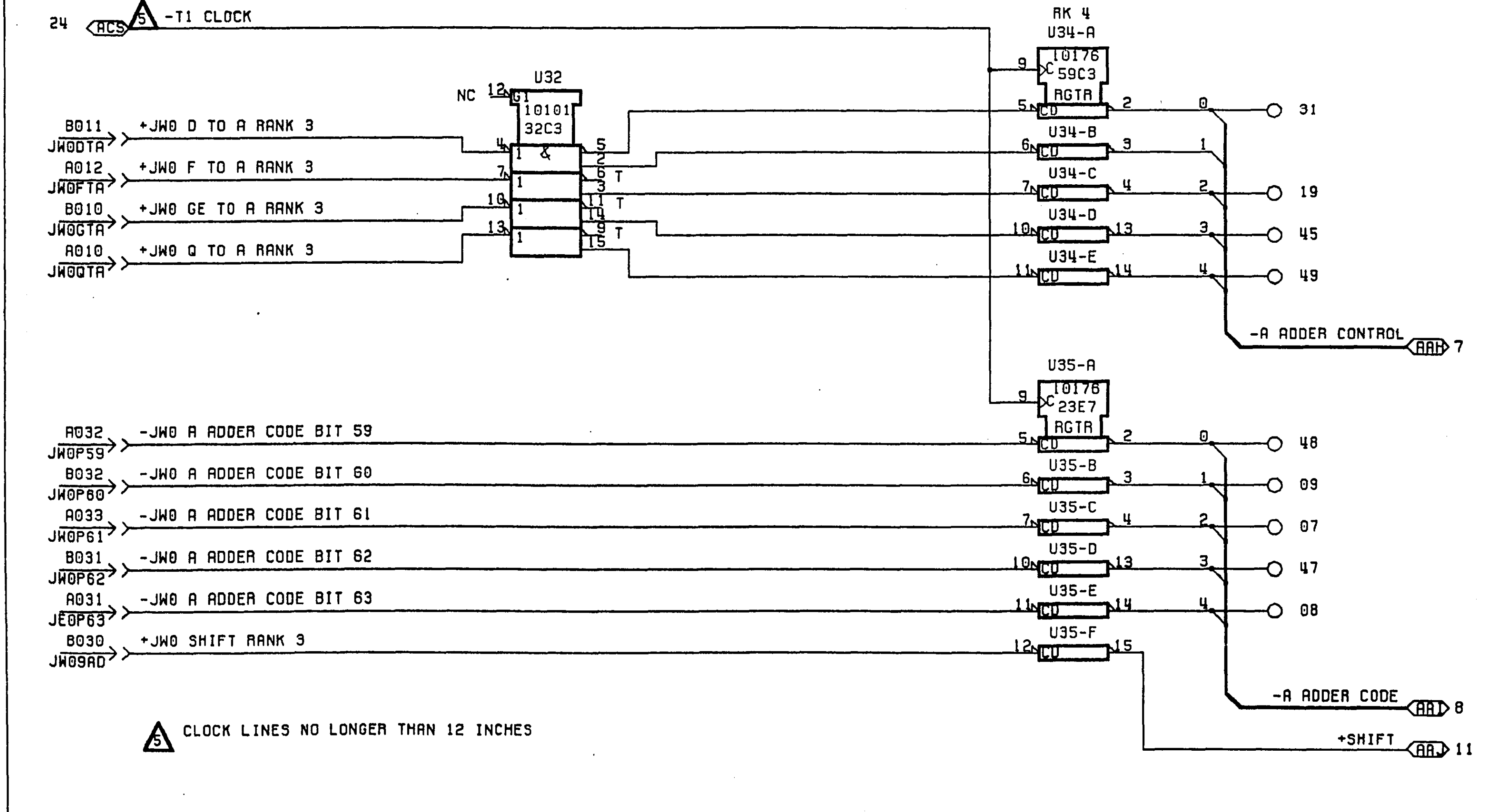
CONTROL DATA	REGISTER BOARD A REGISTER PARITY CHECK/GEN A=0,1 DECODE, A REG RANK 3 OUTPU TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 5	60462210	PAGE KA-05	

A ADDER B OPERAND INPUT DATA RGTR



24 ACL 5 -T1 CLOCK
U29-A 10176 05X9 RGTR
B123 KB0A48 -PPM 0 A RGTR RANK 3 DATA BIT 48
A125 KB0A49 -PPM 0 A RGTR RANK 3 DATA BIT 49
B125 KB0A50 -PPM 0 A RGTR RANK 3 DATA BIT 50
B116 KB0A51 -PPM 0 A RGTR RANK 3 DATA BIT 51
A118 KB0A52 -PPM 0 A RGTR RANK 3 DATA BIT 52
B118 KB0A53 -PPM 0 A RGTR RANK 3 DATA BIT 53
U29-B U29-C U29-D U29-E U29-F
U30-A 10176 05Z1 RGTR
A123 KB0A54 -PPM 0 A RGTR RANK 3 DATA BIT 54
B122 KB0A55 -PPM 0 A RGTR RANK 3 DATA BIT 55
A122 KB0A56 -PPM 0 A RGTR RANK 3 DATA BIT 56
A120 KB0A57 -PPM 0 A RGTR RANK 3 DATA BIT 57
B119 KB0A58 -PPM 0 A RGTR RANK 3 DATA BIT 58
A119 KB0A59 -PPM 0 A RGTR RANK 3 DATA BIT 59
U30-B U30-C U30-D U30-E U30-F
U31-A 10176 05W7 RGTR
B121 KB0A60 -PPM 0 A RGTR RANK 3 DATA BIT 60
A121 KB0A61 -PPM 0 A RGTR RANK 3 DATA BIT 61
B120 KB0A62 -PPM 0 A RGTR RANK 3 DATA BIT 62
B115 KB0A63 -PPM 0 A RGTR RANK 3 DATA BIT 63
A116 KB0APB -PPM 0 A RGTR RANK 3 DATA BIT PAR
U31-B U31-C U31-D U31-E
14 P0 64
-PPM RANK 4 BIT 48 M48 29
-PPM RANK 4 BIT 49 M49 29
-PPM RANK 4 BIT 50 M50 29
-PPM RANK 4 BIT 51 M51 29
-PPM RANK 4 BIT 52 M52 30
-PPM RANK 4 BIT 53 M53 30
-PPM RANK 4 BIT 54 M54 30
-PPM RANK 4 BIT 55 M55 30
-PPM RANK 4 BIT 56 M56 31
-PPM RANK 4 BIT 57 M57 31
-PPM RANK 4 BIT 58 M58 29-32
-PPM RANK 4 BIT 59 M59 31
-PPM RANK 4 BIT 60 M60 32
-PPM RANK 4 BIT 61 M61 32
-PPM RANK 4 BIT 62 M62 32
-PPM RANK 4 BIT 63 M63 32
64 P0 -PPM RANK 4 PAR FDP 33
-PPM DATA RANK 4 AAG 7,11,17-19
RK 4 U33-A 10176 86Q7 RGTR
U33-B U33-C U33-D U33-E U33-F
58 59 60 61 62 63
24 ACM 5 -T1 CLOCK
25 ACW -Q DATA RANK 3
-Q DATA RANK 4 AAF 7

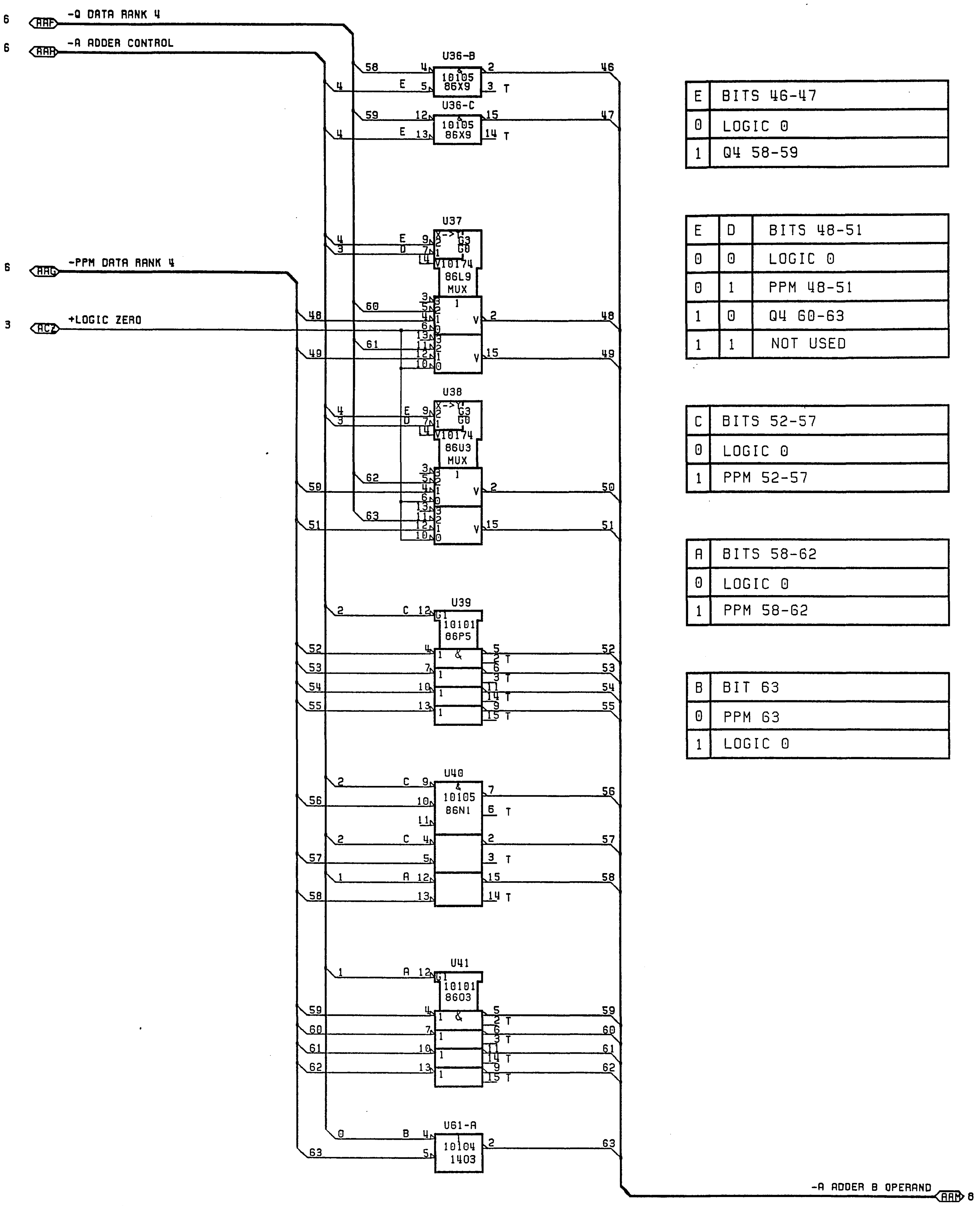
A ADDER CONTROL



24 ACS 5 -T1 CLOCK
RK 4 U34-A 10176 59C3 RGTR
NC 12 U32 G1 10101 32C3
1 &
T T T
B011 JW0DTA +JW0 D TO A RANK 3
A012 JW0FTA +JW0 F TO A RANK 3
B010 JW0GTA +JW0 GE TO A RANK 3
A010 JW0QTA +JW0 Q TO A RANK 3
U34-B U34-C U34-D U34-E
0 31
1
2 19
3 45
4 49
-A ADDER CONTROL AAH 7
U35-A 10176 23E7 RGTR
A032 JW0P59 -JW0 A ADDER CODE BIT 59
B032 JW0P60 -JW0 A ADDER CODE BIT 60
A033 JW0P61 -JW0 A ADDER CODE BIT 61
B031 JW0P62 -JW0 A ADDER CODE BIT 62
A031 JE0P63 -JW0 A ADDER CODE BIT 63
B030 JW09AD +JW0 SHIFT RANK 3
U35-B U35-C U35-D U35-E U35-F
0 48
1 09
2 07
3 47
4 08
-A ADDER CODE AAI 8
+SHIFT AAJ 11
5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD A ADDER B OPERAND INPUT DATA A ADDER CONTROL TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		N	SHEET NO. 6	60462210	PAGE KA-08

A ADDER B OPERAND MUX.



E	BITS 46-47
0	LOGIC 0
1	Q4 58-59

E	D	BITS 48-51
0	0	LOGIC 0
0	1	PPM 48-51
1	0	Q4 60-63
1	1	NOT USED

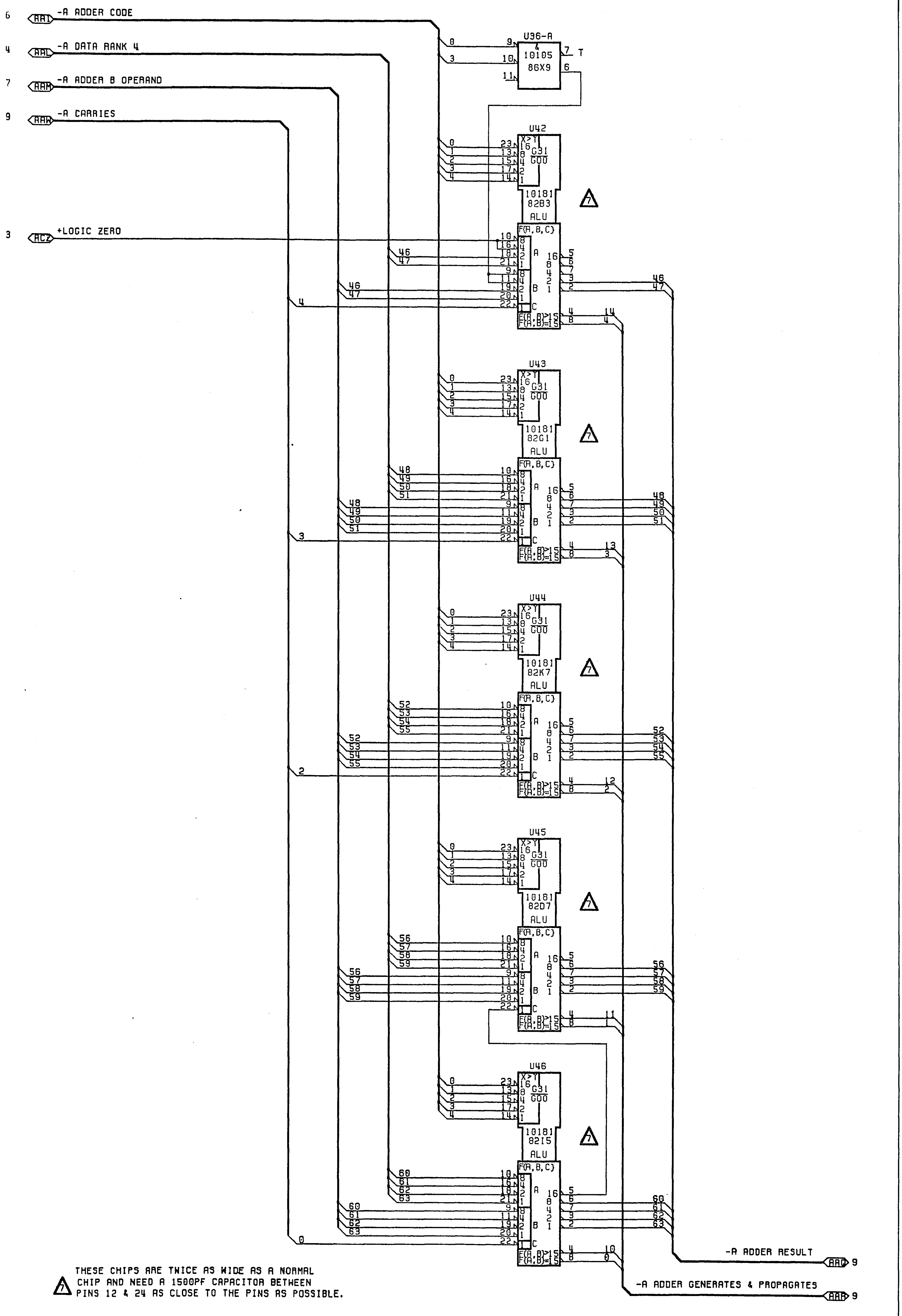
C	BITS 52-57
0	LOGIC 0
1	PPM 52-57

A	BITS 58-62
0	LOGIC 0
1	PPM 58-62

B	BIT 63
0	PPM 63
1	LOGIC 0

CONTROL DATA	REGISTER BOARD A ADDER B OPERAND MUX TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 7	60462210	PAGE KA-07	

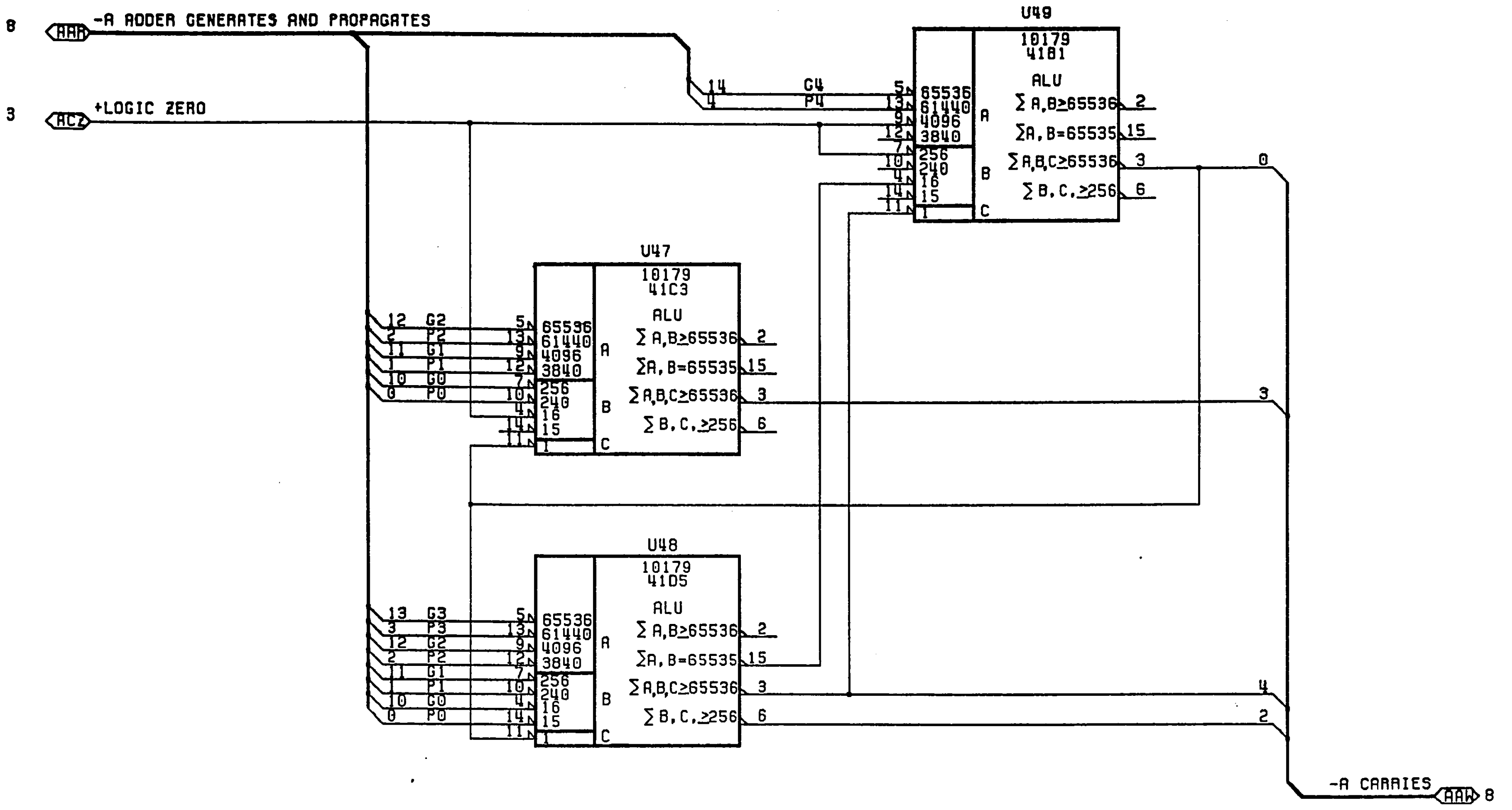
A ADDER



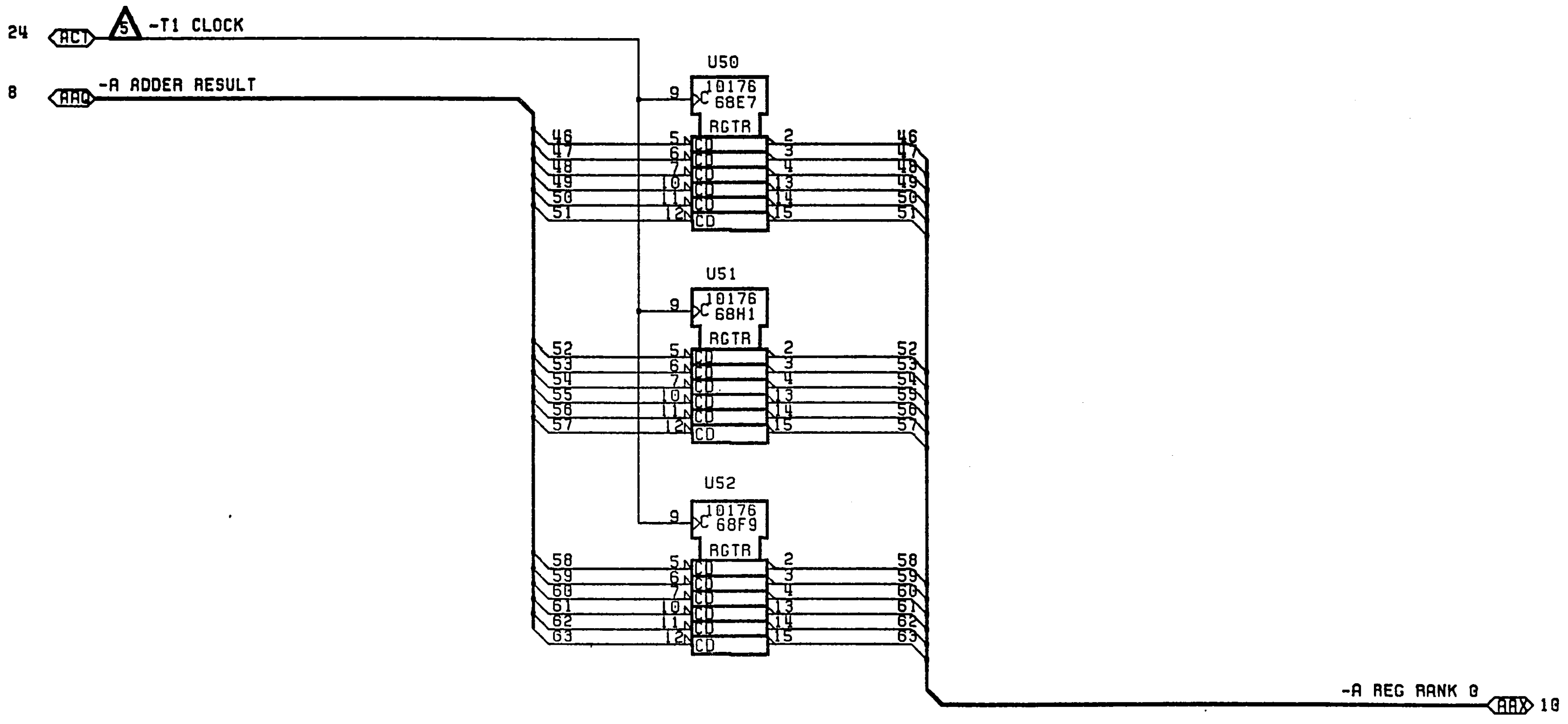
7 THESE CHIPS ARE TWICE AS WIDE AS A NORMAL CHIP AND NEED A 1500PF CAPACITOR BETWEEN PINS 12 & 24 AS CLOSE TO THE PINS AS POSSIBLE.

CONTROL DATA	REGISTER BOARD A ADDER TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
			SHEET NO. 8	60462210	PAGE KA-08

A ADDER LOOKAHEAD

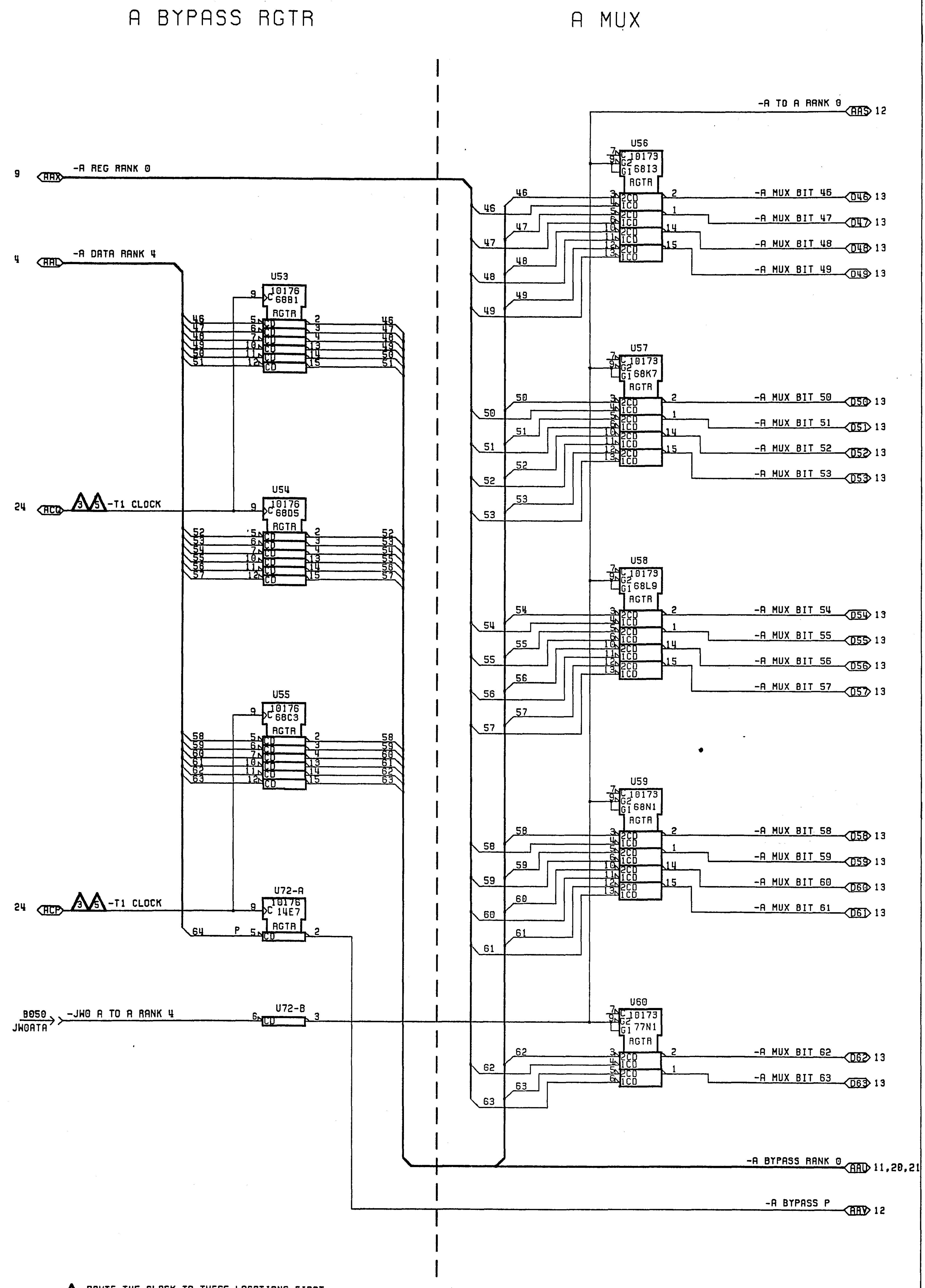


A ADDER OUTPUT RGTR



5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD A ADDER LOOK AHEAD A ADDER OUTPUT REGISTER TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 9	60462210	PAGE KR-09	

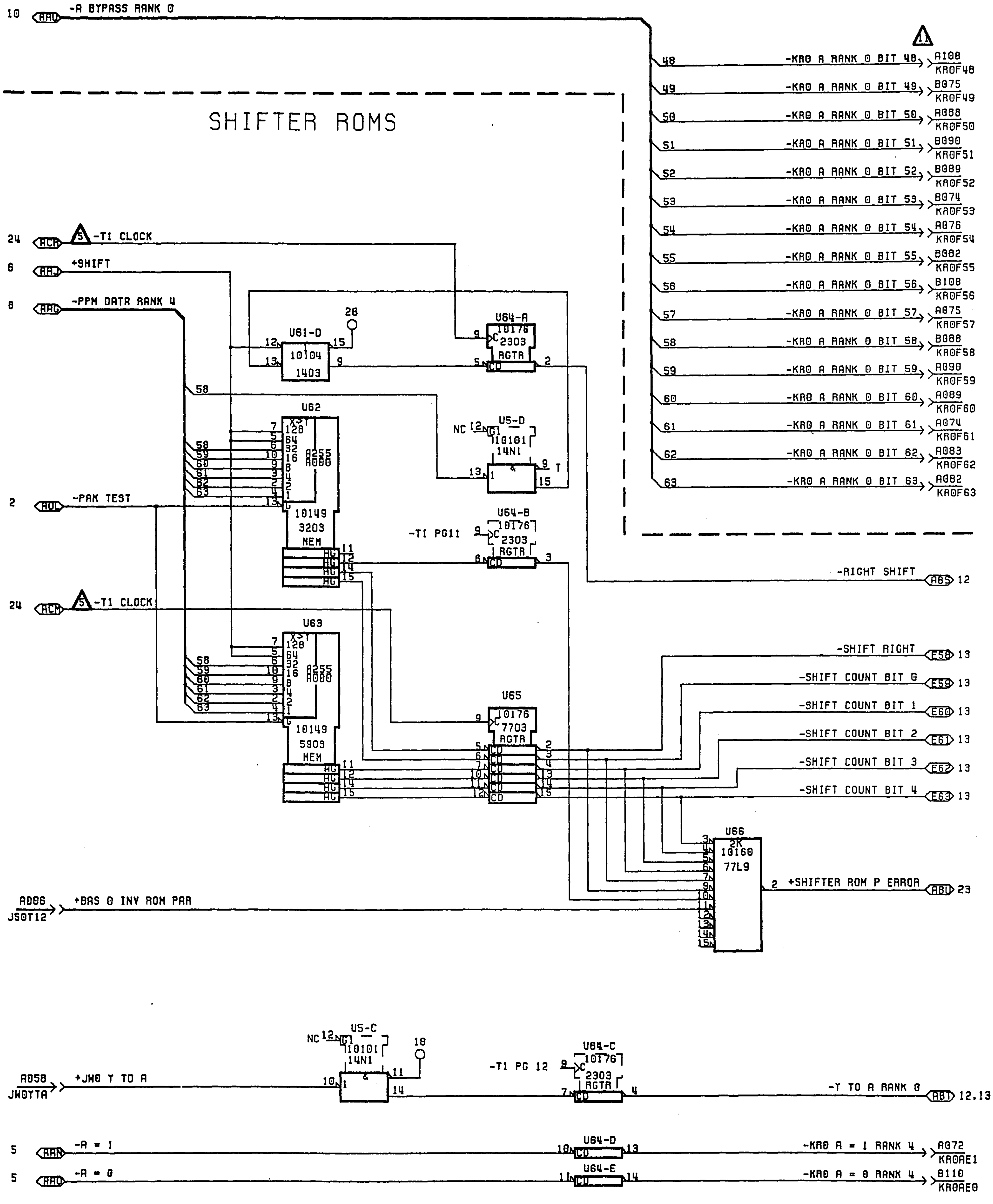


3 ROUTE THE CLOCK TO THESE LOCATIONS FIRST

5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD A BYPASS REGISTER AND A MUX TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		N	SHEET NO. 18	60462210	PAGE KA-18

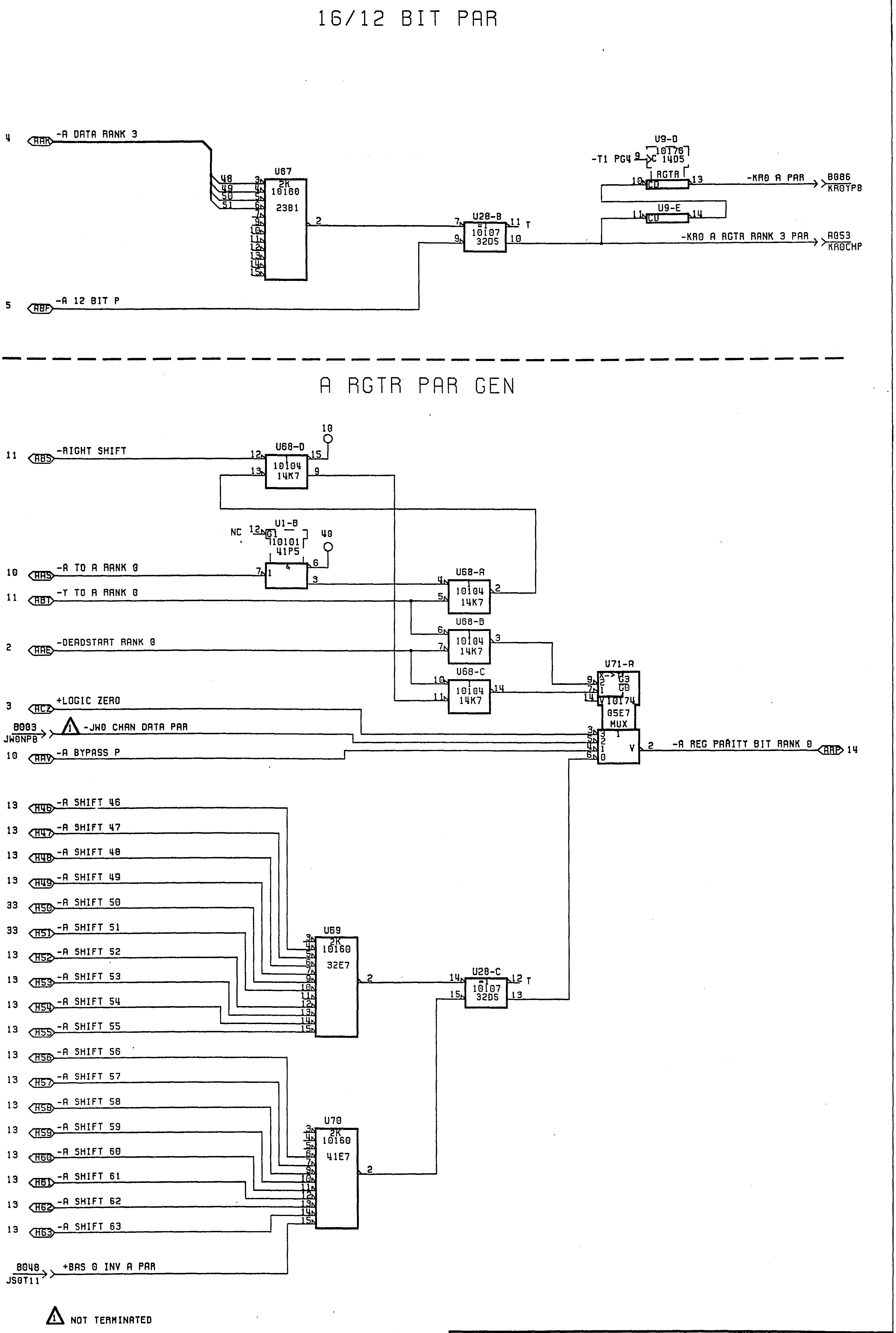
A RANK 0 OUTPUT


SHIFTER ROMS
10 AAU -A BYPASS RANK 0
48 -KR0 A RANK 0 BIT 48 A108 KR0F48
49 -KR0 A RANK 0 BIT 49 B075 KR0F49
50 -KR0 A RANK 0 BIT 50 A088 KR0F50
51 -KR0 A RANK 0 BIT 51 B090 KR0F51
52 -KR0 A RANK 0 BIT 52 B089 KR0F52
53 -KR0 A RANK 0 BIT 53 B074 KR0F53
54 -KR0 A RANK 0 BIT 54 A076 KR0F54
55 -KR0 A RANK 0 BIT 55 B082 KR0F55
56 -KR0 A RANK 0 BIT 56 B108 KR0F56
57 -KR0 A RANK 0 BIT 57 A075 KR0F57
58 -KR0 A RANK 0 BIT 58 B088 KR0F58
59 -KR0 A RANK 0 BIT 59 A090 KR0F59
60 -KR0 A RANK 0 BIT 60 A089 KR0F60
61 -KR0 A RANK 0 BIT 61 A074 KR0F61
62 -KR0 A RANK 0 BIT 62 A083 KR0F62
63 -KR0 A RANK 0 BIT 63 A082 KR0F63
1
24 ACA 5 -T1 CLOCK
6 AAJ +SHIFT
8 AAG -PPM DATA RANK 4
26
U61-D 10104 1403
U64-A 10176 2303 AGTA
U62 A255 A000 10149 3203 MEM
128 64 32 16 8 4 2 1
58 59 60 61 62 63
NC U5-D 10101 14N1
T
2 ADL -PAR TEST
-T1 PG11
U64-B 10176 2303 AGTA
-RIGHT SHIFT AB5 12
24 ACA 5 -T1 CLOCK
U63 A255 A000 10149 5903 MEM
U65 10176 7703 AGTA
-SHIFT RIGHT E58 13
-SHIFT COUNT BIT 0 E59 13
-SHIFT COUNT BIT 1 E60 13
-SHIFT COUNT BIT 2 E61 13
-SHIFT COUNT BIT 3 E62 13
-SHIFT COUNT BIT 4 E63 13
U66 2K 10160 77L9
+SHIFTER ROM P ERROR ABL 23
A006 JS0T12 +BAS 0 INV ROM PAR
NC U5-C 10101 14N1
18
A058 JW0YTA +JW0 Y TO A
-T1 PG 12
U64-C 10176 2303 AGTA
-Y TO A RANK 0 AB1 12.13
5 AAN -A = 1
U64-D
-KR0 A = 1 RANK 4 A072 KR0AE1
5 AAQ -A = 0
U64-E
-KR0 A = 0 RANK 4 B110 KR0AE0

5 CLOCK LINES NO LONGER THAN 12 INCHES

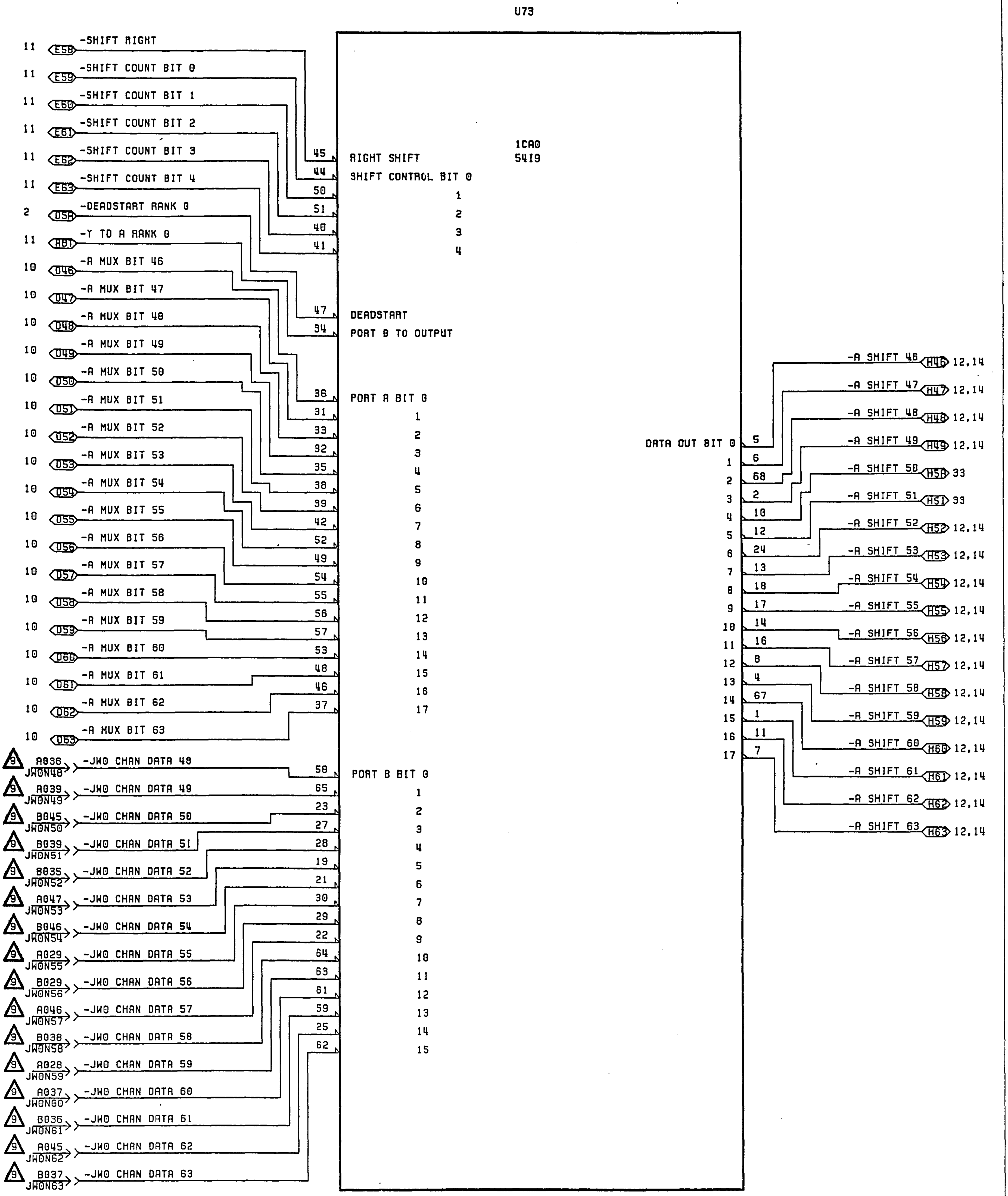
1 EVERY EFFORT SHOULD BE MADE TO MAKE THESE OUTPUTS 18 INCHES OR LESS

CONTROL DATA	REGISTER BOARD A RANK 0 OUTPUT SHIFTER ROMS TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 11	60462210	PAGE KR-11	



CONTROL DATA	REGISTER BOARD A REGISTER PARITY 16/12 BIT PARITY TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 12	60462210	PAGE KA-12	

SHIFTER Y TO A MUX



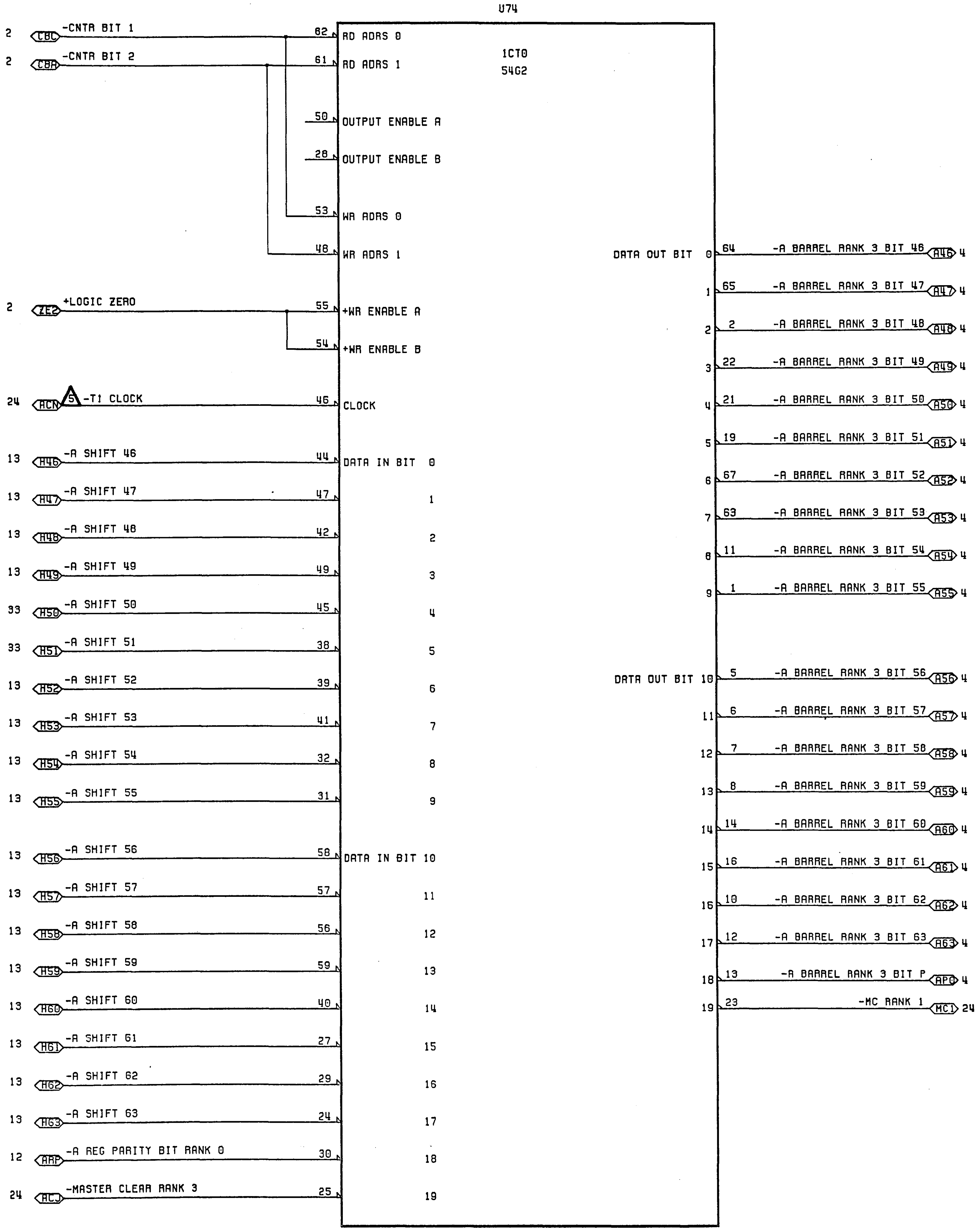
9 NOT TERMINATED AND 18 INCHES OR LESS

CONTROL DATA

REGISTER BOARD
SHIFTER Y TO A MUX
TYPE 1KRH

B	DWG NO.	DATE	REV
	53575536	11/01/85	A
SHEET NO. 13	60462210	PAGE KR-13	

A BARREL RANKS 1-3 BITS 46-63, PAR


U74
1CT0
54G2
2 CBC -CNTR BIT 1 62 RD ADRS 0
2 CBA -CNTR BIT 2 61 RD ADRS 1
50 OUTPUT ENABLE A
28 OUTPUT ENABLE B
53 WR ADRS 0
48 WR ADRS 1
2 ZE2 +LOGIC ZERO 55 +WR ENABLE A
54 +WR ENABLE B
24 ACN 5 -T1 CLOCK 46 CLOCK
13 H46 -A SHIFT 46 44 DATA IN BIT 0
13 H47 -A SHIFT 47 47 1
13 H48 -A SHIFT 48 42 2
13 H49 -A SHIFT 49 49 3
33 H50 -A SHIFT 50 45 4
33 H51 -A SHIFT 51 38 5
13 H52 -A SHIFT 52 39 6
13 H53 -A SHIFT 53 41 7
13 H54 -A SHIFT 54 32 8
13 H55 -A SHIFT 55 31 9
13 H56 -A SHIFT 56 58 DATA IN BIT 10
13 H57 -A SHIFT 57 57 11
13 H58 -A SHIFT 58 56 12
13 H59 -A SHIFT 59 59 13
13 H60 -A SHIFT 60 40 14
13 H61 -A SHIFT 61 27 15
13 H62 -A SHIFT 62 29 16
13 H63 -A SHIFT 63 24 17
12 ARP -A REG PARITY BIT RANK 0 30 18
24 ACJ -MASTER CLEAR RANK 3 25 19
DATA OUT BIT 0 64 -A BARREL RANK 3 BIT 46 A46 4
1 65 -A BARREL RANK 3 BIT 47 A47 4
2 2 -A BARREL RANK 3 BIT 48 A48 4
3 22 -A BARREL RANK 3 BIT 49 A49 4
4 21 -A BARREL RANK 3 BIT 50 A50 4
5 19 -A BARREL RANK 3 BIT 51 A51 4
6 67 -A BARREL RANK 3 BIT 52 A52 4
7 63 -A BARREL RANK 3 BIT 53 A53 4
8 11 -A BARREL RANK 3 BIT 54 A54 4
9 1 -A BARREL RANK 3 BIT 55 A55 4
DATA OUT BIT 10 5 -A BARREL RANK 3 BIT 56 A56 4
11 6 -A BARREL RANK 3 BIT 57 A57 4
12 7 -A BARREL RANK 3 BIT 58 A58 4
13 8 -A BARREL RANK 3 BIT 59 A59 4
14 14 -A BARREL RANK 3 BIT 60 A60 4
15 16 -A BARREL RANK 3 BIT 61 A61 4
16 10 -A BARREL RANK 3 BIT 62 A62 4
17 12 -A BARREL RANK 3 BIT 63 A63 4
18 13 -A BARREL RANK 3 BIT P APO 4
19 23 -MC RANK 1 MC1 24

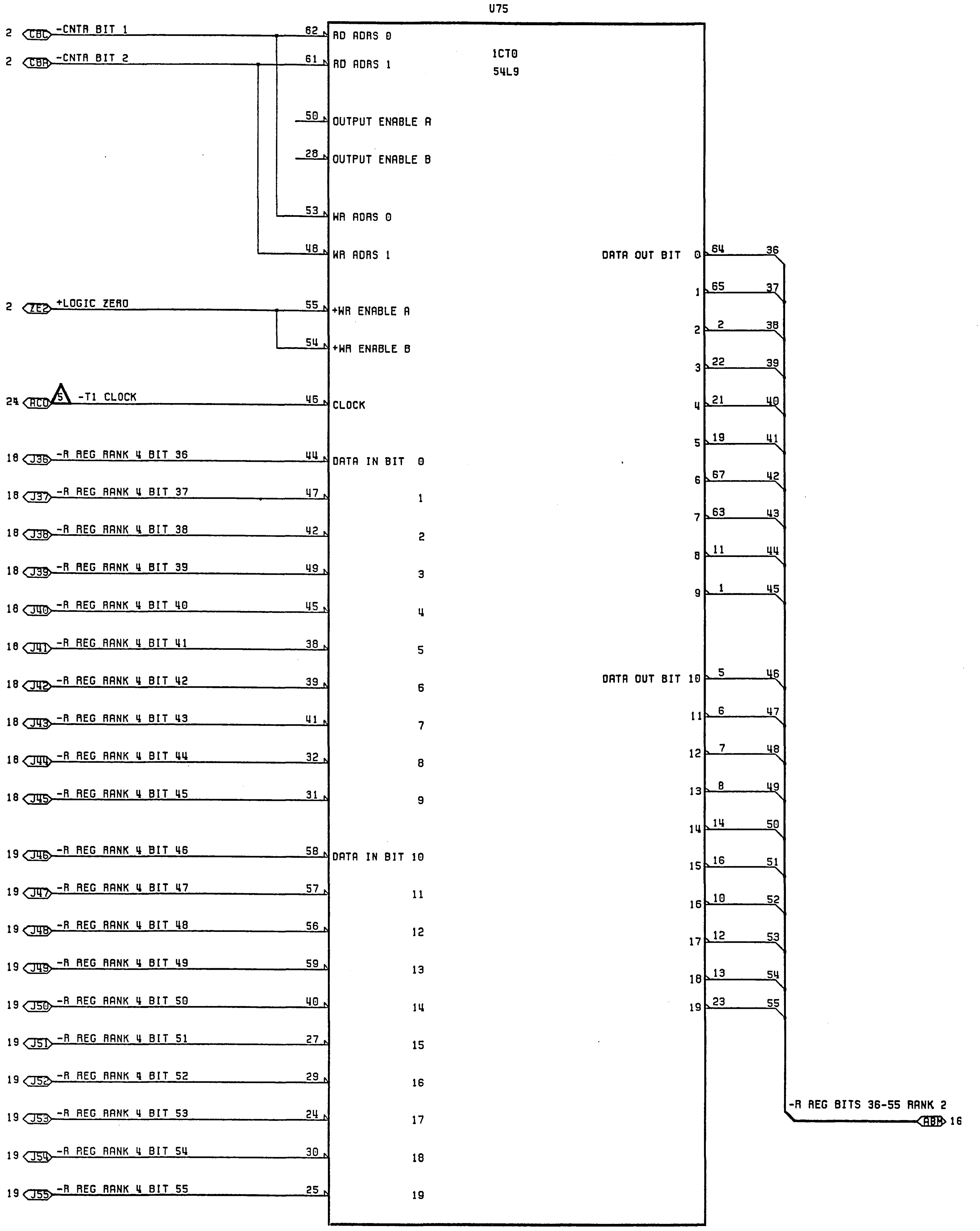
5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA

REGISTER BOARD
A BARREL BITS 46-63, P
TYPE 1KRH

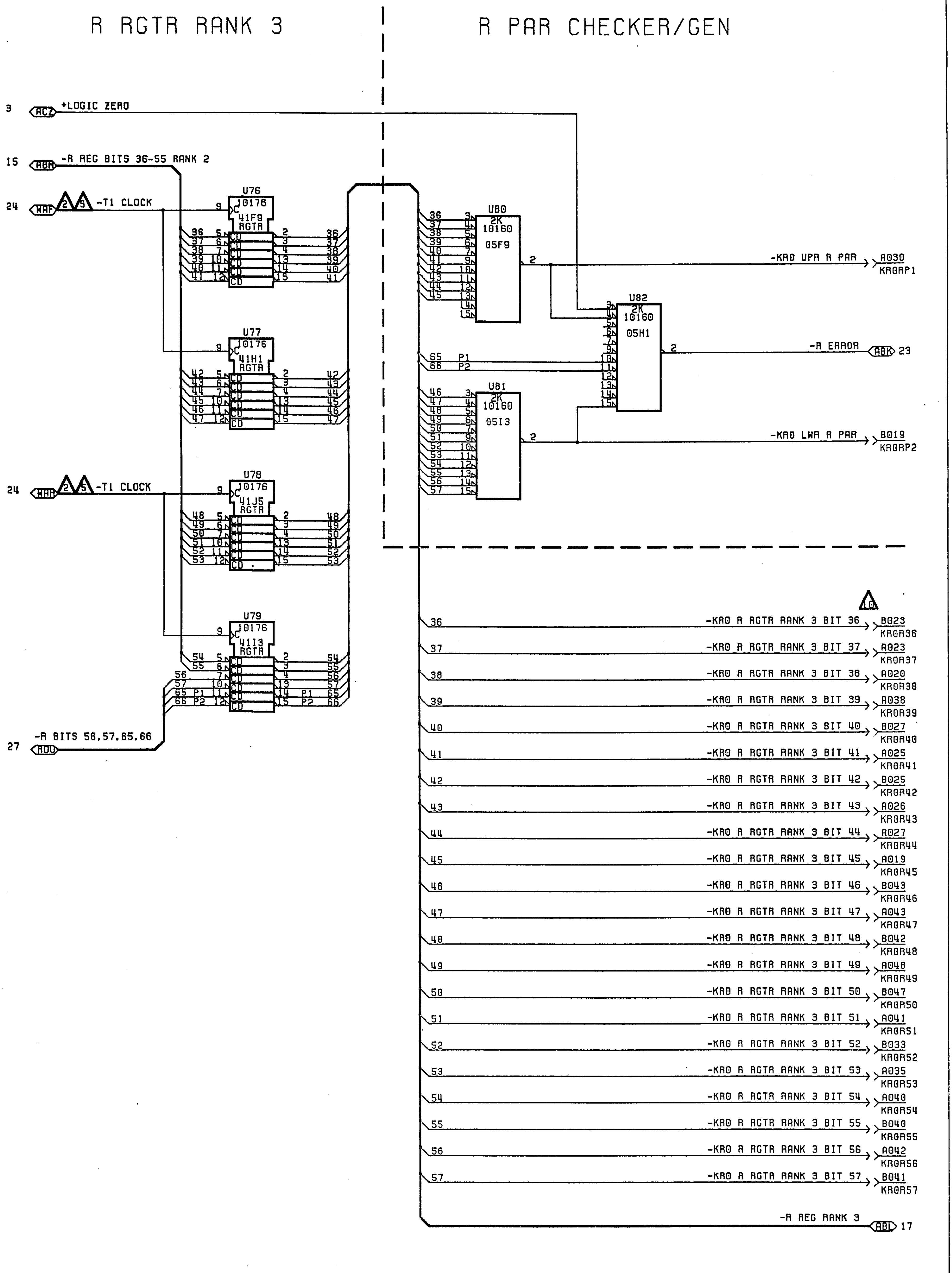
B	DWG NO. 53575536		DATE 11/01/85	REV A
SHEET NO.	14	60462210	PAGE KA-14	

R BARREL RANKS 0-2 BITS 36-55


U75
1CT0
54L9
2 CBC -CNTR BIT 1 62 RD ADRS 0
2 CBR -CNTR BIT 2 61 RD ADRS 1
50 OUTPUT ENABLE A
28 OUTPUT ENABLE B
53 WR ADRS 0
48 WR ADRS 1
2 ZE2 +LOGIC ZERO 55 +WR ENABLE A
54 +WR ENABLE B
24 RCD 5 -T1 CLOCK 46 CLOCK
18 J36 -R REG RANK 4 BIT 36 44 DATA IN BIT 0
18 J37 -R REG RANK 4 BIT 37 47 1
18 J38 -R REG RANK 4 BIT 38 42 2
18 J39 -R REG RANK 4 BIT 39 49 3
18 J40 -R REG RANK 4 BIT 40 45 4
18 J41 -R REG RANK 4 BIT 41 38 5
18 J42 -R REG RANK 4 BIT 42 39 6
18 J43 -R REG RANK 4 BIT 43 41 7
18 J44 -R REG RANK 4 BIT 44 32 8
18 J45 -R REG RANK 4 BIT 45 31 9
19 J46 -R REG RANK 4 BIT 46 58 DATA IN BIT 10
19 J47 -R REG RANK 4 BIT 47 57 11
19 J48 -R REG RANK 4 BIT 48 56 12
19 J49 -R REG RANK 4 BIT 49 59 13
19 J50 -R REG RANK 4 BIT 50 40 14
19 J51 -R REG RANK 4 BIT 51 27 15
19 J52 -R REG RANK 4 BIT 52 29 16
19 J53 -R REG RANK 4 BIT 53 24 17
19 J54 -R REG RANK 4 BIT 54 30 18
19 J55 -R REG RANK 4 BIT 55 25 19
DATA OUT BIT 0 64 36
1 65 37
2 2 38
3 22 39
4 21 40
5 19 41
6 67 42
7 63 43
8 11 44
9 1 45
DATA OUT BIT 10 5 46
11 6 47
12 7 48
13 8 49
14 14 50
15 16 51
16 10 52
17 12 53
18 13 54
19 23 55
-R REG BITS 36-55 RANK 2
ABH 16

⚠5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD R BARREL BITS 36-55 RANKS 0-2 TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		N	SHEET NO. 15	60462210	PAGE KA-15

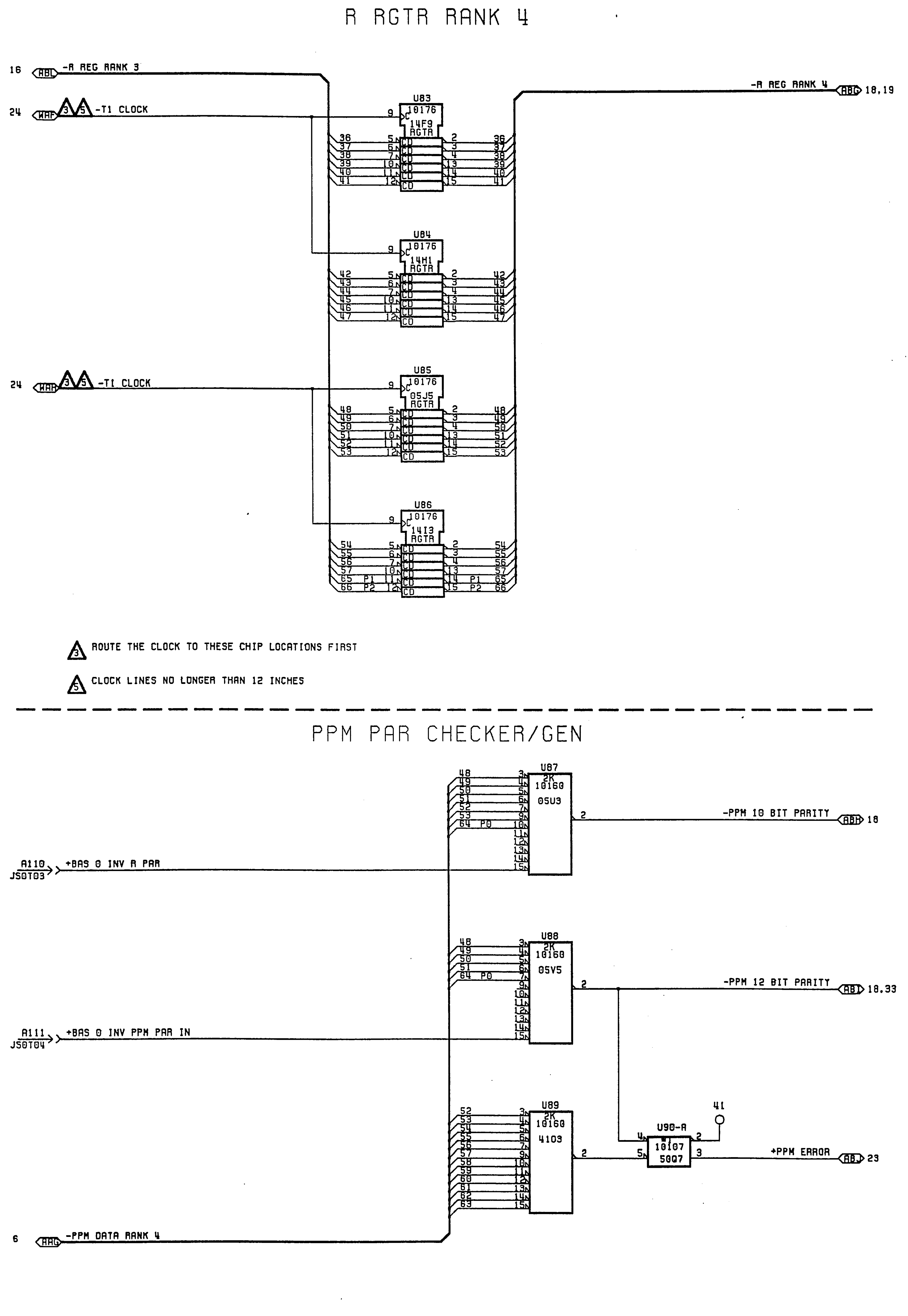

R RGTR RANK 3
R PAR CHECKER/GEN
3 RCZ +LOGIC ZERO
15 RBM -R REG BITS 36-55 RANK 2
24 RAF 2 5 -T1 CLOCK
24 RAH 2 5 -T1 CLOCK
27 RDD -R BITS 56,57,65,66
U76 10176 41F9 RGTR
U77 10176 41H1 RGTR
U78 10176 41J5 RGTR
U79 10176 41I3 RGTR
U80 2K 10160 05F9
U81 2K 10160 05I3
U82 2K 10160 05H1
65 P1
66 P2
-KR0 UPR R PAR A030 KR0RP1
-R ERROR RBK 23
-KR0 LWR R PAR B019 KR0RP2
10
-KR0 R RGTR RANK 3 BIT 36 B023 KR0R36
-KR0 R RGTR RANK 3 BIT 37 A023 KR0R37
-KR0 R RGTR RANK 3 BIT 38 A020 KR0R38
-KR0 R RGTR RANK 3 BIT 39 A038 KR0R39
-KR0 R RGTR RANK 3 BIT 40 B027 KR0R40
-KR0 R RGTR RANK 3 BIT 41 A025 KR0R41
-KR0 R RGTR RANK 3 BIT 42 B025 KR0R42
-KR0 R RGTR RANK 3 BIT 43 A026 KR0R43
-KR0 R RGTR RANK 3 BIT 44 A027 KR0R44
-KR0 R RGTR RANK 3 BIT 45 A019 KR0R45
-KR0 R RGTR RANK 3 BIT 46 B043 KR0R46
-KR0 R RGTR RANK 3 BIT 47 A043 KR0R47
-KR0 R RGTR RANK 3 BIT 48 B042 KR0R48
-KR0 R RGTR RANK 3 BIT 49 A048 KR0R49
-KR0 R RGTR RANK 3 BIT 50 B047 KR0R50
-KR0 R RGTR RANK 3 BIT 51 A041 KR0R51
-KR0 R RGTR RANK 3 BIT 52 B033 KR0R52
-KR0 R RGTR RANK 3 BIT 53 A035 KR0R53
-KR0 R RGTR RANK 3 BIT 54 A040 KR0R54
-KR0 R RGTR RANK 3 BIT 55 B040 KR0R55
-KR0 R RGTR RANK 3 BIT 56 A042 KR0R56
-KR0 R RGTR RANK 3 BIT 57 B041 KR0R57
-R REG RANK 3 RBL 17

2 ROUTE THE CLOCK TO THESE CHIP LOCATIONS LAST

5 CLOCK LINES NO LONGER THAN 12 INCHES

10 IF POSSIBLE IT IS BETTER IF THESE OUTPUT
LINES ARE AT LEAST 18 INCHES

CONTROL DATA	REGISTER BOARD R REGISTER RANK 3 AND R PARITY CHECKER/GEN TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 16	60462210		PAGE KR-16

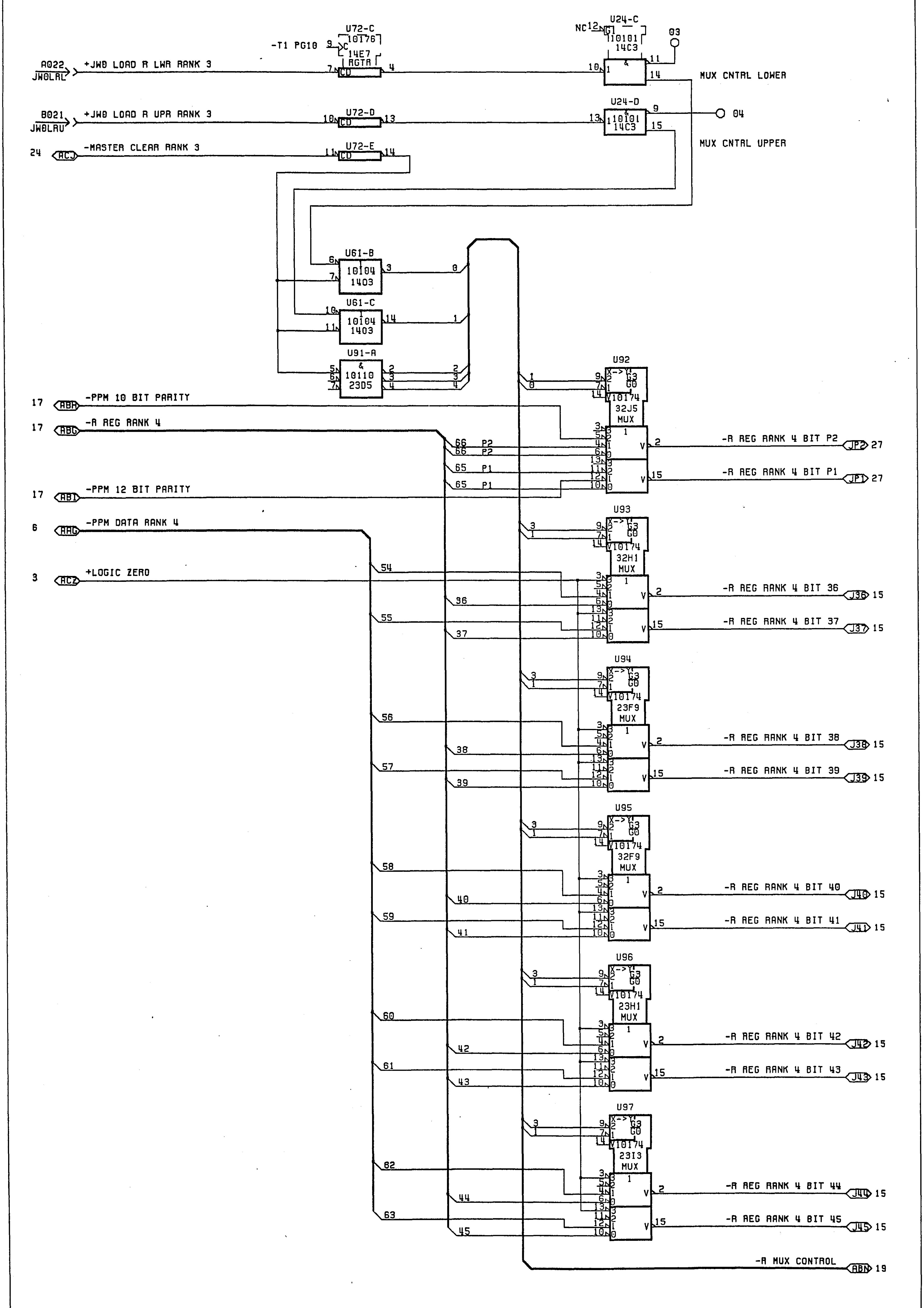


3 ROUTE THE CLOCK TO THESE CHIP LOCATIONS FIRST

5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD R REGISTER RANK 4 AND PPM PARITY CHECKER/GEN TYPE 1KRH	8	DWG NO. 53575536	DATE 11/01/85	REV A
		N	SHEET NO. 17	60462210	PAGE KR-17

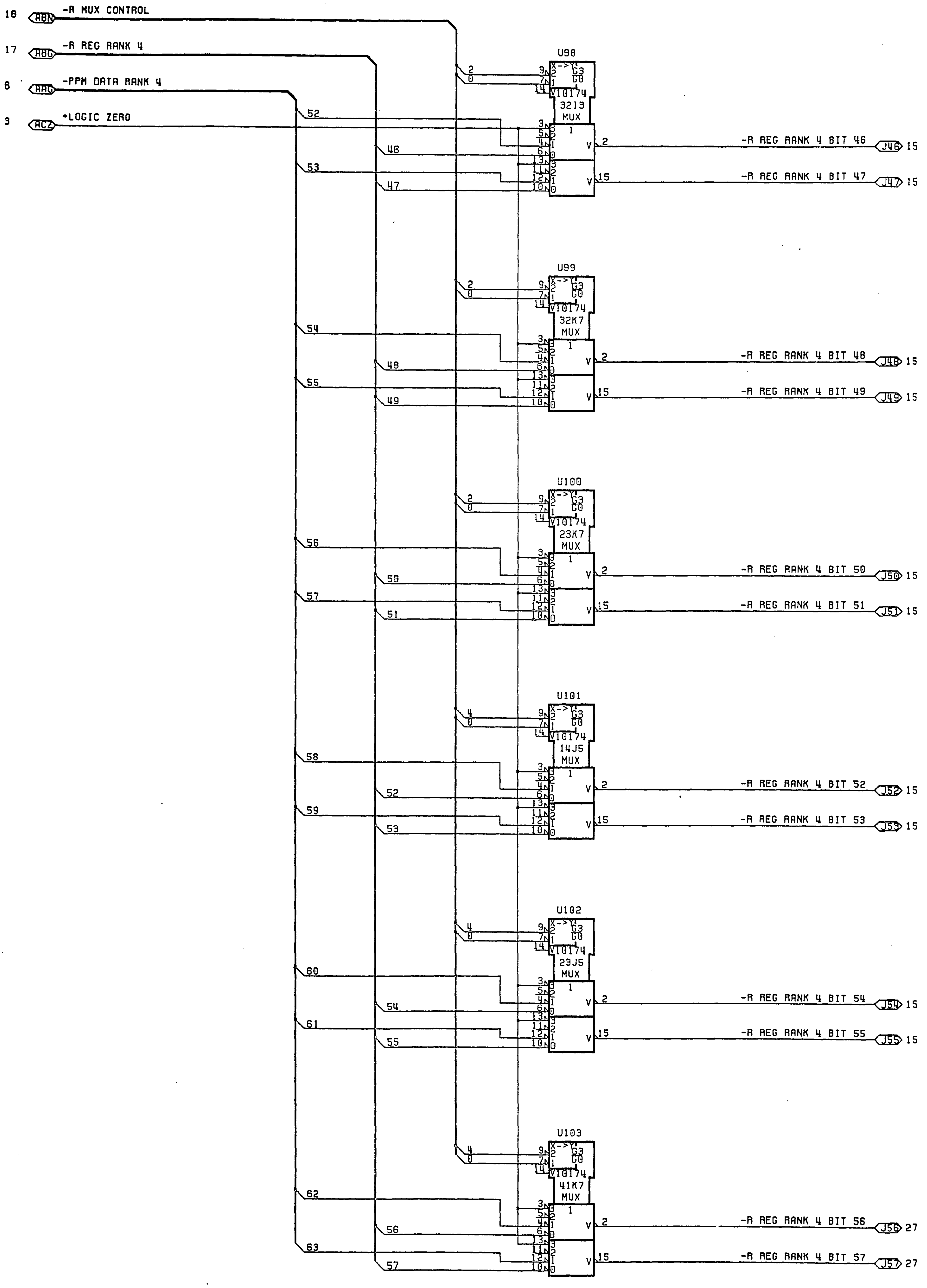
R MUX BITS 36-45, PAR BITS 1,2



U72-C
10176
14E7
RGTR
-T1 PG10
A022
JW0LRL
+JW0 LOAD R LWR RANK 3
B021
JW0LRU
+JW0 LOAD R UPR RANK 3
24 ACJ -MASTER CLEAR RANK 3
U72-D
U72-E
NC
U24-C
10101
14C3
03
MUX CNTRL LOWER
U24-D
10101
14C3
04
MUX CNTRL UPPER
U61-B
10104
14D3
U61-C
10104
14D3
U91-A
10110
23D5
17 ABH -PPM 10 BIT PARITY
17 ABG -R REG RANK 4
17 ABI -PPM 12 BIT PARITY
6 AAG -PPM DATA RANK 4
3 ACZ +LOGIC ZERO
U92
10174
32J5
MUX
U93
10174
32H1
MUX
U94
10174
23F9
MUX
U95
10174
32F9
MUX
U96
10174
23H1
MUX
U97
10174
23I3
MUX
-R REG RANK 4 BIT P2 JP2 27
-R REG RANK 4 BIT P1 JP1 27
-R REG RANK 4 BIT 36 J36 15
-R REG RANK 4 BIT 37 J37 15
-R REG RANK 4 BIT 38 J38 15
-R REG RANK 4 BIT 39 J39 15
-R REG RANK 4 BIT 40 J40 15
-R REG RANK 4 BIT 41 J41 15
-R REG RANK 4 BIT 42 J42 15
-R REG RANK 4 BIT 43 J43 15
-R REG RANK 4 BIT 44 J44 15
-R REG RANK 4 BIT 45 J45 15
-R MUX CONTROL ABN 19

CONTROL DATA	REGISTER BOARD R MUX BITS 36-45, P1, P2 TYPE 1KRH	B	DWG NO. 59575536	DATE 11/01/85	REV A
		N	SHEET NO. 18	60462210	PAGE KA-18

R MUX BITS 46-57

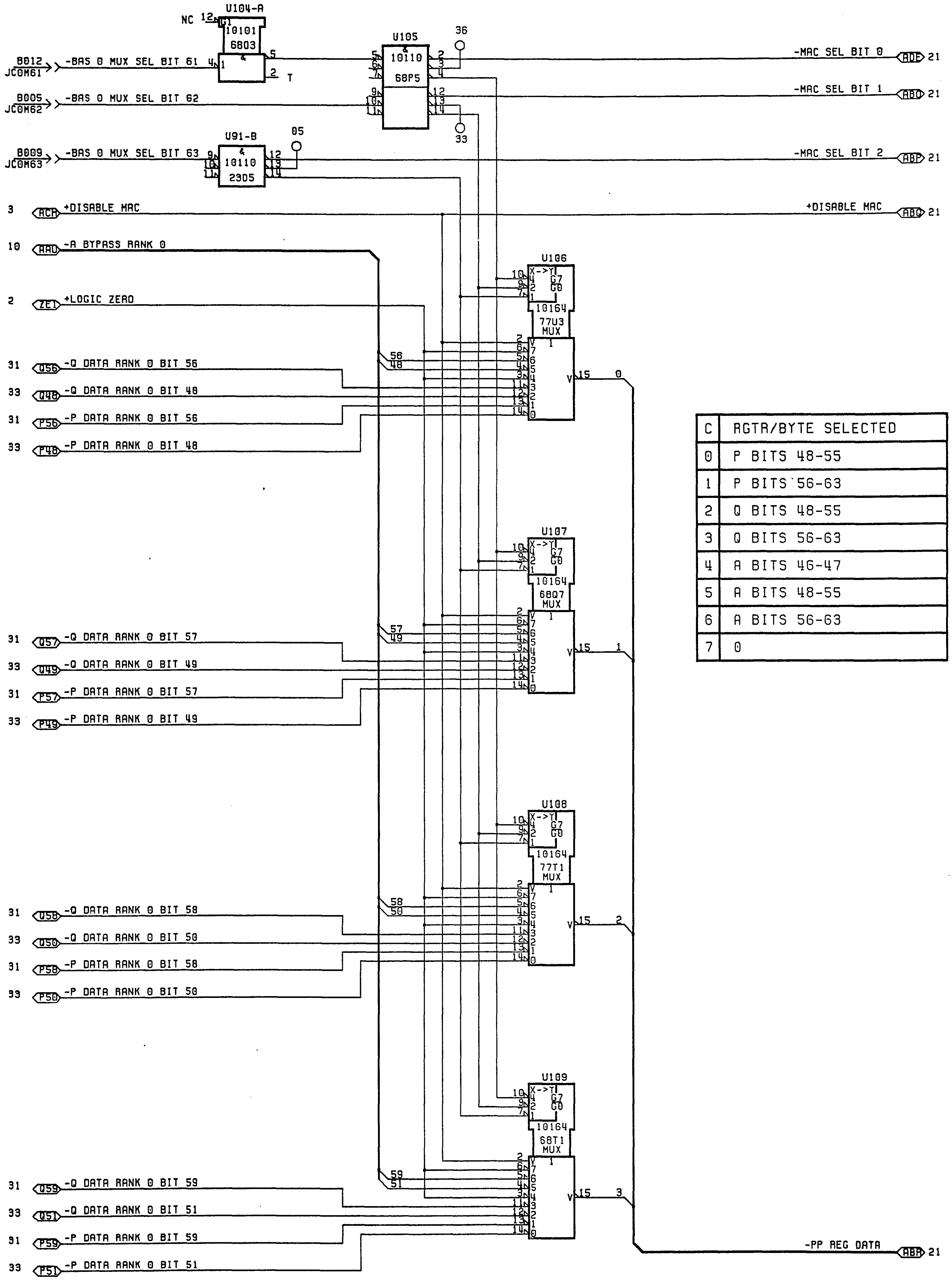

18 ABN -R MUX CONTROL
17 ABG -R REG RANK 4
6 AAG -PPM DATA RANK 4
3 ACZ +LOGIC ZERO
U98 10174 3213 MUX
U99 10174 32K7 MUX
U100 10174 23K7 MUX
U101 10174 14J5 MUX
U102 10174 23J5 MUX
U103 10174 41K7 MUX
-R REG RANK 4 BIT 46 J46 15
-R REG RANK 4 BIT 47 J47 15
-R REG RANK 4 BIT 48 J48 15
-R REG RANK 4 BIT 49 J49 15
-R REG RANK 4 BIT 50 J50 15
-R REG RANK 4 BIT 51 J51 15
-R REG RANK 4 BIT 52 J52 15
-R REG RANK 4 BIT 53 J53 15
-R REG RANK 4 BIT 54 J54 15
-R REG RANK 4 BIT 55 J55 15
-R REG RANK 4 BIT 56 J56 27
-R REG RANK 4 BIT 57 J57 27

CONTROL DATA

REGISTER BOARD
R MUX BITS 46-57
TYPE 1KAH

B	DWG NO. 53575536	DATE 11/01/85	REV A
SHEET NO. 19	60462210	PAGE KA-19	

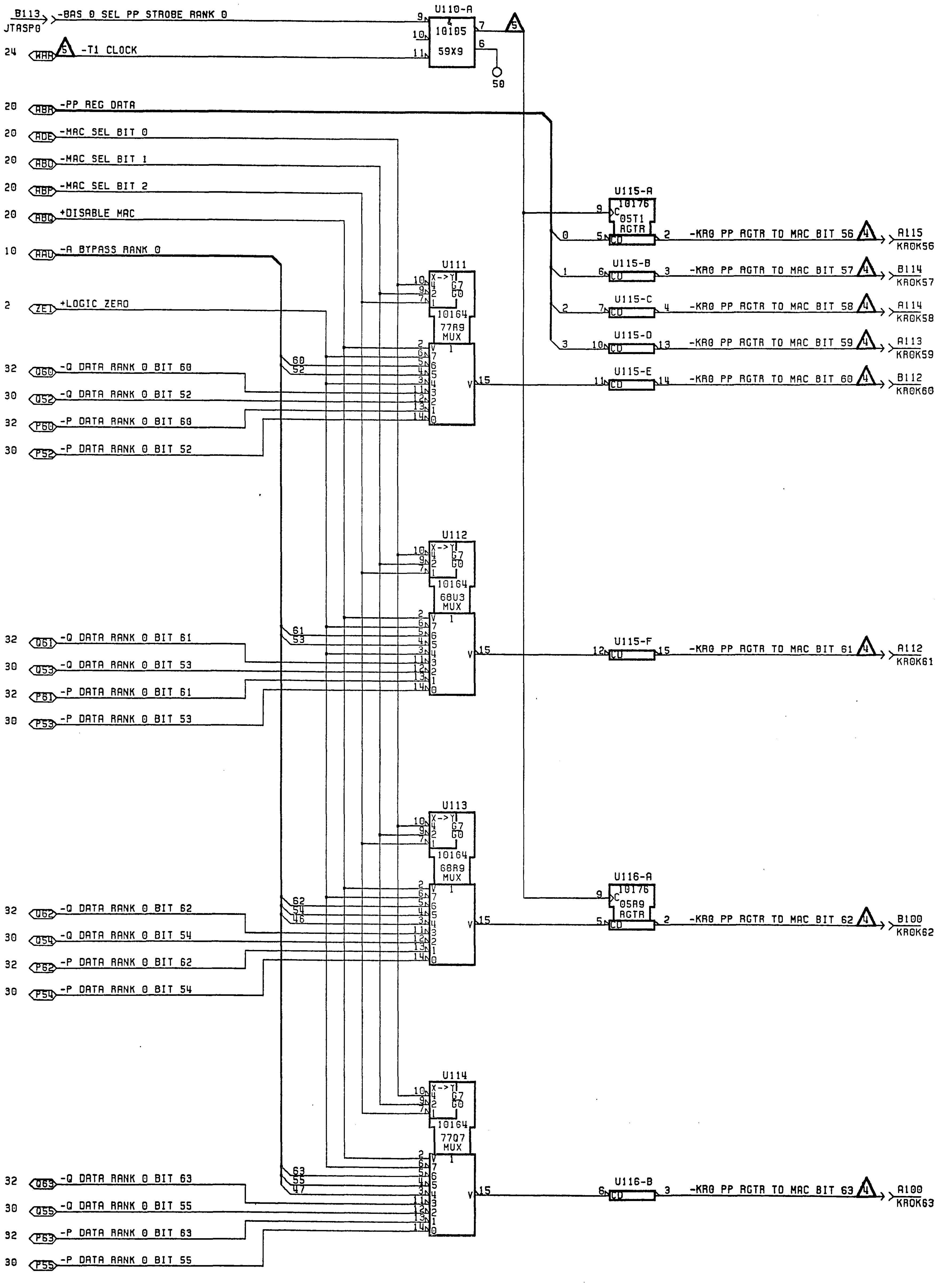
MAC RGTR / BYTE MUX BITS 0-3


U104-A
NC 12 G1
10101
6803
B012 JCOM61 -BAS 0 MUX SEL BIT 61 4 1
5
2 T
U105
10110
68P5
36
33
B005 JCOM62 -BAS 0 MUX SEL BIT 62
U91-B
10110
2305
05
B009 JCOM63 -BAS 0 MUX SEL BIT 63
-MAC SEL BIT 0 ADE 21
-MAC SEL BIT 1 ABD 21
-MAC SEL BIT 2 ABF 21
3 ACR +DISABLE MAC
+DISABLE MAC ABG 21
10 AAU -A BYPASS RANK 0
2 ZE1 +LOGIC ZERO
U106 10164 77U3 MUX
U107 10164 68Q7 MUX
U108 10164 77T1 MUX
U109 10164 68T1 MUX
X->Y G7 G0
31 Q56 -Q DATA RANK 0 BIT 56
33 Q48 -Q DATA RANK 0 BIT 48
31 P56 -P DATA RANK 0 BIT 56
33 P48 -P DATA RANK 0 BIT 48
56
48
31 Q57 -Q DATA RANK 0 BIT 57
33 Q49 -Q DATA RANK 0 BIT 49
31 P57 -P DATA RANK 0 BIT 57
33 P49 -P DATA RANK 0 BIT 49
57
49
31 Q58 -Q DATA RANK 0 BIT 58
33 Q50 -Q DATA RANK 0 BIT 50
31 P58 -P DATA RANK 0 BIT 58
33 P50 -P DATA RANK 0 BIT 50
58
50
31 Q59 -Q DATA RANK 0 BIT 59
33 Q51 -Q DATA RANK 0 BIT 51
31 P59 -P DATA RANK 0 BIT 59
33 P51 -P DATA RANK 0 BIT 51
59
51
V 15 0
V 15 1
V 15 2
V 15 3
-PP REG DATA ABH 21

C	RGTR/BYTE SELECTED
0	P BITS 48-55
1	P BITS 56-63
2	Q BITS 48-55
3	Q BITS 56-63
4	A BITS 46-47
5	A BITS 48-55
6	A BITS 56-63
7	0

CONTROL DATA
REGISTER BOARD
MAC REGISTER/BYTE MUX BITS 0-3
TYPE 1KRH
N
B
DWG NO. 53575536
DATE 11/01/85
REV A
SHEET NO. 20
60462210
PAGE KR-20

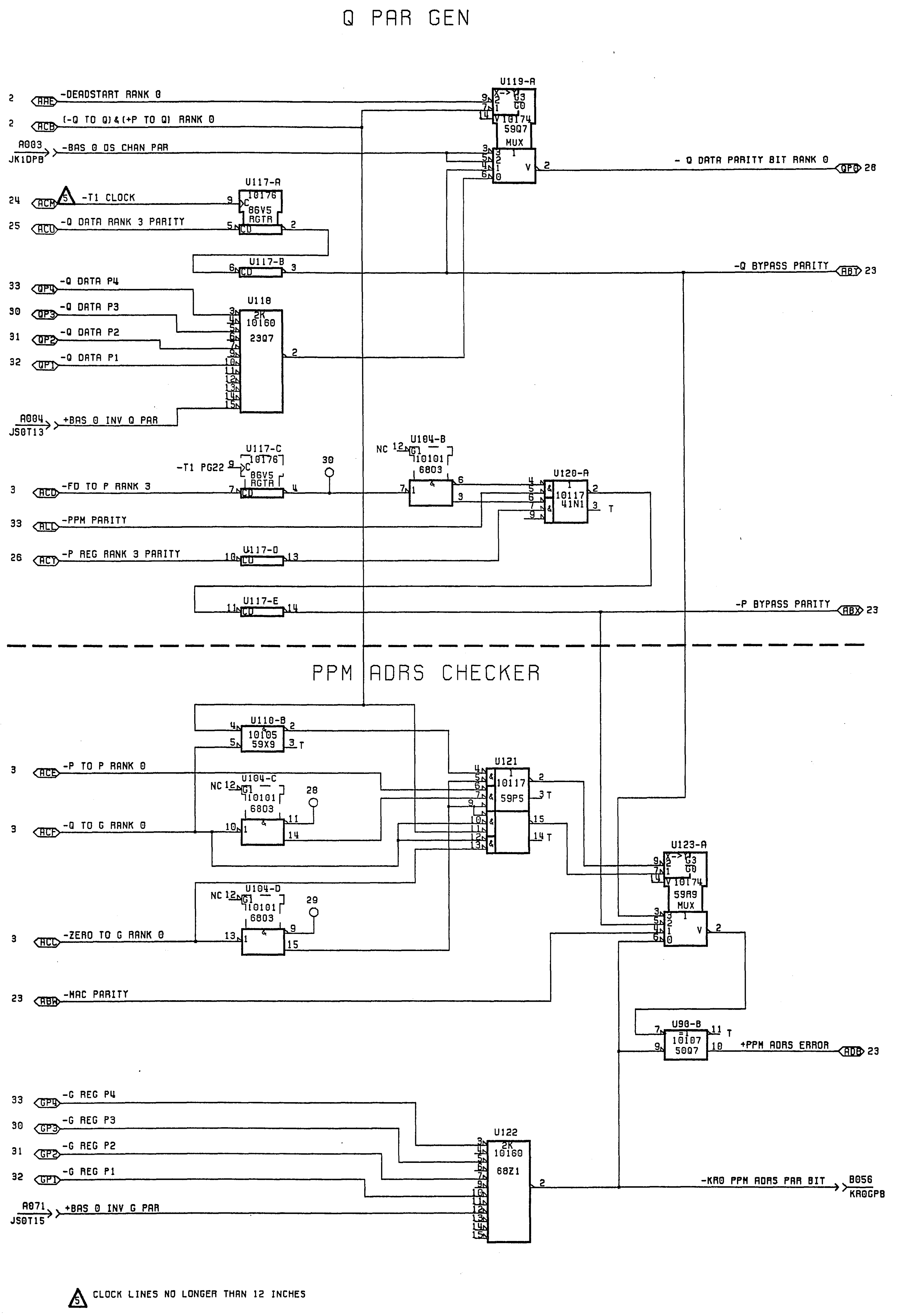
MAC RGTR / BYTE MUX BITS 4-7


B113 JTASP0 -BAS 0 SEL PP STROBE RANK 0
24 AAA -T1 CLOCK
U110-A 10105 59X9
9 10 11 7 6 58
20 A8A -PP REG DATA
20 ADE -MAC SEL BIT 0
20 A8D -MAC SEL BIT 1
20 A8P -MAC SEL BIT 2
20 A8Q +DISABLE MAC
10 AAD -A BYPASS RANK 0
2 ZE1 +LOGIC ZERO
U111 10164 77A9 MUX
32 Q60 -Q DATA RANK 0 BIT 60
30 Q52 -Q DATA RANK 0 BIT 52
32 P60 -P DATA RANK 0 BIT 60
30 P52 -P DATA RANK 0 BIT 52
U112 10164 68U3 MUX
32 Q61 -Q DATA RANK 0 BIT 61
30 Q53 -Q DATA RANK 0 BIT 53
32 P61 -P DATA RANK 0 BIT 61
30 P53 -P DATA RANK 0 BIT 53
U113 10164 68A9 MUX
32 Q62 -Q DATA RANK 0 BIT 62
30 Q54 -Q DATA RANK 0 BIT 54
32 P62 -P DATA RANK 0 BIT 62
30 P54 -P DATA RANK 0 BIT 54
U114 10164 7707 MUX
32 Q63 -Q DATA RANK 0 BIT 63
30 Q55 -Q DATA RANK 0 BIT 55
32 P63 -P DATA RANK 0 BIT 63
30 P55 -P DATA RANK 0 BIT 55
U115-A 10176 05T1 AGTR
-KA0 PP RGTR TO MAC BIT 56 A115 KAOK56
U115-B -KA0 PP RGTR TO MAC BIT 57 B114 KAOK57
U115-C -KA0 PP RGTR TO MAC BIT 58 A114 KAOK58
U115-D -KA0 PP RGTR TO MAC BIT 59 A113 KAOK59
U115-E -KA0 PP RGTR TO MAC BIT 60 B112 KAOK60
U115-F -KA0 PP RGTR TO MAC BIT 61 A112 KAOK61
U116-A 10176 05A9 AGTR
-KA0 PP RGTR TO MAC BIT 62 B100 KAOK62
U116-B -KA0 PP RGTR TO MAC BIT 63 A100 KAOK63

4 SHORT (NO LONGER THAN 6 INCHES) AND NOT TERMINATED

5 CLOCK LINES NO LONGER THAN 12 INCHES

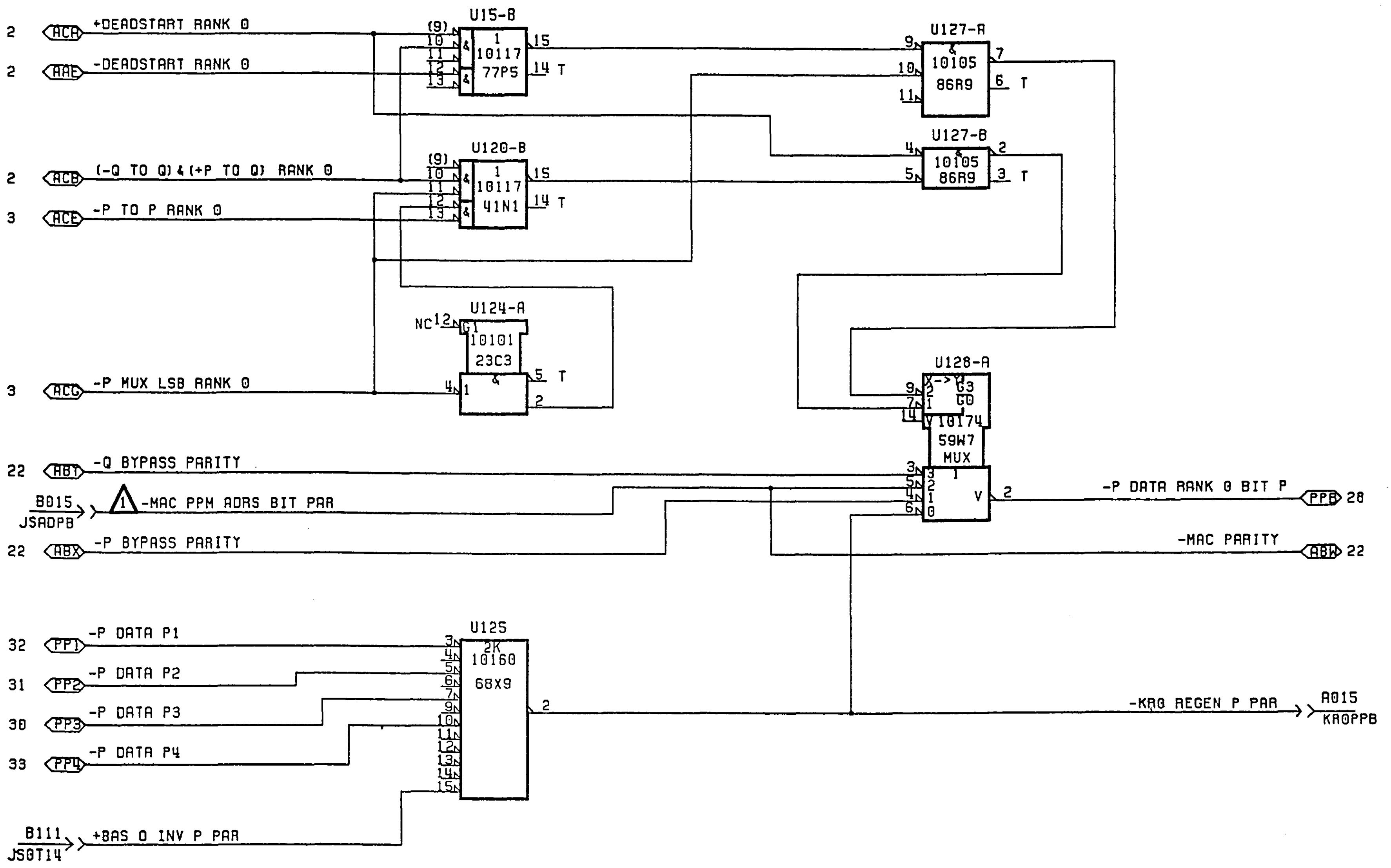
CONTROL DATA	REGISTER BOARD MAC REGISTER/BYTE MUX BITS 4-7	B	DWG NO. 53575536	DATE 11/01/85	REV A
	TYPE 1KAH	N	SHEET NO. 21	60462210	PAGE KA-21



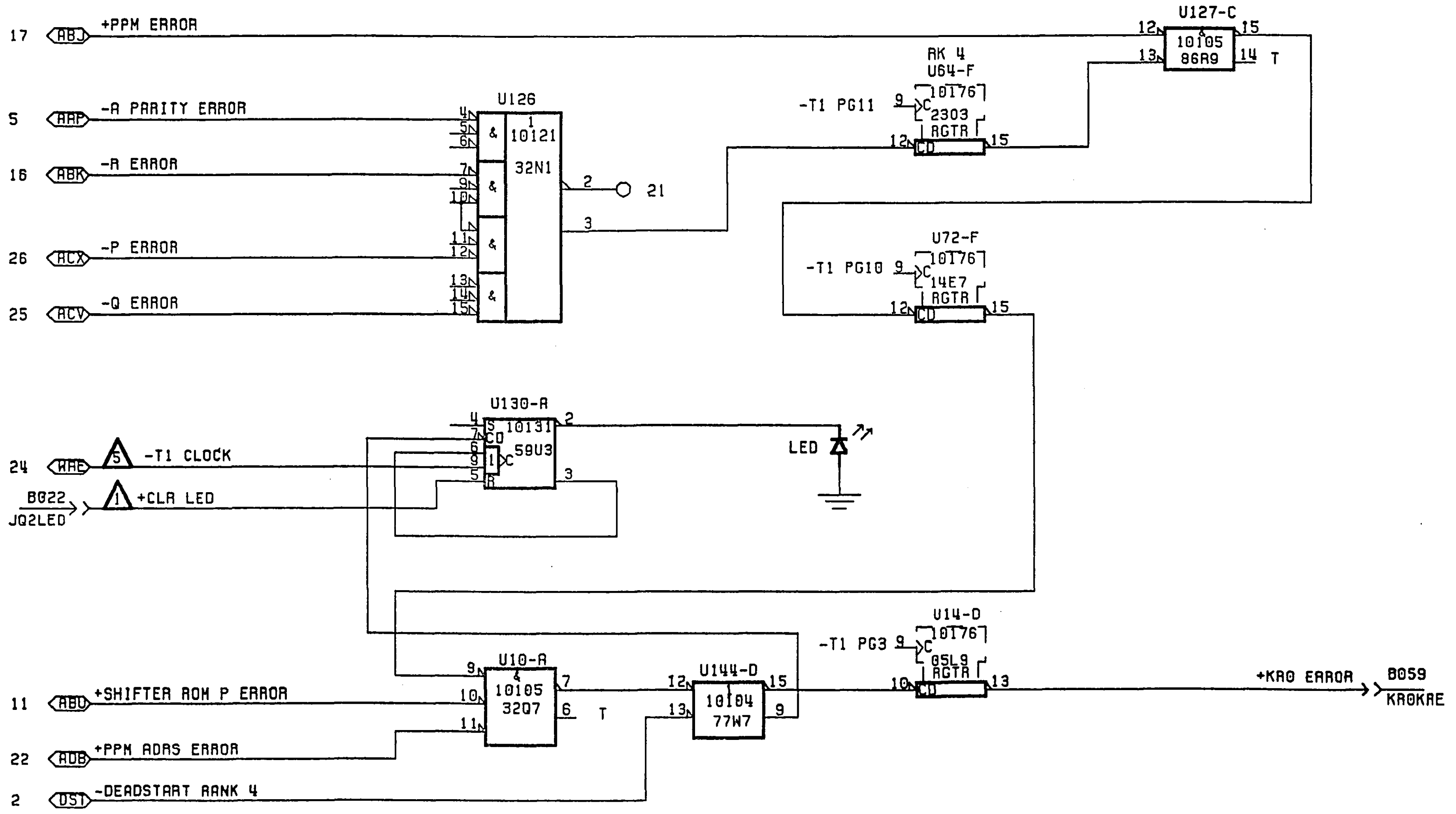
5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD Q PARITY GENERATOR PPM ADDRESS CHECKER TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		N	SHEET NO. 22	60462210	PAGE KR-22

P PAR GEN



KR ERROR SUMMARY

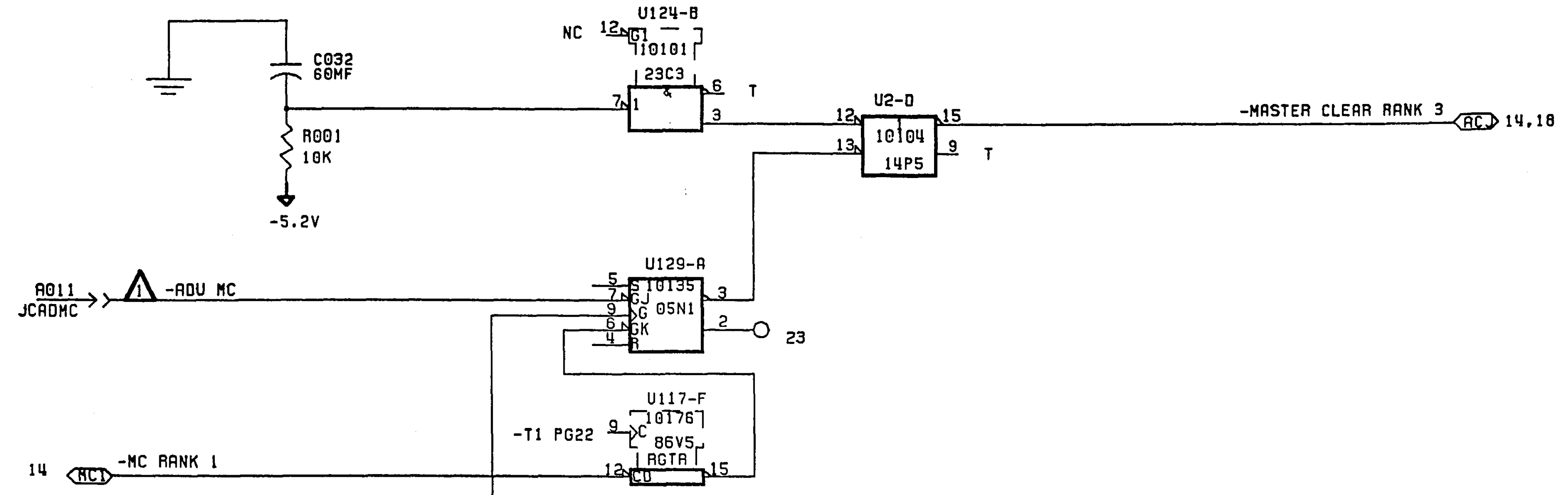


△1 NOT TERMINATED

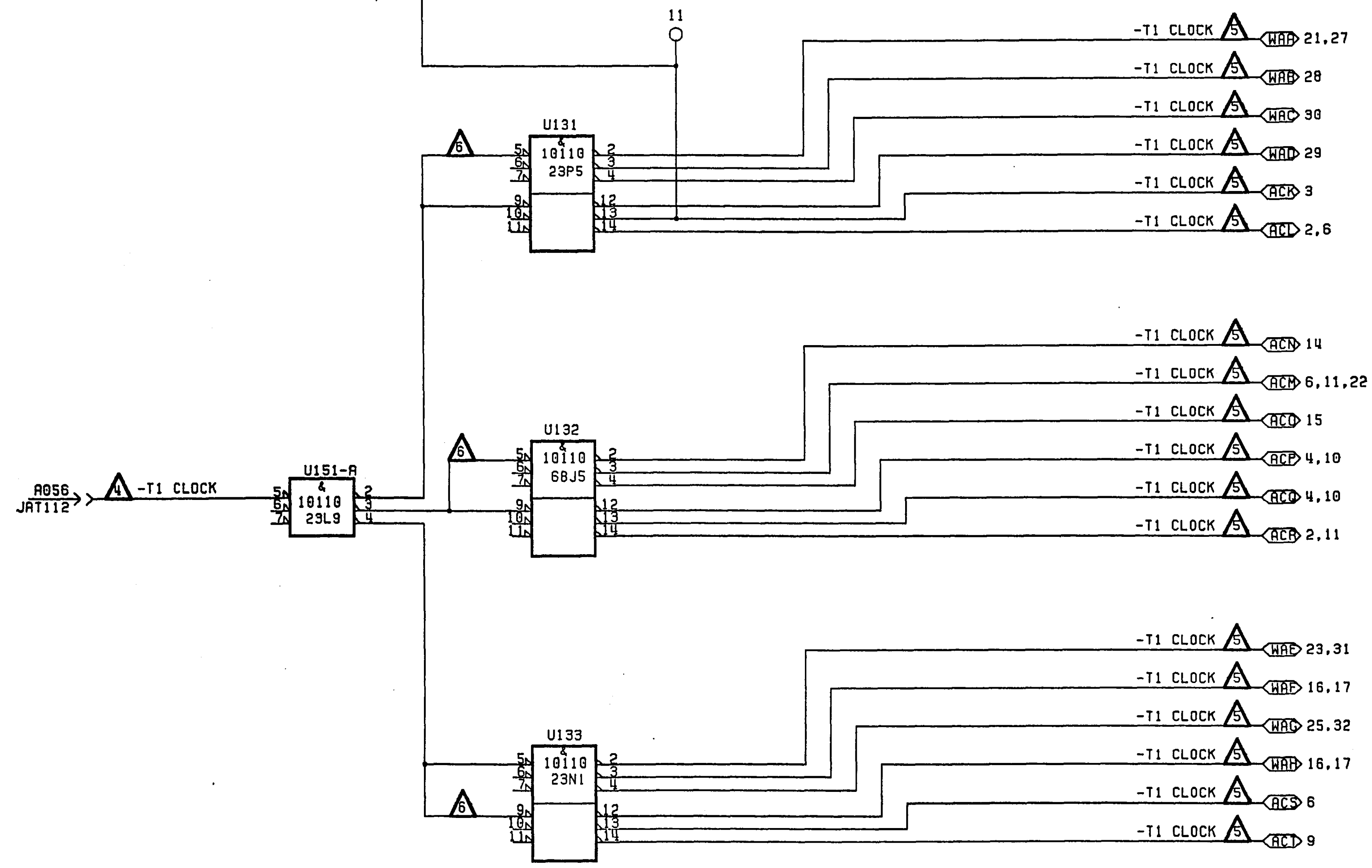
△5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD P PARITY GENERATOR KR ERROR SUMMARY TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
	N	SHEET NO. 23	60462210	PAGE KR-23	

PWR ON MC



T1 CLK F/O



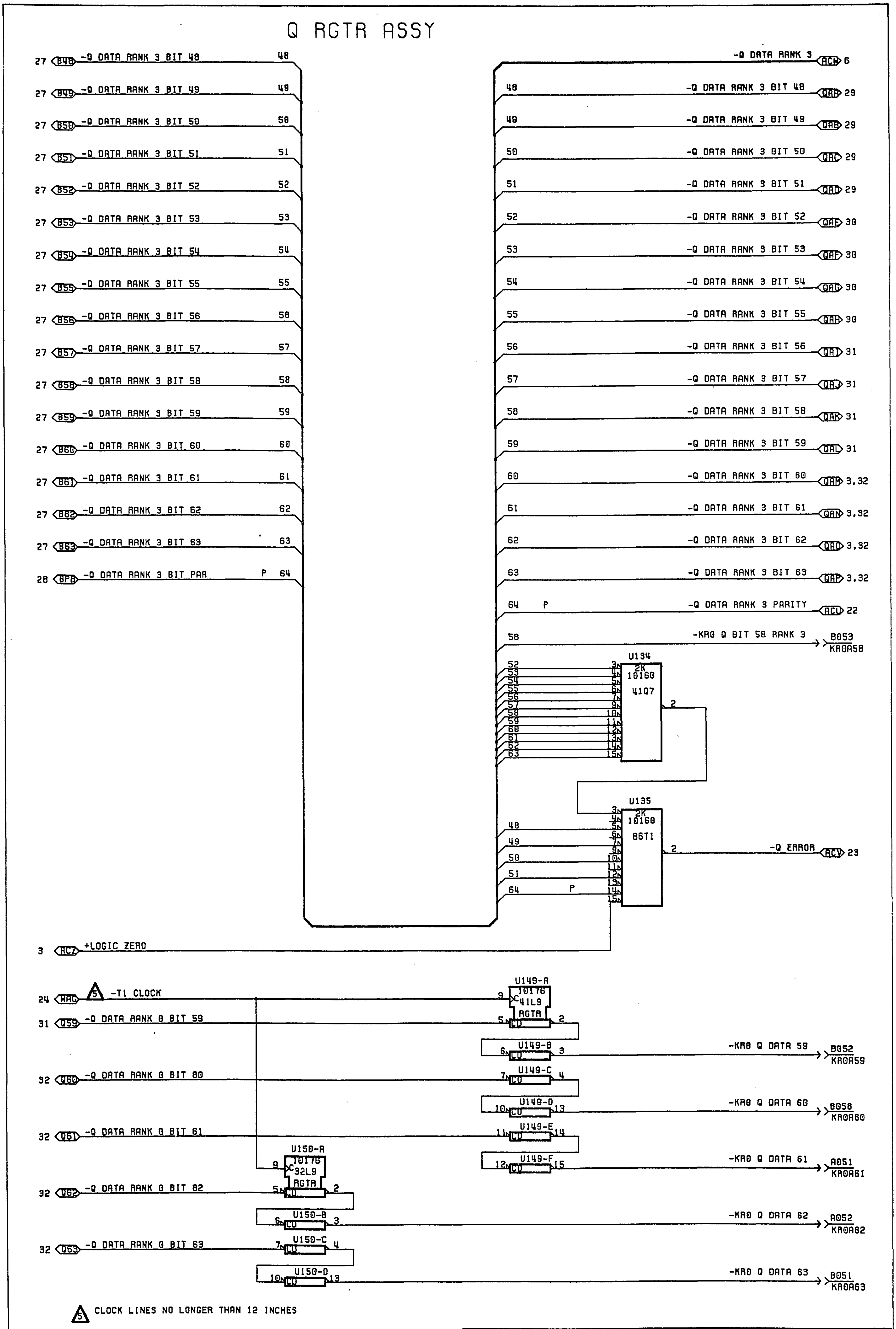
1 NOT TERMINATED

4 INPUT CLOCK LINE NO LONGER THAN 4 INCHES

5 CLOCK LINES NO LONGER THAN 12 INCHES

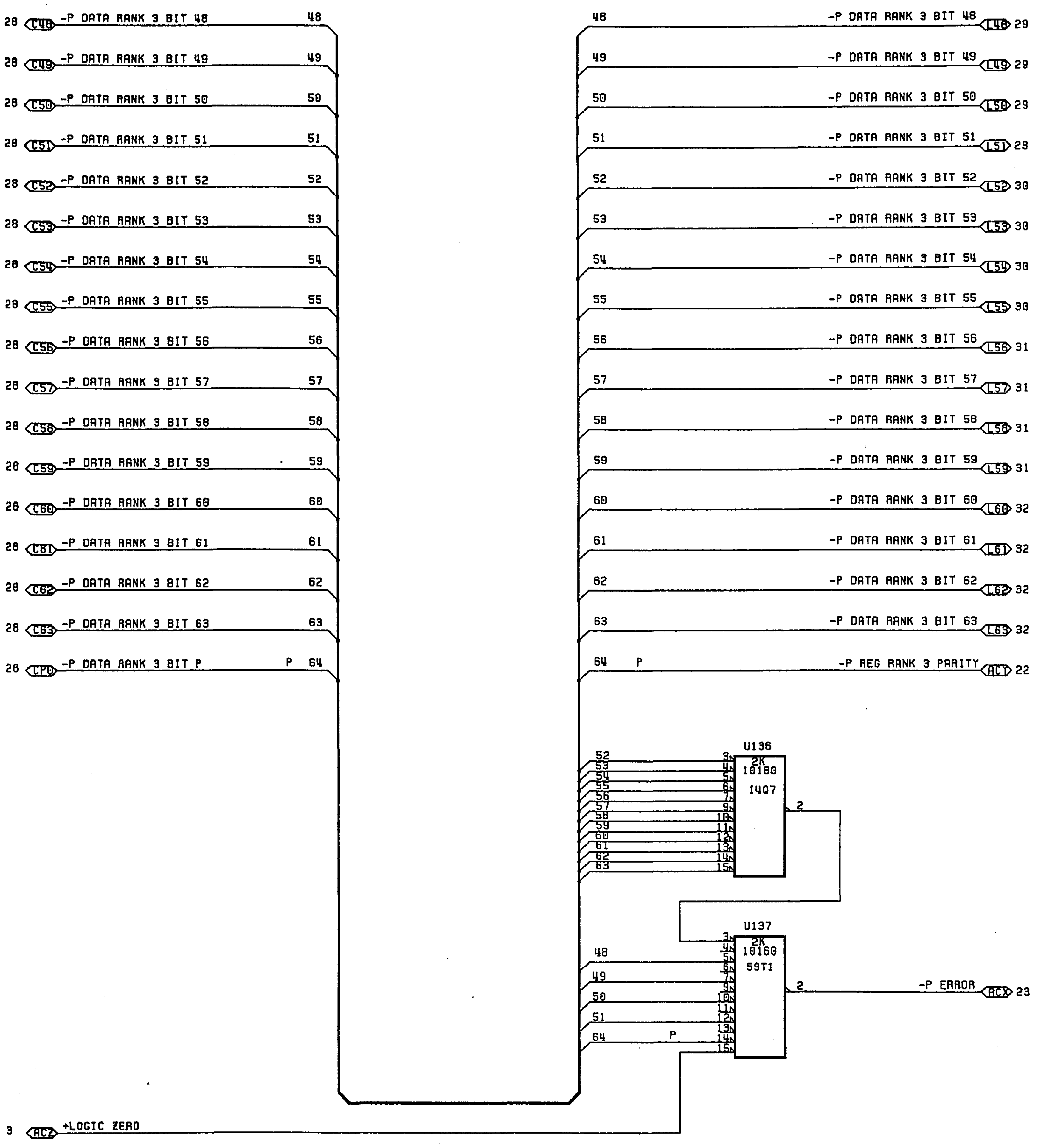
6 CLOCK LINES NO LONGER THAN 7 INCHES

CONTROL DATA	REGISTER BOARD POWER ON MASTER CLEAR T1 CLOCK FANOUT TYPE 1KAH	B	DWG NO. 59575538	DATE 11/01/85	REV A
		N	SHEET NO. 24	60462210	PAGE KA-24


Q RGTR ASSY
27 B48 -Q DATA RANK 3 BIT 48 48
27 B49 -Q DATA RANK 3 BIT 49 49
27 B50 -Q DATA RANK 3 BIT 50 50
27 B51 -Q DATA RANK 3 BIT 51 51
27 B52 -Q DATA RANK 3 BIT 52 52
27 B53 -Q DATA RANK 3 BIT 53 53
27 B54 -Q DATA RANK 3 BIT 54 54
27 B55 -Q DATA RANK 3 BIT 55 55
27 B56 -Q DATA RANK 3 BIT 56 56
27 B57 -Q DATA RANK 3 BIT 57 57
27 B58 -Q DATA RANK 3 BIT 58 58
27 B59 -Q DATA RANK 3 BIT 59 59
27 B60 -Q DATA RANK 3 BIT 60 60
27 B61 -Q DATA RANK 3 BIT 61 61
27 B62 -Q DATA RANK 3 BIT 62 62
27 B63 -Q DATA RANK 3 BIT 63 63
28 BPB -Q DATA RANK 3 BIT PAR P 64
-Q DATA RANK 3 ACW 6
48 -Q DATA RANK 3 BIT 48 QAA 29
49 -Q DATA RANK 3 BIT 49 QAB 29
50 -Q DATA RANK 3 BIT 50 QAC 29
51 -Q DATA RANK 3 BIT 51 QAD 29
52 -Q DATA RANK 3 BIT 52 QAE 30
53 -Q DATA RANK 3 BIT 53 QAF 30
54 -Q DATA RANK 3 BIT 54 QAG 30
55 -Q DATA RANK 3 BIT 55 QAH 30
56 -Q DATA RANK 3 BIT 56 QAI 31
57 -Q DATA RANK 3 BIT 57 QAJ 31
58 -Q DATA RANK 3 BIT 58 QAK 31
59 -Q DATA RANK 3 BIT 59 QAL 31
60 -Q DATA RANK 3 BIT 60 QAM 3,32
61 -Q DATA RANK 3 BIT 61 QAN 3,32
62 -Q DATA RANK 3 BIT 62 QAO 3,32
63 -Q DATA RANK 3 BIT 63 QAP 3,32
64 P -Q DATA RANK 3 PARITY ACU 22
58 -KR0 Q BIT 58 RANK 3 B053 KR0A58
U134 2K 10160 4I07
52 53 54 55 56 57 58 59 60 61 62 63
3 4 5 6 7 9 10 11 12 13 14 15
2
U135 2K 10160 86T1
48 49 50 51 64 P
3 4 5 6 7 9 10 11 12 13 14 15
2 -Q ERROR ACV 23
3 ACZ +LOGIC ZERO
24 HAG 5 -T1 CLOCK
U149-A 10176 41L9 RGTR
9 C 5 CD 2
31 Q59 -Q DATA RANK 0 BIT 59
U149-B 6 CD 3 -KR0 Q DATA 59 B052 KR0A59
32 Q60 -Q DATA RANK 0 BIT 60
U149-C 7 CD 4
U149-D 10 CD 13 -KR0 Q DATA 60 B058 KR0A60
32 Q61 -Q DATA RANK 0 BIT 61
U149-E 11 CD 14
U149-F 12 CD 15 -KR0 Q DATA 61 A051 KR0A61
U150-A 10176 32L9 RGTR
9 C 5 CD 2
32 Q62 -Q DATA RANK 0 BIT 62
U150-B 6 CD 3 -KR0 Q DATA 62 A052 KR0A62
32 Q63 -Q DATA RANK 0 BIT 63
U150-C 7 CD 4
U150-D 10 CD 13 -KR0 Q DATA 63 B051 KR0A63
5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD Q REGISER ASSEMBLY TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		N SHEET NO. 25	60462210	PAGE KA-25	

P RGTR ASSY


28 C48 -P DATA RANK 3 BIT 48 48
28 C49 -P DATA RANK 3 BIT 49 49
28 C50 -P DATA RANK 3 BIT 50 50
28 C51 -P DATA RANK 3 BIT 51 51
28 C52 -P DATA RANK 3 BIT 52 52
28 C53 -P DATA RANK 3 BIT 53 53
28 C54 -P DATA RANK 3 BIT 54 54
28 C55 -P DATA RANK 3 BIT 55 55
28 C56 -P DATA RANK 3 BIT 56 56
28 C57 -P DATA RANK 3 BIT 57 57
28 C58 -P DATA RANK 3 BIT 58 58
28 C59 -P DATA RANK 3 BIT 59 59
28 C60 -P DATA RANK 3 BIT 60 60
28 C61 -P DATA RANK 3 BIT 61 61
28 C62 -P DATA RANK 3 BIT 62 62
28 C63 -P DATA RANK 3 BIT 63 63
28 CP0 -P DATA RANK 3 BIT P P 64
48 -P DATA RANK 3 BIT 48 L48 29
49 -P DATA RANK 3 BIT 49 L49 29
50 -P DATA RANK 3 BIT 50 L50 29
51 -P DATA RANK 3 BIT 51 L51 29
52 -P DATA RANK 3 BIT 52 L52 30
53 -P DATA RANK 3 BIT 53 L53 30
54 -P DATA RANK 3 BIT 54 L54 30
55 -P DATA RANK 3 BIT 55 L55 30
56 -P DATA RANK 3 BIT 56 L56 31
57 -P DATA RANK 3 BIT 57 L57 31
58 -P DATA RANK 3 BIT 58 L58 31
59 -P DATA RANK 3 BIT 59 L59 31
60 -P DATA RANK 3 BIT 60 L60 32
61 -P DATA RANK 3 BIT 61 L61 32
62 -P DATA RANK 3 BIT 62 L62 32
63 -P DATA RANK 3 BIT 63 L63 32
64 P -P REG RANK 3 PARITY ACY 22
U136
2K
10160
14Q7
52 53 54 55 56 57 58 59 60 61 62 63
3 4 5 6 7 9 10 11 12 13 14 15
2
U137
2K
10160
59T1
48 49 50 51 64 P
3 4 5 6 7 9 10 11 12 13 14 15
2
-P ERROR ACX 23
3 ACZ +LOGIC ZERO

CONTROL DATA

REGISTER BOARD
P REGISER ASSEMBLY
TYPE 1KAH

N

B

DWG NO. 53575536

DATE 11/01/85

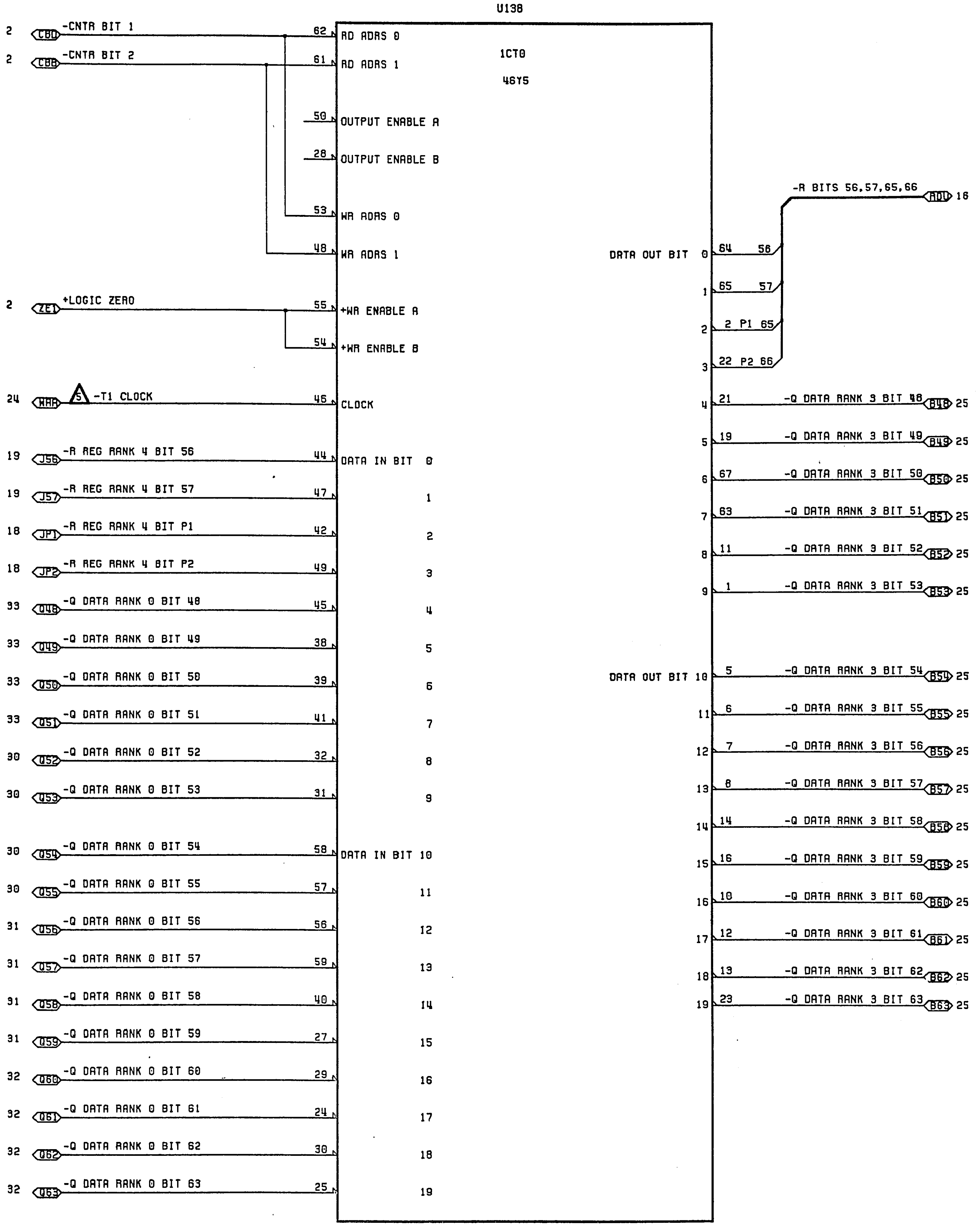
REV A

SHEET NO. 26

60462210

PAGE KA-28

Q BARREL RANKS 1-3 BITS 48-63,PAR
R BARREL RANKS 0-2 BITS 56,57,PAR BITS 1,2

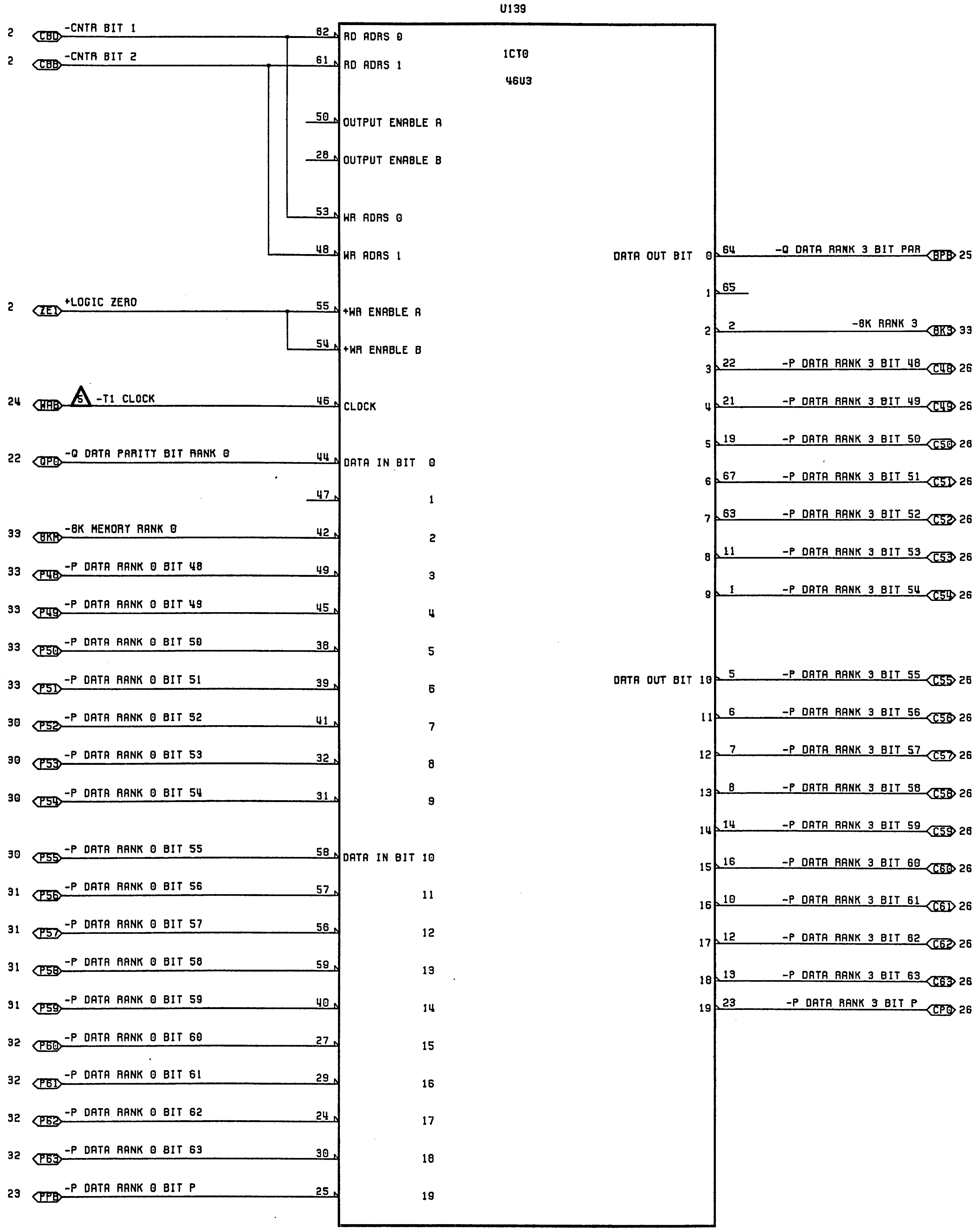


U138
1CT0
46Y5
2 CB0 -CNTR BIT 1 62 RD ADRS 0
2 CB8 -CNTR BIT 2 61 RD ADRS 1
50 OUTPUT ENABLE A
28 OUTPUT ENABLE B
53 WR ADRS 0
48 WR ADRS 1
2 ZE1 +LOGIC ZERO 55 +WR ENABLE A
54 +WR ENABLE B
24 HAA 5 -T1 CLOCK 46 CLOCK
19 J56 -R REG RANK 4 BIT 56 44 DATA IN BIT 0
19 J57 -R REG RANK 4 BIT 57 47 1
18 JP1 -R REG RANK 4 BIT P1 42 2
18 JP2 -R REG RANK 4 BIT P2 49 3
33 Q48 -Q DATA RANK 0 BIT 48 45 4
33 Q49 -Q DATA RANK 0 BIT 49 38 5
33 Q50 -Q DATA RANK 0 BIT 50 39 6
33 Q51 -Q DATA RANK 0 BIT 51 41 7
30 Q52 -Q DATA RANK 0 BIT 52 32 8
30 Q53 -Q DATA RANK 0 BIT 53 31 9
30 Q54 -Q DATA RANK 0 BIT 54 58 DATA IN BIT 10
30 Q55 -Q DATA RANK 0 BIT 55 57 11
31 Q56 -Q DATA RANK 0 BIT 56 56 12
31 Q57 -Q DATA RANK 0 BIT 57 59 13
31 Q58 -Q DATA RANK 0 BIT 58 40 14
31 Q59 -Q DATA RANK 0 BIT 59 27 15
32 Q60 -Q DATA RANK 0 BIT 60 29 16
32 Q61 -Q DATA RANK 0 BIT 61 24 17
32 Q62 -Q DATA RANK 0 BIT 62 30 18
32 Q63 -Q DATA RANK 0 BIT 63 25 19
-R BITS 56,57,65,66 AD1 16
DATA OUT BIT 0 64 56
1 65 57
2 2 P1 65
3 22 P2 66
4 21 -Q DATA RANK 3 BIT 48 B48 25
5 19 -Q DATA RANK 3 BIT 49 B49 25
6 67 -Q DATA RANK 3 BIT 50 B50 25
7 63 -Q DATA RANK 3 BIT 51 B51 25
8 11 -Q DATA RANK 3 BIT 52 B52 25
9 1 -Q DATA RANK 3 BIT 53 B53 25
DATA OUT BIT 10 5 -Q DATA RANK 3 BIT 54 B54 25
11 6 -Q DATA RANK 3 BIT 55 B55 25
12 7 -Q DATA RANK 3 BIT 56 B56 25
13 8 -Q DATA RANK 3 BIT 57 B57 25
14 14 -Q DATA RANK 3 BIT 58 B58 25
15 16 -Q DATA RANK 3 BIT 59 B59 25
16 10 -Q DATA RANK 3 BIT 60 B60 25
17 12 -Q DATA RANK 3 BIT 61 B61 25
18 13 -Q DATA RANK 3 BIT 62 B62 25
19 23 -Q DATA RANK 3 BIT 63 B63 25

5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA	REGISTER BOARD Q BARREL BITS 48-63 -R BARREL BITS 56,57,P1,P2 TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 27	60462210	PAGE KR-27	

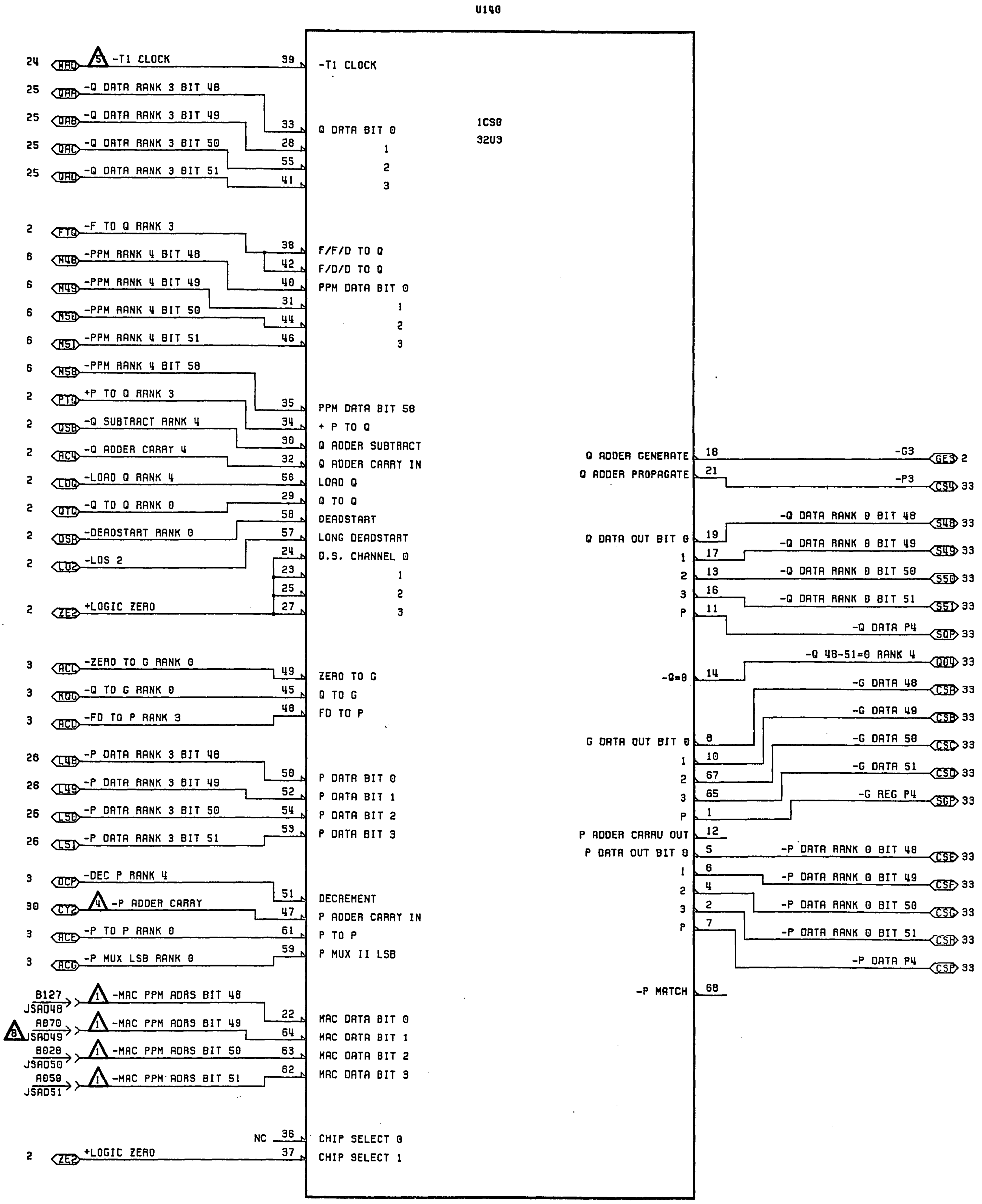
P BARREL RANKS 1-3 Q PAR BIT. RGTR


U139
1CT0
46U3
2 CB0 -CNTR BIT 1 62 RD ADRS 0
2 CBB -CNTR BIT 2 61 RD ADRS 1
50 OUTPUT ENABLE A
28 OUTPUT ENABLE B
53 WR ADRS 0
48 WR ADRS 1
2 ZE1 +LOGIC ZERO 55 +WR ENABLE A
54 +WR ENABLE B
24 WAB 5 -T1 CLOCK 46 CLOCK
22 QP0 -Q DATA PARITY BIT RANK 0 44 DATA IN BIT 0
47 1
33 8KM -8K MEMORY RANK 0 42 2
33 P48 -P DATA RANK 0 BIT 48 49 3
33 P49 -P DATA RANK 0 BIT 49 45 4
33 P50 -P DATA RANK 0 BIT 50 38 5
33 P51 -P DATA RANK 0 BIT 51 39 6
30 P52 -P DATA RANK 0 BIT 52 41 7
30 P53 -P DATA RANK 0 BIT 53 32 8
30 P54 -P DATA RANK 0 BIT 54 31 9
30 P55 -P DATA RANK 0 BIT 55 58 DATA IN BIT 10
31 P56 -P DATA RANK 0 BIT 56 57 11
31 P57 -P DATA RANK 0 BIT 57 56 12
31 P58 -P DATA RANK 0 BIT 58 59 13
31 P59 -P DATA RANK 0 BIT 59 40 14
32 P60 -P DATA RANK 0 BIT 60 27 15
32 P61 -P DATA RANK 0 BIT 61 29 16
32 P62 -P DATA RANK 0 BIT 62 24 17
32 P63 -P DATA RANK 0 BIT 63 30 18
23 PPB -P DATA RANK 0 BIT P 25 19
DATA OUT BIT 0 64 -Q DATA RANK 3 BIT PAR BPB 25
1 65
2 2 -8K RANK 3 8K3 33
3 22 -P DATA RANK 3 BIT 48 C48 26
4 21 -P DATA RANK 3 BIT 49 C49 26
5 19 -P DATA RANK 3 BIT 50 C50 26
6 67 -P DATA RANK 3 BIT 51 C51 26
7 63 -P DATA RANK 3 BIT 52 C52 26
8 11 -P DATA RANK 3 BIT 53 C53 26
9 1 -P DATA RANK 3 BIT 54 C54 26
DATA OUT BIT 10 5 -P DATA RANK 3 BIT 55 C55 26
11 6 -P DATA RANK 3 BIT 56 C56 26
12 7 -P DATA RANK 3 BIT 57 C57 26
13 8 -P DATA RANK 3 BIT 58 C58 26
14 14 -P DATA RANK 3 BIT 59 C59 26
15 16 -P DATA RANK 3 BIT 60 C60 26
16 10 -P DATA RANK 3 BIT 61 C61 26
17 12 -P DATA RANK 3 BIT 62 C62 26
18 13 -P DATA RANK 3 BIT 63 C63 26
19 23 -P DATA RANK 3 BIT P CP0 26

△5 CLOCK LINES NO LONGER THAN 12 INCHES

CONTROL DATA
REGISTER BOARD
P BARREL, Q PARITY BIT
TYPE 1KAH
N
B
DWG NO. 53575536
DATE 11/01/85
REV A
SHEET NO. 28
60462210
PAGE KA-28

Q,P SLOT BITS 48-51


U140
1CS0
32U3
24 WAD 5 -T1 CLOCK 39 -T1 CLOCK
25 QAA -Q DATA RANK 3 BIT 48 33 Q DATA BIT 0
25 QAB -Q DATA RANK 3 BIT 49 28 1
25 QAC -Q DATA RANK 3 BIT 50 55 2
25 QAD -Q DATA RANK 3 BIT 51 41 3
2 FTQ -F TO Q RANK 3 38 F/F/D TO Q
42 F/D/D TO Q
6 N48 -PPM RANK 4 BIT 48 40 PPM DATA BIT 0
6 N49 -PPM RANK 4 BIT 49 31 1
6 N50 -PPM RANK 4 BIT 50 44 2
6 N51 -PPM RANK 4 BIT 51 46 3
6 N58 -PPM RANK 4 BIT 58 35 PPM DATA BIT 58
2 PTQ +P TO Q RANK 3 34 + P TO Q
2 QSB -Q SUBTRACT RANK 4 30 Q ADDER SUBTRACT
2 AC4 -Q ADDER CARRY 4 32 Q ADDER CARRY IN
2 LDQ -LOAD Q RANK 4 56 LOAD Q
2 QTQ -Q TO Q RANK 0 29 Q TO Q
2 DSR -DEADSTART RANK 0 58 DEADSTART
57 LONG DEADSTART
2 LD2 -LDS 2 24 D.S. CHANNEL 0
23 1
25 2
2 ZE2 +LOGIC ZERO 27 3
3 ACC -ZERO TO G RANK 0 49 ZERO TO G
3 KQG -Q TO G RANK 0 45 Q TO G
3 ACD -FD TO P RANK 3 48 FD TO P
26 L48 -P DATA RANK 3 BIT 48 50 P DATA BIT 0
26 L49 -P DATA RANK 3 BIT 49 52 P DATA BIT 1
26 L50 -P DATA RANK 3 BIT 50 54 P DATA BIT 2
26 L51 -P DATA RANK 3 BIT 51 53 P DATA BIT 3
3 DCP -DEC P RANK 4 51 DECREMENT
30 CY2 4 -P ADDER CARRY 47 P ADDER CARRY IN
3 ACE -P TO P RANK 0 61 P TO P
3 ACG -P MUX LSB RANK 0 59 P MUX II LSB
B127 JSAD48 1 -MAC PPM ADRS BIT 48 22 MAC DATA BIT 0
8 A070 JSAD49 1 -MAC PPM ADRS BIT 49 64 MAC DATA BIT 1
B028 JSAD50 1 -MAC PPM ADRS BIT 50 63 MAC DATA BIT 2
A058 JSAD51 1 -MAC PPM ADRS BIT 51 62 MAC DATA BIT 3
NC 36 CHIP SELECT 0
2 ZE2 +LOGIC ZERO 37 CHIP SELECT 1
Q ADDER GENERATE 18 -G3 GE3 2
Q ADDER PROPAGATE 21 -P3 CS4 33
Q DATA OUT BIT 0 19 -Q DATA RANK 0 BIT 48 S48 33
1 17 -Q DATA RANK 0 BIT 49 S49 33
2 13 -Q DATA RANK 0 BIT 50 S50 33
3 16 -Q DATA RANK 0 BIT 51 S51 33
P 11 -Q DATA P4 SQP 33
-Q=0 14 -Q 48-51=0 RANK 4 Q04 33
G DATA OUT BIT 0 8 -G DATA 48 CSB 33
1 10 -G DATA 49 CSB 33
2 67 -G DATA 50 CSC 33
3 65 -G DATA 51 CSD 33
P 1 -G REG P4 SGP 33
P ADDER CARRU OUT 12
P DATA OUT BIT 0 5 -P DATA RANK 0 BIT 48 CSE 33
1 6 -P DATA RANK 0 BIT 49 CSF 33
2 4 -P DATA RANK 0 BIT 50 CSG 33
3 2 -P DATA RANK 0 BIT 51 CSH 33
P 7 -P DATA P4 CSP 33
-P MATCH 68

1 NOT TERMINATED

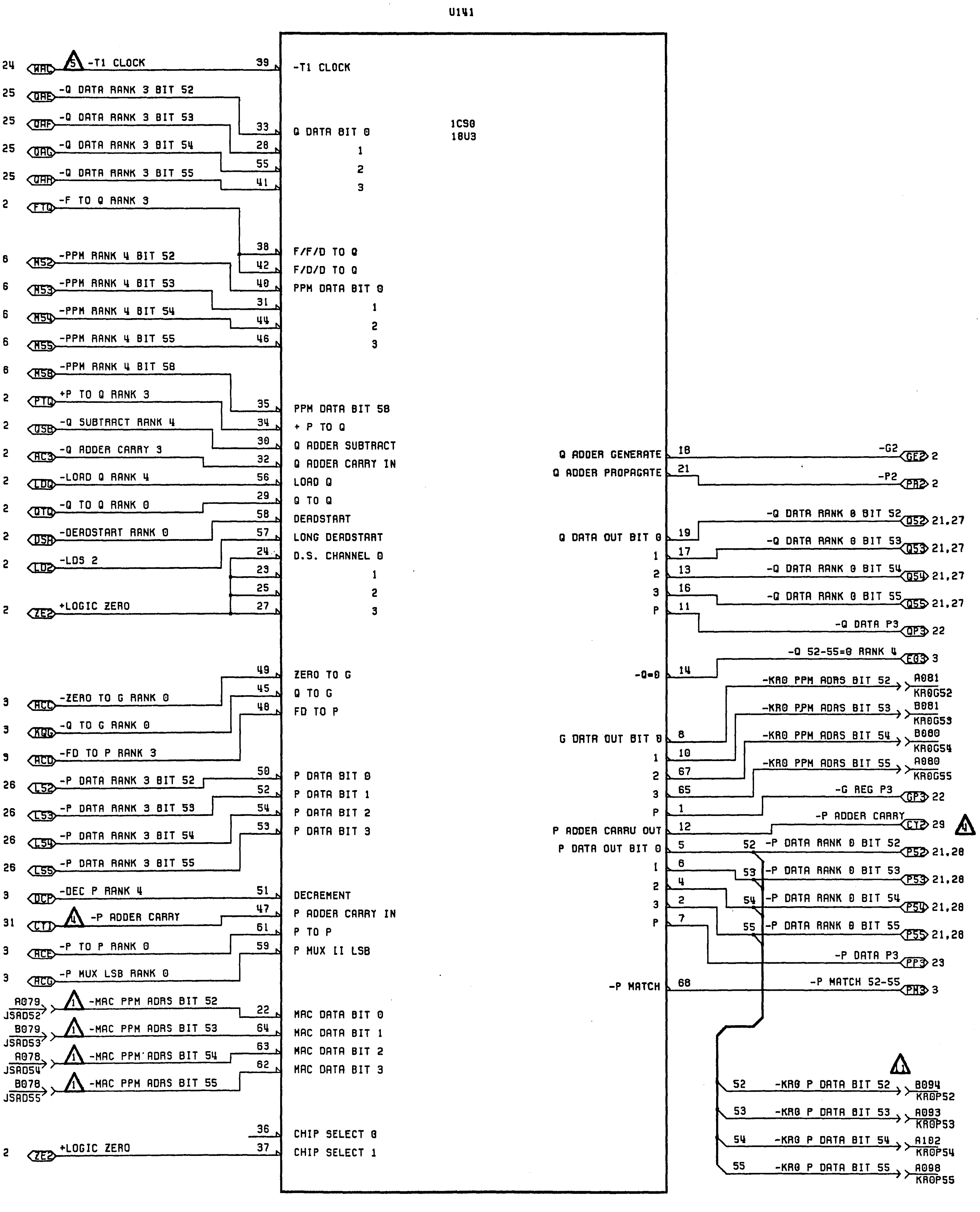
4 SHORT (NO LONGER THAN 3 INCHES)

5 CLOCK LINES NO LONGER THAN 12 INCHES

8 MAKE SURE THIS PIN
IS NO LONGER CONNECTED
AS A +5 VOLT SOURCE

CONTROL DATA	REGISTER BOARD Q,P SLOT BITS 48-51 TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 29	60462210	PAGE KR-28	

Q,P SLOT BITS 52-55 .



U141
1CS0
18U3
24 WAC 5 -T1 CLOCK 39 -T1 CLOCK
25 QAE -Q DATA RANK 3 BIT 52
25 QAF -Q DATA RANK 3 BIT 53 33 Q DATA BIT 0
25 QAG -Q DATA RANK 3 BIT 54 28 1
55 2
25 QAH -Q DATA RANK 3 BIT 55 41 3
2 FTQ -F TO Q RANK 3
38 F/F/D TO Q
6 N52 -PPM RANK 4 BIT 52 42 F/D/D TO Q
6 N53 -PPM RANK 4 BIT 53 40 PPM DATA BIT 0
31 1
6 N54 -PPM RANK 4 BIT 54 44 2
6 N55 -PPM RANK 4 BIT 55 46 3
6 N58 -PPM RANK 4 BIT 58
2 PTQ +P TO Q RANK 3 35 PPM DATA BIT 58
2 QSB -Q SUBTRACT RANK 4 34 + P TO Q
30 Q ADDER SUBTRACT
2 AC3 -Q ADDER CARRY 3 32 Q ADDER CARRY IN
2 LDQ -LOAD Q RANK 4 56 LOAD Q
29 Q TO Q
2 QTQ -Q TO Q RANK 0 58 DEADSTART
2 DSR -DEADSTART RANK 0 57 LONG DEADSTART
2 LD2 -LDS 2 24 D.S. CHANNEL 0
23 1
25 2
2 ZE2 +LOGIC ZERO 27 3
49 ZERO TO G
3 ACC -ZERO TO G RANK 0 45 Q TO G
3 KQG -Q TO G RANK 0 48 FD TO P
3 ACD -FD TO P RANK 3
26 L52 -P DATA RANK 3 BIT 52 50 P DATA BIT 0
52 P DATA BIT 1
26 L53 -P DATA RANK 3 BIT 53 54 P DATA BIT 2
26 L54 -P DATA RANK 3 BIT 54 53 P DATA BIT 3
26 L55 -P DATA RANK 3 BIT 55
3 DCP -DEC P RANK 4 51 DECREMENT
31 CT1 4 -P ADDER CARRY 47 P ADDER CARRY IN
61 P TO P
3 ACE -P TO P RANK 0 59 P MUX II LSB
3 ACG -P MUX LSB RANK 0
A079 JSAD52 1 -MAC PPM ADRS BIT 52 22 MAC DATA BIT 0
B079 JSAD53 1 -MAC PPM ADRS BIT 53 64 MAC DATA BIT 1
A078 JSAD54 1 -MAC PPM ADRS BIT 54 63 MAC DATA BIT 2
B078 JSAD55 1 -MAC PPM ADRS BIT 55 62 MAC DATA BIT 3
36 CHIP SELECT 0
2 ZE2 +LOGIC ZERO 37 CHIP SELECT 1
Q ADDER GENERATE 18 -G2 GE2 2
Q ADDER PROPAGATE 21 -P2 PA2 2
Q DATA OUT BIT 0 19 -Q DATA RANK 0 BIT 52 Q52 21,27
1 17 -Q DATA RANK 0 BIT 53 Q53 21,27
2 13 -Q DATA RANK 0 BIT 54 Q54 21,27
3 16 -Q DATA RANK 0 BIT 55 Q55 21,27
P 11 -Q DATA P3 QP3 22
-Q=0 14 -Q 52-55=0 RANK 4 E03 3
-KR0 PPM ADRS BIT 52 A081 KR0G52
-KR0 PPM ADRS BIT 53 B081 KR0G53
G DATA OUT BIT 0 8 -KR0 PPM ADRS BIT 54 B080 KR0G54
1 10
2 67 -KR0 PPM ADRS BIT 55 A080 KR0G55
3 65 -G REG P3 GP3 22
P 1 -P ADDER CARRY CY2 29 4
P ADDER CARRY OUT 12
P DATA OUT BIT 0 5 52 -P DATA RANK 0 BIT 52 P52 21,28
1 6 53 -P DATA RANK 0 BIT 53 P53 21,28
2 4 54 -P DATA RANK 0 BIT 54 P54 21,28
3 2
P 7 55 -P DATA RANK 0 BIT 55 P55 21,28
-P DATA P3 PP3 23
-P MATCH 68 -P MATCH 52-55 PM3 3
11
52 -KR0 P DATA BIT 52 B094 KR0P52
53 -KR0 P DATA BIT 53 A093 KR0P53
54 -KR0 P DATA BIT 54 A102 KR0P54
55 -KR0 P DATA BIT 55 A098 KR0P55

1 NOT TERMINATED

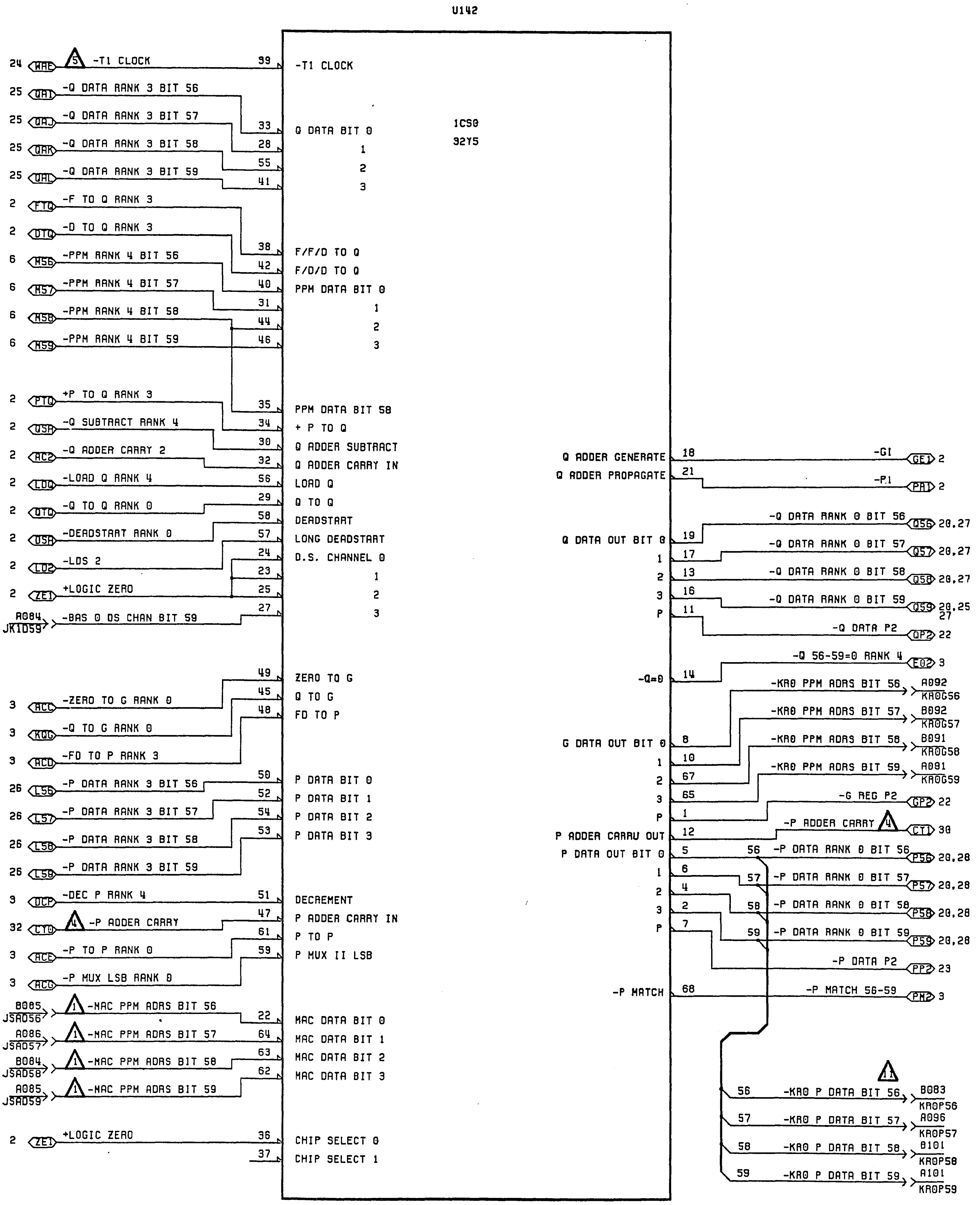
4 SHORT (NO LONGER THAN 3 INCHES)

5 CLOCK LINES NO LONGER THAN 12 INCHES

11 EVERY EFFORT SHOULD BE MADE TO MAKE THESE OUTPUTS 18 INCHES OR LESS

CONTROL DATA	REGISTER BOARD Q,P SLOT BITS 52-55 TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
		SHEET NO. 38	60462210	PAGE KR-38	

Q, P SLOT BITS 56-59


U142
1CS0
32Y5
24 WAE 5 -T1 CLOCK 39 -T1 CLOCK
25 QAI -Q DATA RANK 3 BIT 56
25 QAJ -Q DATA RANK 3 BIT 57
25 QAK -Q DATA RANK 3 BIT 58
25 QAL -Q DATA RANK 3 BIT 59
33 28 55 41
Q DATA BIT 0
1
2
3
2 FTQ -F TO Q RANK 3
2 DTQ -D TO Q RANK 3
6 M56 -PPM RANK 4 BIT 56
6 M57 -PPM RANK 4 BIT 57
6 M58 -PPM RANK 4 BIT 58
6 M59 -PPM RANK 4 BIT 59
38 42 40 31 44 46
F/F/D TO Q
F/D/D TO Q
PPM DATA BIT 0
1
2
3
2 PTQ +P TO Q RANK 3
2 QSR -Q SUBTRACT RANK 4
2 AC2 -Q ADDER CARRY 2
2 LDQ -LOAD Q RANK 4
2 QTQ -Q TO Q RANK 0
2 DSR -DEADSTART RANK 0
2 LD2 -LDS 2
2 ZE1 +LOGIC ZERO
A084 JK1D59 -BAS 0 DS CHAN BIT 59
35 34 30 32 56 29 58 57 24 23 25 27
PPM DATA BIT 58
+ P TO Q
Q ADDER SUBTRACT
Q ADDER CARRY IN
LOAD Q
Q TO Q
DEADSTART
LONG DEADSTART
D.S. CHANNEL 0
1
2
3
49 45 48
ZERO TO G
Q TO G
FD TO P
3 ACC -ZERO TO G RANK 0
3 KQG -Q TO G RANK 0
3 ACD -FD TO P RANK 3
26 L56 -P DATA RANK 3 BIT 56
26 L57 -P DATA RANK 3 BIT 57
26 L58 -P DATA RANK 3 BIT 58
26 L59 -P DATA RANK 3 BIT 59
50 52 54 53
P DATA BIT 0
P DATA BIT 1
P DATA BIT 2
P DATA BIT 3
3 DCP -DEC P RANK 4
32 CTO 4 -P ADDER CARRY
3 ACE -P TO P RANK 0
3 ACG -P MUX LSB RANK 0
51 47 61 59
DECREMENT
P ADDER CARRY IN
P TO P
P MUX II LSB
B085 JSAD56 1 -MAC PPM ADRS BIT 56
A086 JSAD57 1 -MAC PPM ADRS BIT 57
B084 JSAD58 1 -MAC PPM ADRS BIT 58
A085 JSAD59 1 -MAC PPM ADRS BIT 59
22 64 63 62
MAC DATA BIT 0
MAC DATA BIT 1
MAC DATA BIT 2
MAC DATA BIT 3
2 ZE1 +LOGIC ZERO 36 37
CHIP SELECT 0
CHIP SELECT 1
Q ADDER GENERATE 18 -G1 GE1 2
Q ADDER PROPAGATE 21 -P1 PA1 2
Q DATA OUT BIT 0 19 -Q DATA RANK 0 BIT 56 Q56 20,27
1 17 -Q DATA RANK 0 BIT 57 Q57 20,27
2 13 -Q DATA RANK 0 BIT 58 Q58 20,27
3 16 -Q DATA RANK 0 BIT 59 Q59 20,25 27
P 11 -Q DATA P2 QP2 22
-Q=0 14 -Q 56-59=0 RANK 4 E02 3
-KA0 PPM ADRS BIT 56 A092 KA0G56
-KA0 PPM ADRS BIT 57 B092 KA0G57
G DATA OUT BIT 0 8 -KA0 PPM ADRS BIT 58 B091 KA0G58
1 10 -KA0 PPM ADRS BIT 59 A091 KA0G59
2 67
3 65 -G REG P2 GP2 22
P 1 -P ADDER CARRY 4 CT1 30
P ADDER CARRU OUT 12
P DATA OUT BIT 0 5 56 -P DATA RANK 0 BIT 56 P56 20,28
1 6 57 -P DATA RANK 0 BIT 57 P57 20,28
2 4 58 -P DATA RANK 0 BIT 58 P58 20,28
3 2 59 -P DATA RANK 0 BIT 59 P59 20,28
P 7 -P DATA P2 PP2 23
-P MATCH 68 -P MATCH 56-59 PM2 3
11
56 -KA0 P DATA BIT 56 B083 KA0P56
57 -KA0 P DATA BIT 57 A096 KA0P57
58 -KA0 P DATA BIT 58 B101 KA0P58
59 -KA0 P DATA BIT 59 A101 KA0P59

1 NOT TERMINATED

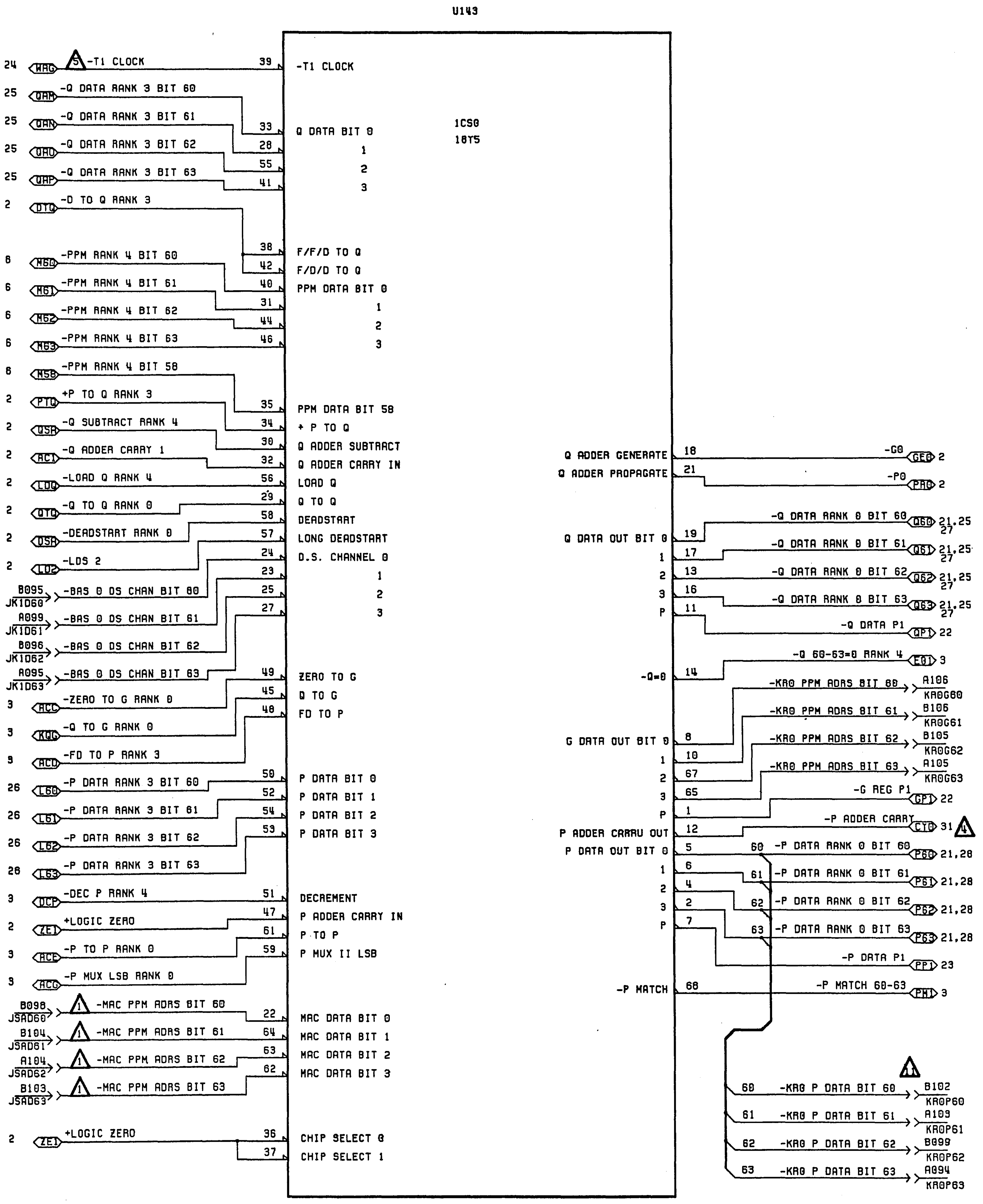
4 SHORT (NOT MORE THAN 3 INCHES)

5 CLOCK LINES NO LONGER THAN 12 INCHES

11 EVERY EFFORT SHOULD BE MADE TO MAKE THESE OUTPUTS 18 INCHES OR LESS

CONTROL DATA
REGISTER BOARD
Q, P SLOT BITS 56-59
TYPE 1KAH
B
DWG NO. 53575536
DATE 11/01/85
REV A
N SHEET NO. 31 60462210
PAGE KA-91

Q, P SLOT BITS 60-63


U143
1CS0
18Y5
24 WAG △5 -T1 CLOCK 39 -T1 CLOCK
25 QAM -Q DATA RANK 3 BIT 60 33 Q DATA BIT 0
25 QAN -Q DATA RANK 3 BIT 61 28 1
25 QAO -Q DATA RANK 3 BIT 62 55 2
25 QAP -Q DATA RANK 3 BIT 63 41 3
2 DTQ -D TO Q RANK 3 38 F/F/D TO Q
42 F/D/D TO Q
6 M60 -PPM RANK 4 BIT 60 40 PPM DATA BIT 0
6 M61 -PPM RANK 4 BIT 61 31 1
6 M62 -PPM RANK 4 BIT 62 44 2
6 M63 -PPM RANK 4 BIT 63 46 3
6 M58 -PPM RANK 4 BIT 58 35 PPM DATA BIT 58
2 PTQ +P TO Q RANK 3 34 + P TO Q
2 QSR -Q SUBTRACT RANK 4 30 Q ADDER SUBTRACT
2 ACI -Q ADDER CARRY 1 32 Q ADDER CARRY IN
2 LDQ -LOAD Q RANK 4 56 LOAD Q
2 QTQ -Q TO Q RANK 0 29 Q TO Q
2 DSR -DEADSTART RANK 0 58 DEADSTART
57 LONG DEADSTART
2 LD2 -LDS 2 24 D.S. CHANNEL 0
B095 JK1D60 -BAS 0 DS CHAN BIT 60 23 1
A099 JK1D61 -BAS 0 DS CHAN BIT 61 25 2
B096 JK1D62 -BAS 0 DS CHAN BIT 62 27 3
A095 JK1D63 -BAS 0 DS CHAN BIT 63
3 ACG -ZERO TO G RANK 0 49 ZERO TO G
3 KQG -Q TO G RANK 0 45 Q TO G
3 ACD -FD TO P RANK 3 48 FD TO P
26 L60 -P DATA RANK 3 BIT 60 50 P DATA BIT 0
26 L61 -P DATA RANK 3 BIT 61 52 P DATA BIT 1
26 L62 -P DATA RANK 3 BIT 62 54 P DATA BIT 2
26 L63 -P DATA RANK 3 BIT 63 53 P DATA BIT 3
3 DCP -DEC P RANK 4 51 DECREMENT
2 ZE1 +LOGIC ZERO 47 P ADDER CARRY IN
3 ACE -P TO P RANK 0 61 P TO P
3 ACG -P MUX LSB RANK 0 59 P MUX II LSB
B098 JSAD60 △1 -MAC PPM ADRS BIT 60 22 MAC DATA BIT 0
B104 JSAD61 △1 -MAC PPM ADRS BIT 61 64 MAC DATA BIT 1
A104 JSAD62 △1 -MAC PPM ADRS BIT 62 63 MAC DATA BIT 2
B103 JSAD63 △1 -MAC PPM ADRS BIT 63 62 MAC DATA BIT 3
2 ZE1 +LOGIC ZERO 36 CHIP SELECT 0
37 CHIP SELECT 1
Q ADDER GENERATE 18 -G0 GE0 2
Q ADDER PROPAGATE 21 -P0 PA0 2
Q DATA OUT BIT 0 19 -Q DATA RANK 0 BIT 60 Q60 21,25 27
1 17 -Q DATA RANK 0 BIT 61 Q61 21,25 27
2 13 -Q DATA RANK 0 BIT 62 Q62 21,25 27
3 16 -Q DATA RANK 0 BIT 63 Q63 21,25 27
P 11 -Q DATA P1 QP1 22
-Q=0 14 -Q 60-63=0 RANK 4 EQ1 3
-KR0 PPM ADRS BIT 60 A106 KR0G60
-KR0 PPM ADRS BIT 61 B106 KR0G61
G DATA OUT BIT 0 8 -KR0 PPM ADRS BIT 62 B105 KR0G62
1 10 -KR0 PPM ADRS BIT 63 A105 KR0G63
2 67 -G REG P1 GP1 22
3 65
P 1 -P ADDER CARRY CY0 31 △4
P ADDER CARRU OUT 12
P DATA OUT BIT 0 5 60 -P DATA RANK 0 BIT 60 P60 21,28
1 6 61 -P DATA RANK 0 BIT 61 P61 21,28
2 4 62 -P DATA RANK 0 BIT 62 P62 21,28
3 2 63 -P DATA RANK 0 BIT 63 P63 21,28
P 7 -P DATA P1 PP1 23
-P MATCH 68 -P MATCH 60-63 PM1 3
△11
60 -KR0 P DATA BIT 60 B102 KR0P60
61 -KR0 P DATA BIT 61 A103 KR0P61
62 -KR0 P DATA BIT 62 B099 KR0P62
63 -KR0 P DATA BIT 63 A094 KR0P63

△1 NOT TERMINATED

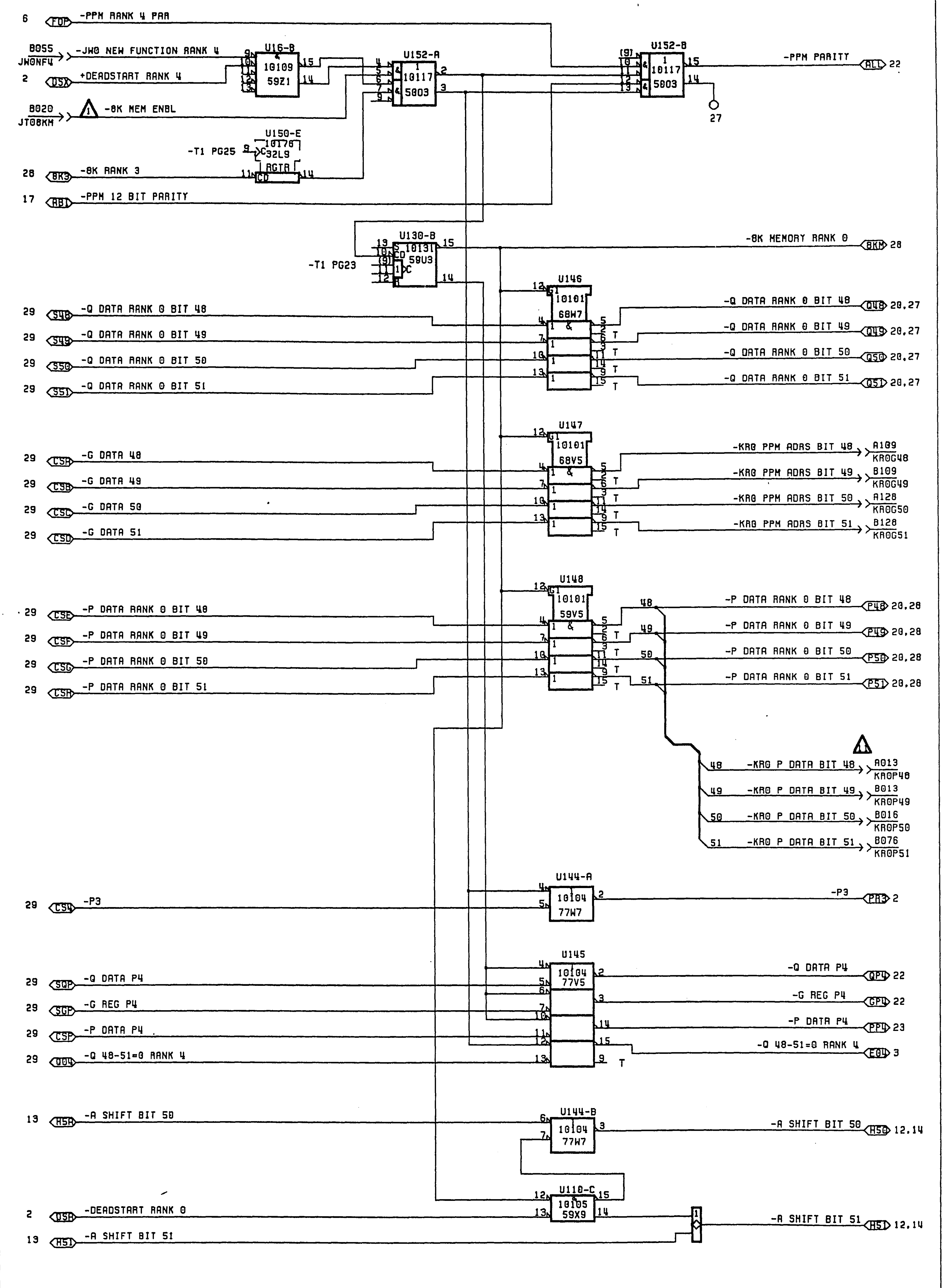
△4 SHORT (NOT MORE THAN 3 INCHES)

△5 CLOCK LINES NO LONGER THAN 12 INCHES

△11 EVERY EFFORT SHOULD BE MADE TO MAKE THESE OUTPUTS 18 INCHES OR LESS

CONTROL DATA	REGISTER BOARD Q. P SLOT BITS 60-63 TYPE 1KRH	B	DWG NO. 53575536	DATE 11/01/85	REV A
	N	SHEET NO. 32	60462210	PAGE KR-32	

4K MEM / 8K MEM SEL


6 FOP -PPM RANK 4 PAR
B055 JWONF4 -JWO NEW FUNCTION RANK 4
2 DSX +DEADSTART RANK 4
B020 JT08KM -8K MEM ENBL
U16-B 10109 59Z1
U152-A 10117 5803
U152-B 10117 5803
-PPM PARITY ALL 22
27
U150-E 10176 32L9 AGTA
-T1 PG25
28 8K3 -8K RANK 3
17 ABI -PPM 12 BIT PARITY
U130-B 10131 59U3
-T1 PG23
-8K MEMORY RANK 0 8KM 28
U146 10101 68W7
29 S48 -Q DATA RANK 0 BIT 48
29 S49 -Q DATA RANK 0 BIT 49
29 S50 -Q DATA RANK 0 BIT 50
29 S51 -Q DATA RANK 0 BIT 51
-Q DATA RANK 0 BIT 48 Q48 20,27
-Q DATA RANK 0 BIT 49 Q49 20,27
-Q DATA RANK 0 BIT 50 Q50 20,27
-Q DATA RANK 0 BIT 51 Q51 20,27
U147 10101 68V5
29 CSA -G DATA 48
29 CSB -G DATA 49
29 CSC -G DATA 50
29 CSD -G DATA 51
-KRG PPM ADRS BIT 48 A109 KRGG48
-KRG PPM ADRS BIT 49 B109 KRGG49
-KRG PPM ADRS BIT 50 A128 KRGG50
-KRG PPM ADRS BIT 51 B128 KRGG51
U148 10101 59V5
29 CSE -P DATA RANK 0 BIT 48
29 CSF -P DATA RANK 0 BIT 49
29 CSG -P DATA RANK 0 BIT 50
29 CSH -P DATA RANK 0 BIT 51
-P DATA RANK 0 BIT 48 P48 20,28
-P DATA RANK 0 BIT 49 P49 20,28
-P DATA RANK 0 BIT 50 P50 20,28
-P DATA RANK 0 BIT 51 P51 20,28
48 -KRG P DATA BIT 48 A013 KRGP48
49 -KRG P DATA BIT 49 B013 KRGP49
50 -KRG P DATA BIT 50 B016 KRGP50
51 -KRG P DATA BIT 51 B076 KRGP51
U144-A 10104 77W7
29 CS4 -P3
-P3 PA3 2
U145 10104 77V5
29 SQP -Q DATA P4
29 SGP -G REG P4
29 CSP -P DATA P4
29 QQ4 -Q 48-51=0 RANK 4
-Q DATA P4 QP4 22
-G REG P4 GP4 22
-P DATA P4 PP4 23
-Q 48-51=0 RANK 4 EQ4 3
U144-B 10104 77W7
13 ASA -A SHIFT BIT 50
-A SHIFT BIT 50 HS0 12,14
U110-C 10105 59X9
2 DSR -DEADSTART RANK 0
13 AS1 -A SHIFT BIT 51
-A SHIFT BIT 51 HS1 12,14

⚠1 NOT TERMINATED

⚠11 EVERY EFFORT SHOULD BE MADE TO MAKE THESE OUTPUTS 18 INCHES OR LESS

CONTROL DATA

REGISTER BOARD
4K MEMORY / 8K MEMORY SELECT
TYPE 1KRH

	DWG NO.	DATE	REV
B	53575536	01/30/86	A
SHEET NO. 33	60462210	PAGE KR-33	

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	05	+A = 1	27	23	+PPM PARITY BIT
02	05	+A = 0	28	22	-Q TO G RANK 0
03	18	+MUX CONTROL LOWER	29	22	-ZERO TO G RANK 0
04	18	+MUX CONTROL UPPER	30	22	-FD TO P RANK 4
05	20	-MAC SELECT BIT 2	31	06	-A ADDER CNTRL BIT 0
06	05	+A PARITY ERROR	32	02	+BAS COUNTER BIT 1
07	06	-A ADDER CODE BIT 2	33	20	-MAC SELECT BIT 1
08	06	-A ADDER CODE BIT 4	34	03	-Q TO P RANK 0
09	06	-A ADDER CODE BIT 1	35	03	+P MUX LSB RANK 0
10	12	-A BYPASS ENABLE	36	20	-MAC SELECT BIT 0
11	24	-T1 CLOCK	37		
12			38	03	-P TO P RANK 0
13	03	-BAS 0 SELECT	39	02	+BAS COUNTER BIT 2
14	03	+LOAD LDS ADDRESS	40	12	-A TO A RANK 0
15			41	17	-PPM ERROR
16			42	02	-Q TO Q RANK 0
17			43	03	-DEC P RANK 4
18	11	+JW0 Y TO A	44	02	-LOAD Q RANK 4
19	06	-A ADDER CNTRL BIT 2	45	06	-A ADDER CNTRL BIT 3
20			46	02	-Q SUBTRACT RANK 4
21	23	-A,R,P, OR Q ERROR	47	06	-A ADDER CODE BIT 3
22	02	+LDS 2	48	06	-A ADDER CODE BIT 0
23	24	+ADU MASTER CLEAR	49	06	-A ADDER CNTRL BIT 4
24			50	21	+STROBE MAC RGTR
25			51	03	+KR0 Q<3 RANK 4
26	11	+RIGHT SHIFT			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 [NOT USED]
TERM	,
UNUSED	B026,B053

CONTROL DATA	REGISTER BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1KAH	B	DWG NO. 53575536	DATE 11/01/85	REV A
	N	SHEET NO. 34	60462210	PAGE KA-94	

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1JXH CIO CHANNEL BOARD BAS I/F

REVISION HISTORY B/M 41652500			
DATE	REV	DESCRIPTION OF CHANGE	INIT
02/07/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS WITH	
		ECO 46883 INSTALLED.	LHJ
04/07/86	B	ECO #47444 ADDS LEVEL 3 REFERENCE	
		TO SHEETS 2 THRU 28	LHJ
07/07/86	C	ECO #47746 CORRECTS SHT 18.	LHJ
01/12/87	D	ECO #48330 PAGE 5	
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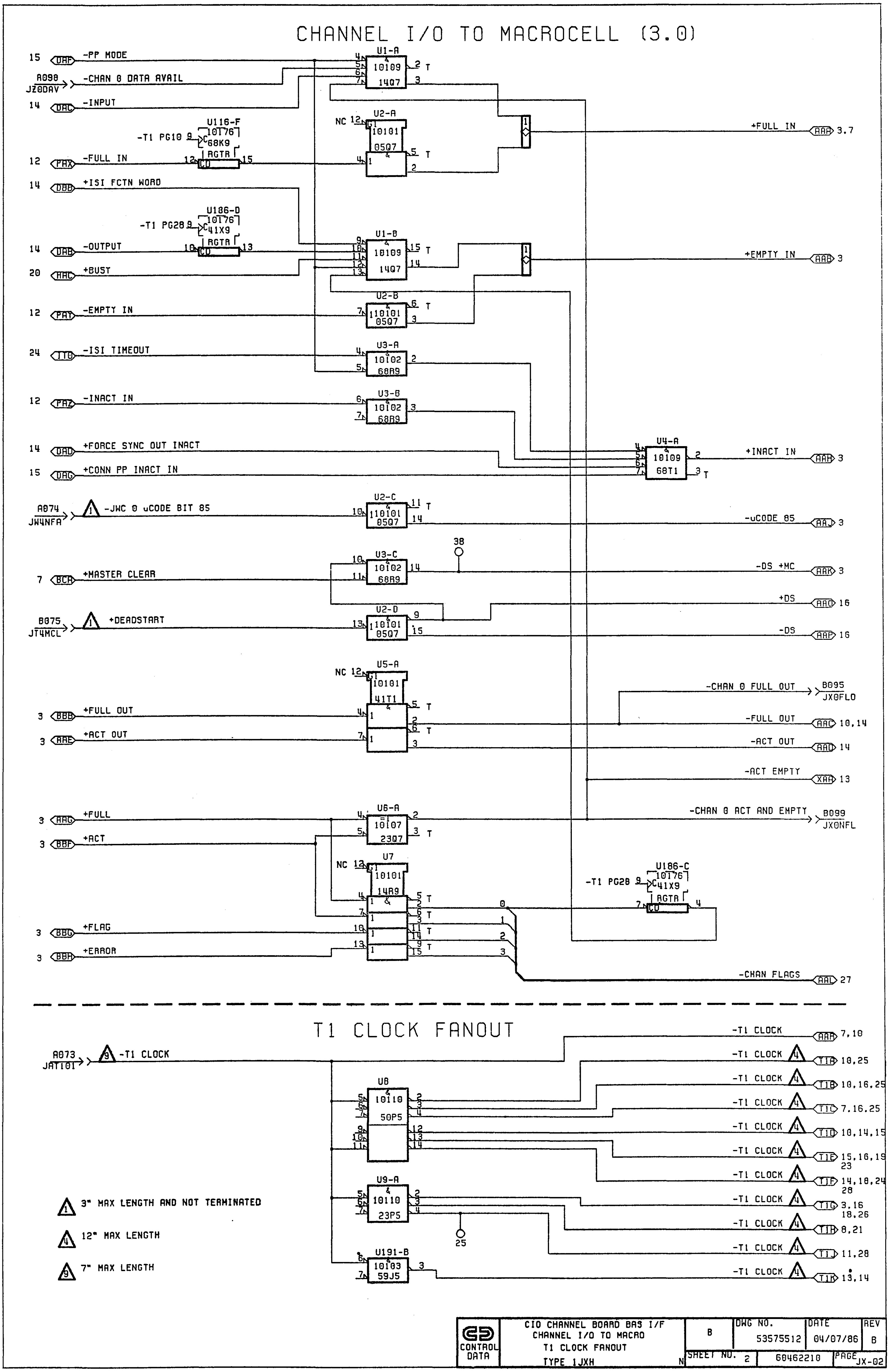
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D11,D14,D17,D20,D23
C11,C14,C17,C20,C23

DWN	L H JOHNSON	02/07/86
CHKD	L H JOHNSON	02/14/86
ENG	D A ZAHALAN	02/14/86
PUBS	D K BONDE	02/14/86
APP	D A ZAHALAN	02/14/86

CONTROL DATA	REVISION HISTORY	B	DWG NO. 53575512	DATE 01/12/87	REV D
	TYPE 1JXH	N	SHEET NO. 1	60462210	PAGE JX-01



1 3" MAX LENGTH AND NOT TERMINATED

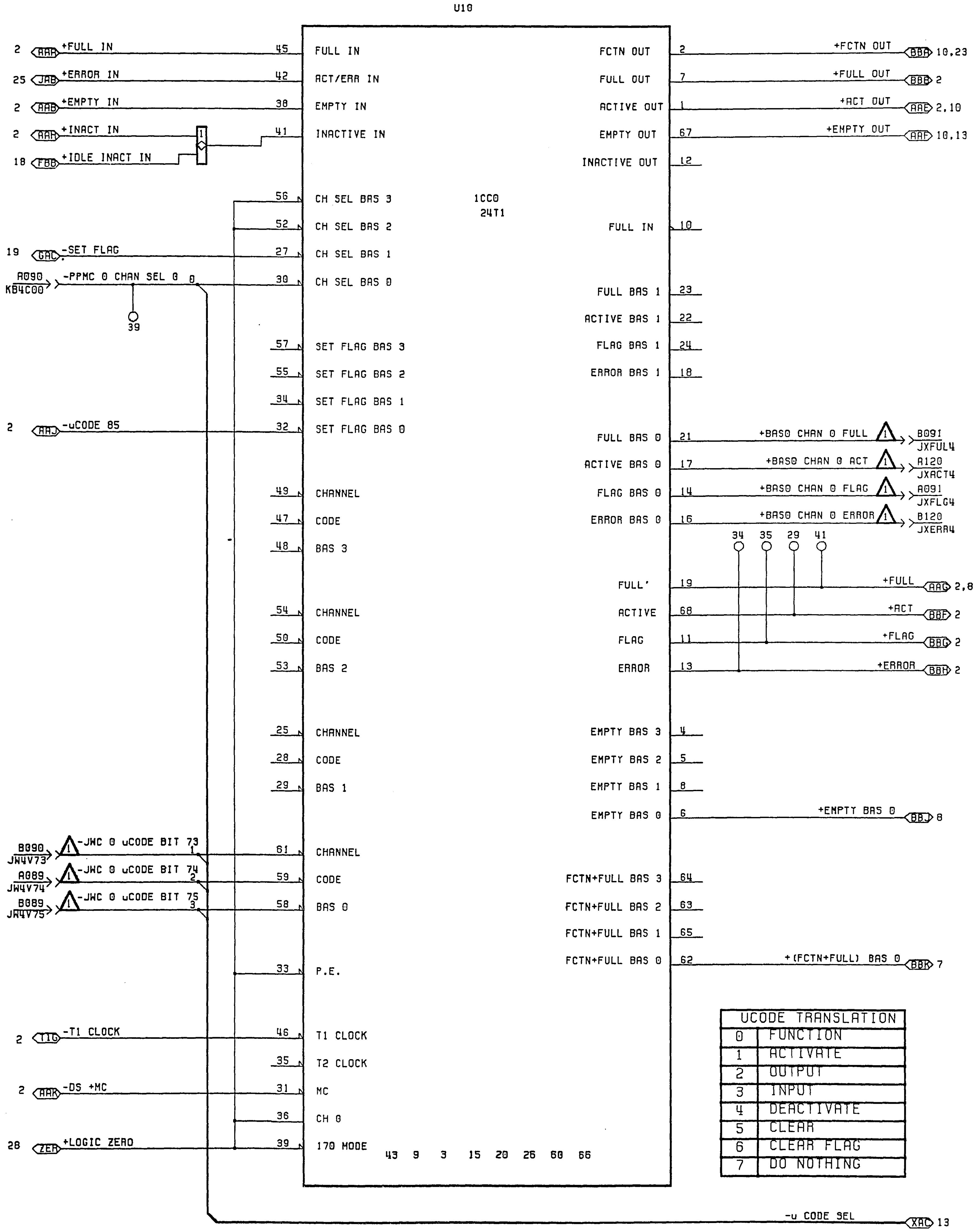
4 12" MAX LENGTH

9 7" MAX LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F CHANNEL I/O TO MACRO T1 CLOCK FANOUT TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV B
		N	SHEET NO. 2	60462210	PAGE JX-02

CHANNEL FLAGS AND MICROCODE TRANSLATOR

(3.0)

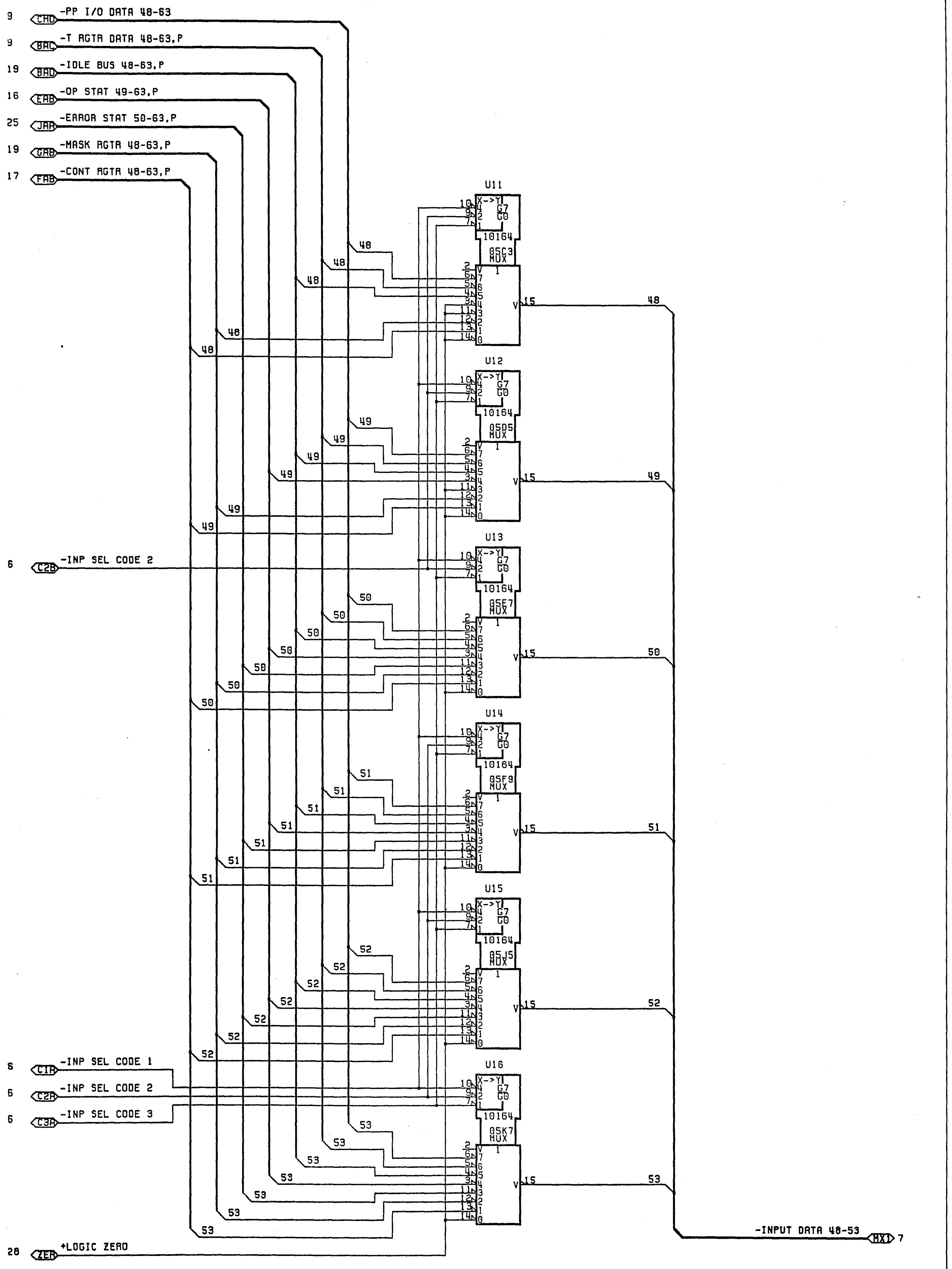

U10
1CC0
24T1
2 AAA +FULL IN 45 FULL IN
25 JAB +ERROR IN 42 ACT/ERR IN
2 AAB +EMPTY IN 38 EMPTY IN
2 AAH +INACT IN 41 INACTIVE IN
18 FBB +IDLE INACT IN
1
56 CH SEL BAS 3
52 CH SEL BAS 2
19 GAC -SET FLAG 27 CH SEL BAS 1
A090 K84C00 -PPMC 0 CHAN SEL 0 0 30 CH SEL BAS 0
39
57 SET FLAG BAS 3
55 SET FLAG BAS 2
34 SET FLAG BAS 1
2 AAJ -uCODE 85 32 SET FLAG BAS 0
49 CHANNEL
47 CODE
48 BAS 3
54 CHANNEL
50 CODE
53 BAS 2
25 CHANNEL
28 CODE
29 BAS 1
B090 JW4V73 -JWC 0 uCODE BIT 73 1 61 CHANNEL
A089 JW4V74 -JWC 0 uCODE BIT 74 2 59 CODE
B089 JW4V75 -JWC 0 uCODE BIT 75 3 58 BAS 0
33 P.E.
2 TIG -T1 CLOCK 46 T1 CLOCK
35 T2 CLOCK
2 AAK -DS +MC 31 MC
36 CH 0
28 ZER +LOGIC ZERO 39 170 MODE
43 9 3 15 20 26 60 66
FCTN OUT 2 +FCTN OUT BBA 10,23
FULL OUT 7 +FULL OUT BBB 2
ACTIVE OUT 1 +ACT OUT AAE 2,10
EMPTY OUT 67 +EMPTY OUT AAF 10,13
INACTIVE OUT 12
FULL IN 10
FULL BAS 1 23
ACTIVE BAS 1 22
FLAG BAS 1 24
ERROR BAS 1 18
FULL BAS 0 21 +BAS0 CHAN 0 FULL B091 JXFUL4
ACTIVE BAS 0 17 +BAS0 CHAN 0 ACT A120 JXACT4
FLAG BAS 0 14 +BAS0 CHAN 0 FLAG A091 JXFLG4
ERROR BAS 0 16 +BAS0 CHAN 0 ERROR B120 JXERR4
34 35 29 41
FULL' 19 +FULL AAG 2,8
ACTIVE 68 +ACT BBF 2
FLAG 11 +FLAG BBG 2
ERROR 13 +ERROR BBH 2
EMPTY BAS 3 4
EMPTY BAS 2 5
EMPTY BAS 1 8
EMPTY BAS 0 6 +EMPTY BAS 0 BBJ 8
FCTN+FULL BAS 3 64
FCTN+FULL BAS 2 63
FCTN+FULL BAS 1 65
FCTN+FULL BAS 0 62 +(FCTN+FULL) BAS 0 BBK 7
-u CODE SEL XAC 13

UCODE TRANSLATION	
0	FUNCTION
1	ACTIVATE
2	OUTPUT
3	INPUT
4	DEACTIVATE
5	CLEAR
6	CLEAR FLAG
7	DO NOTHING

⚠ 3" MAX LENGTH AND NOT TERMINATED

CONTROL DATA	CIO CHANNEL BOARD BAS I/F MACROCELL TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
		SHEET NO. 3	60462210	PAGE JX-03	

INPUT DATA MUX BITS 48-53 (3.1)

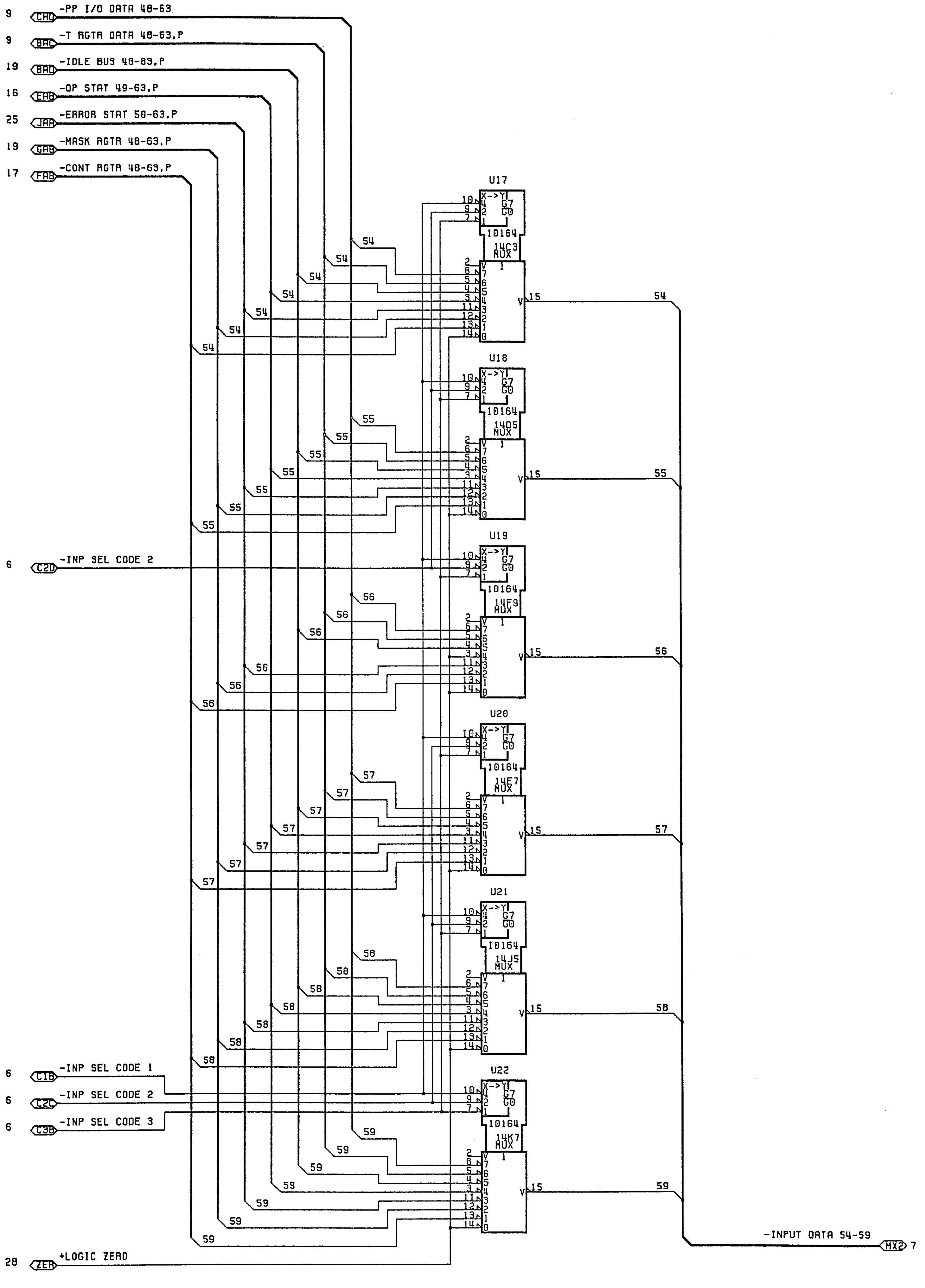


CONTROL DATA	CIO CHANNEL BOARD BAS I/F INPUT DATA MUX BITS 48-53 TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86
			SHEET NO. 4	60462210

REV A

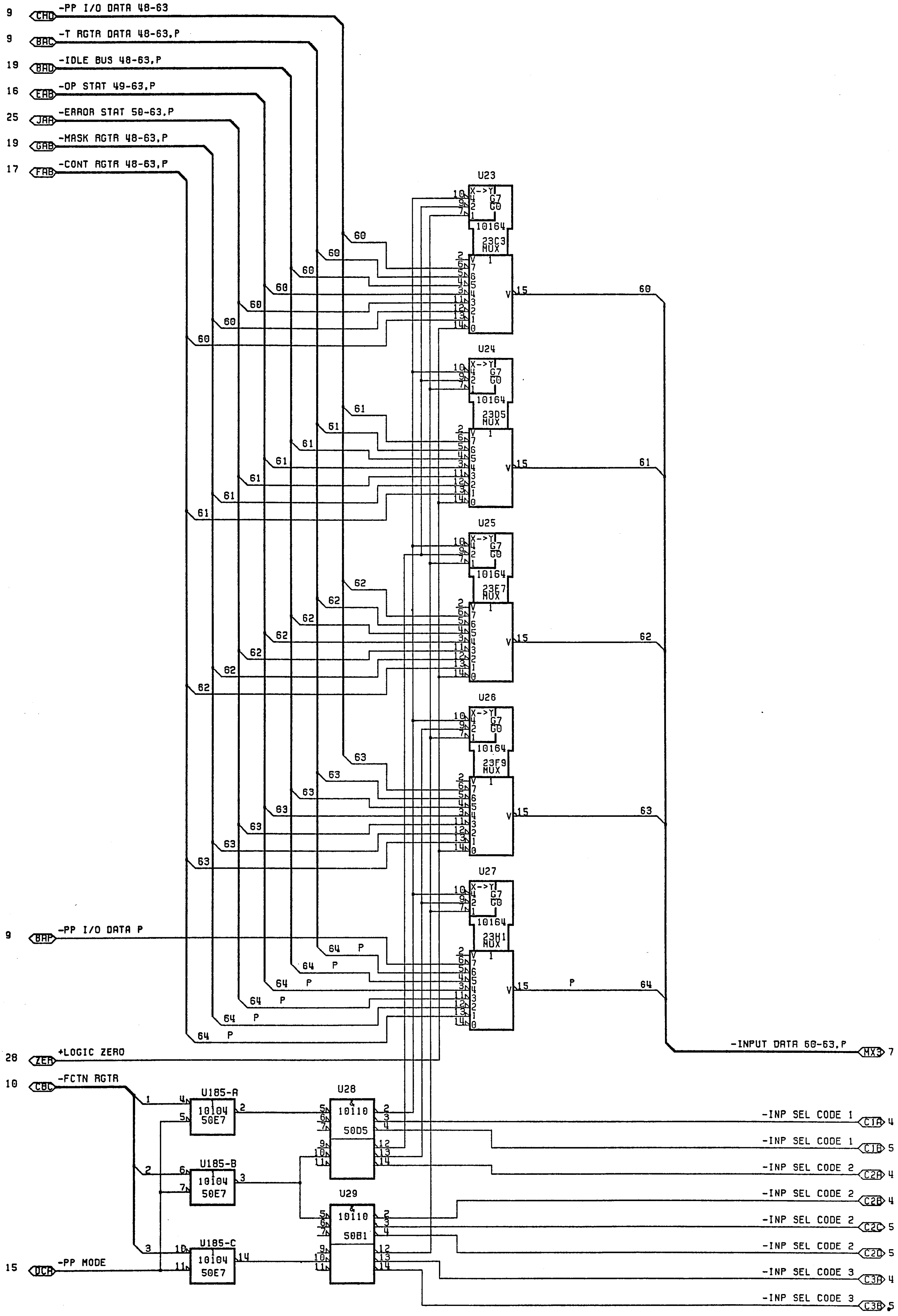
PAGE JX-04

INPUT DATA MUX BITS 54-59 (3.1)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F INPUT DATA MUX BITS 54-59 TYPE 1JXH	B	DWG NO. 53575512	DATE 01/12/87	REV D
		SHEET NO. 5	60462210	PAGE JX-05	

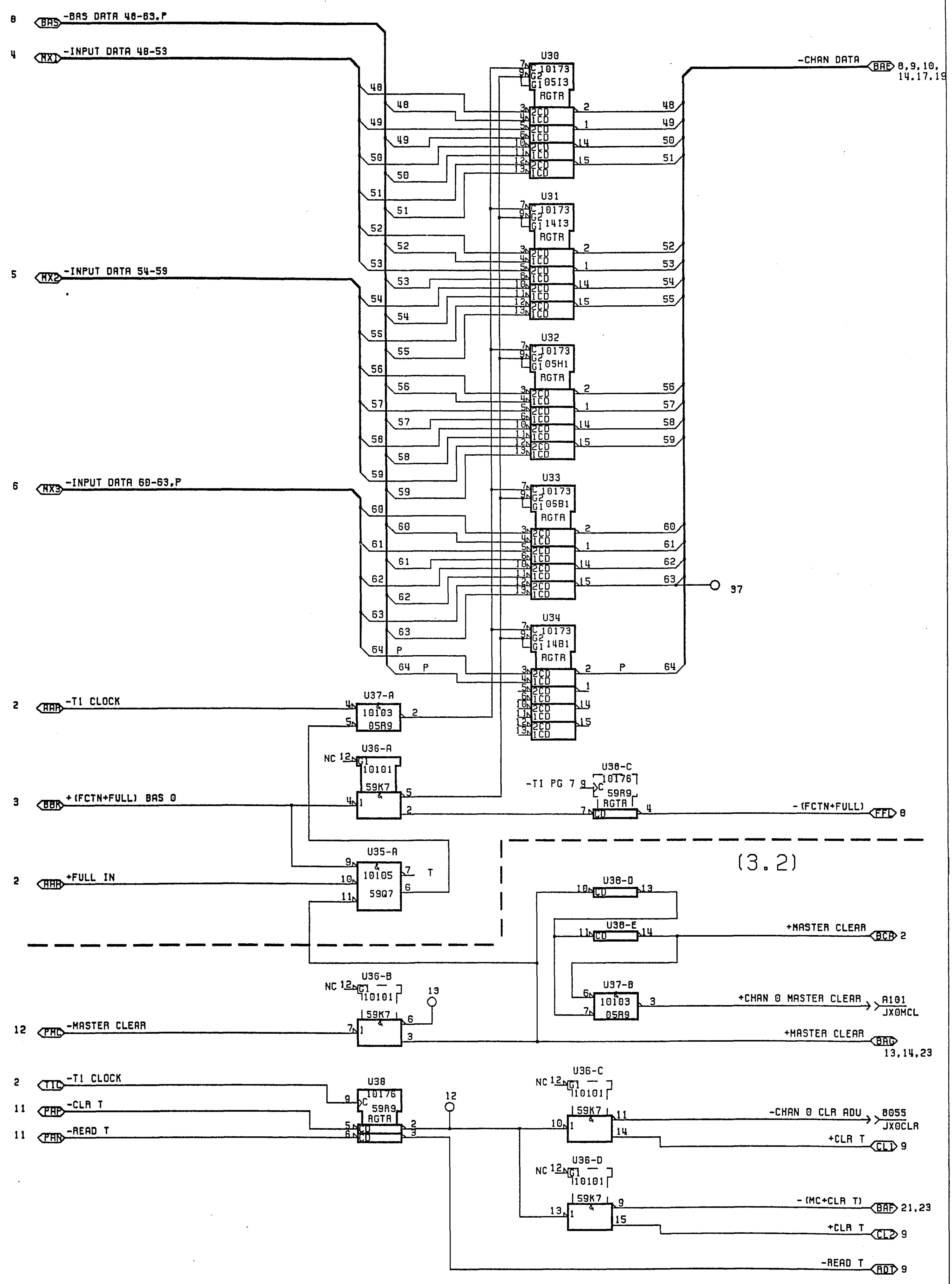
INPUT MUX BITS 60-63,PAR (3.1)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F INPUT MUX BIT 60-63,P TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV B
		N	SHEET NO. 6	60462210	PAGE JX-06

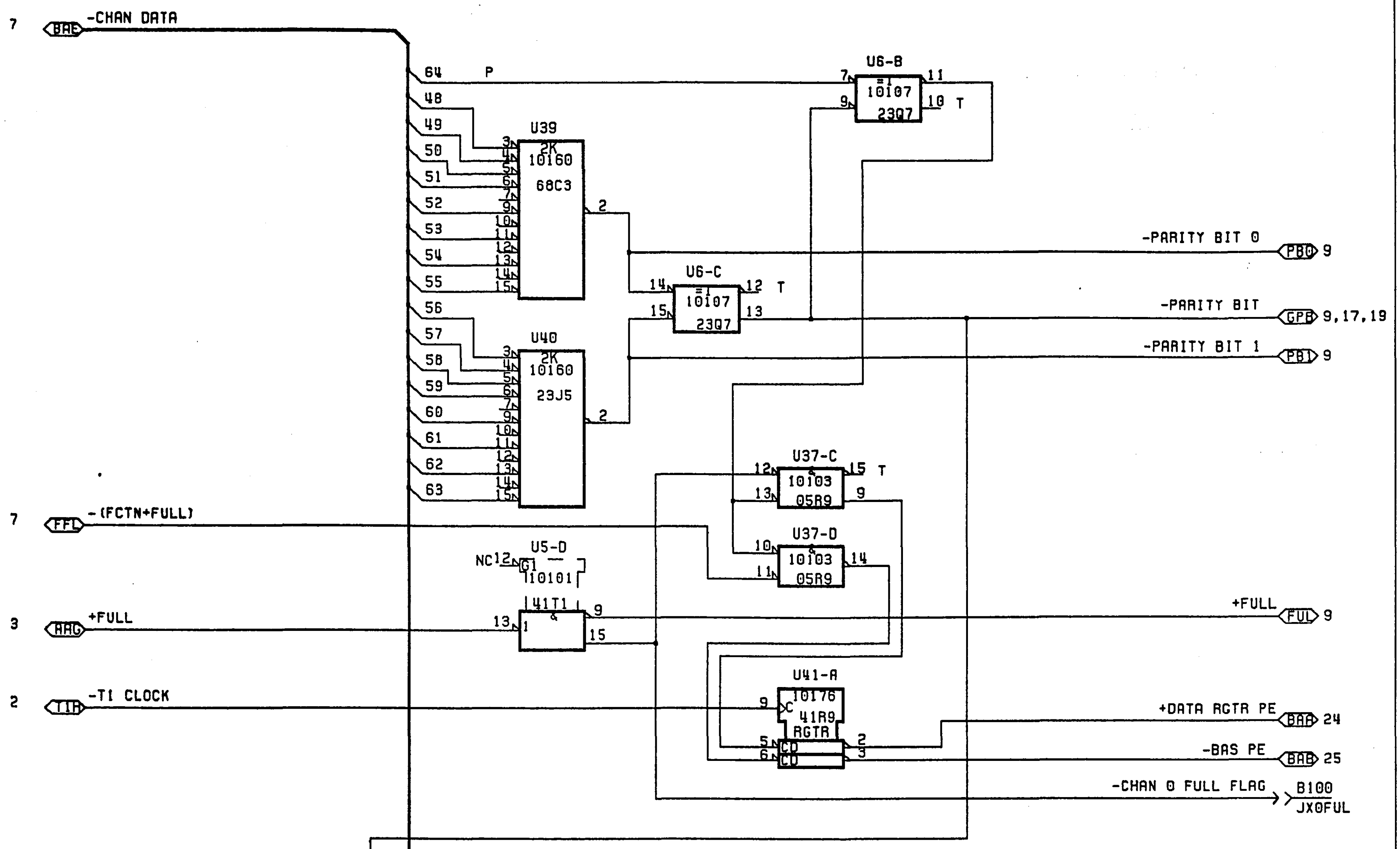
CHANNEL DATA REGISTER 48-63 & PAR

(3.1)

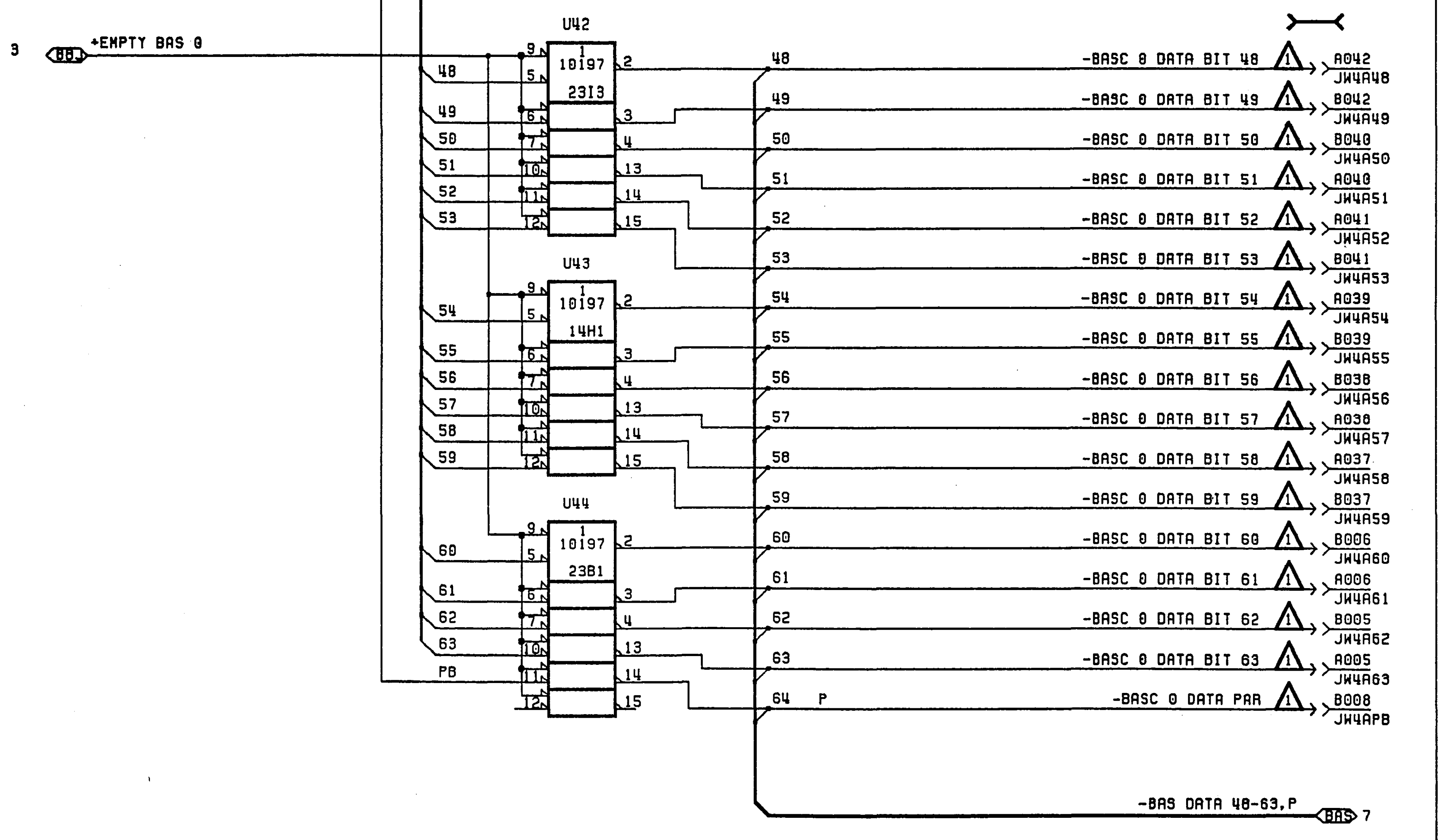


CONTROL DATA	CIO CHANNEL BOARD BAS I/F CHANNEL DATA REGISTER 48-63 & P TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
			SHEET NO. 7	60462210	PAGE JX-07

DATA RGTR PARITY CHECK AND GEN (3.1)



BAS DATA IN AND OUT (3.1)

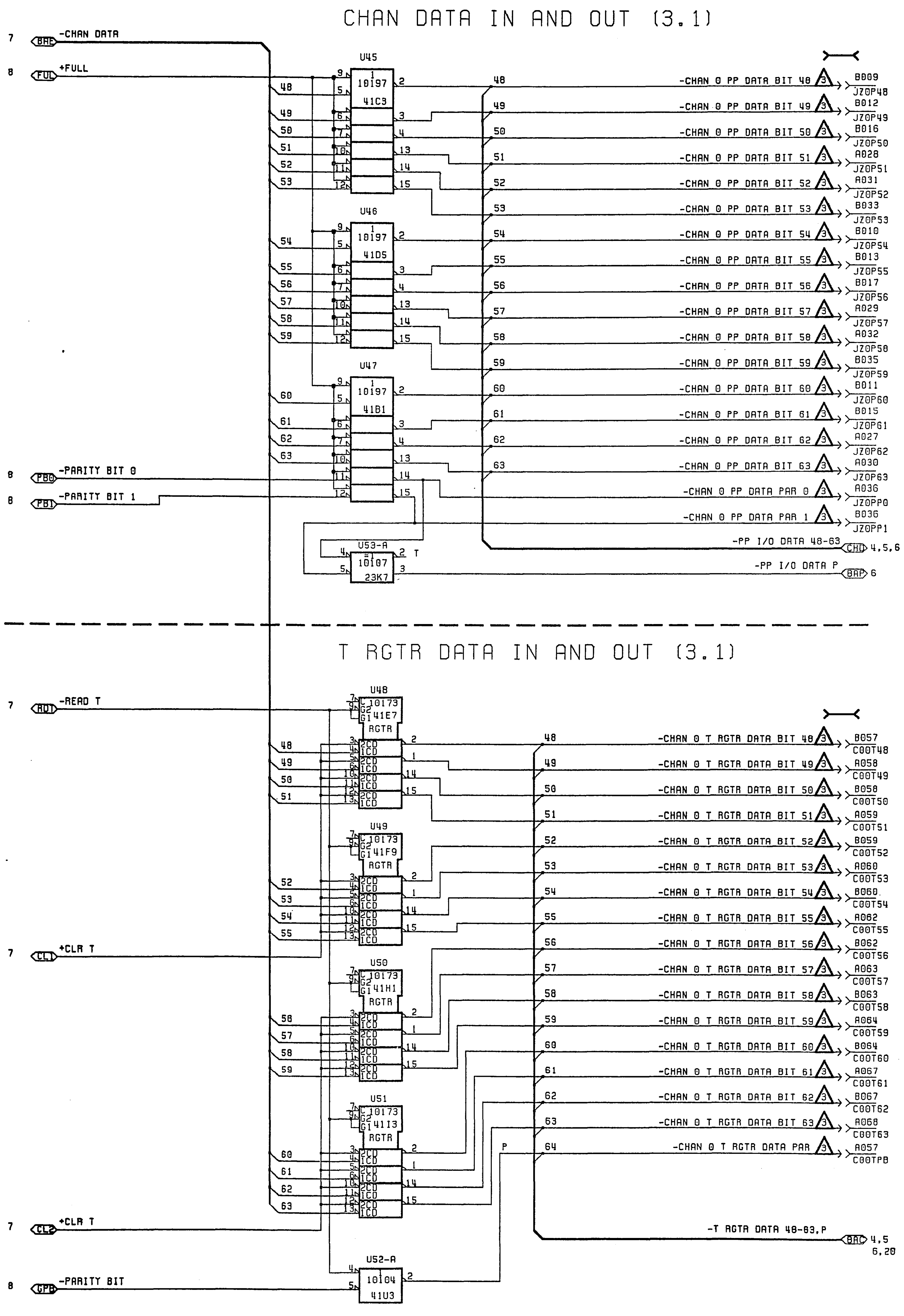

3 BBJ +EMPTY BAS 0
U42 10197 23I3
U43 10197 14H1
U44 10197 23B1
PB
-BASC 0 DATA BIT 48 A042 JW4A48
-BASC 0 DATA BIT 49 B042 JW4A49
-BASC 0 DATA BIT 50 B040 JW4A50
-BASC 0 DATA BIT 51 A040 JW4A51
-BASC 0 DATA BIT 52 A041 JW4A52
-BASC 0 DATA BIT 53 B041 JW4A53
-BASC 0 DATA BIT 54 A039 JW4A54
-BASC 0 DATA BIT 55 B039 JW4A55
-BASC 0 DATA BIT 56 B038 JW4A56
-BASC 0 DATA BIT 57 A038 JW4A57
-BASC 0 DATA BIT 58 A037 JW4A58
-BASC 0 DATA BIT 59 B037 JW4A59
-BASC 0 DATA BIT 60 B006 JW4A60
-BASC 0 DATA BIT 61 A006 JW4A61
-BASC 0 DATA BIT 62 B005 JW4A62
-BASC 0 DATA BIT 63 A005 JW4A63
64 P
-BASC 0 DATA PAR B008 JW4APB
-BAS DATA 48-63,P BAS 7

△ 4" MAX LENGTH AND NOT TERMINATED

CONTROL DATA

CIO CHANNEL BOARD BAS I/F
DATA RGTR PARITY CHECK AND GEN
BAS DATA IN AND OUT
TYPE 1JXH

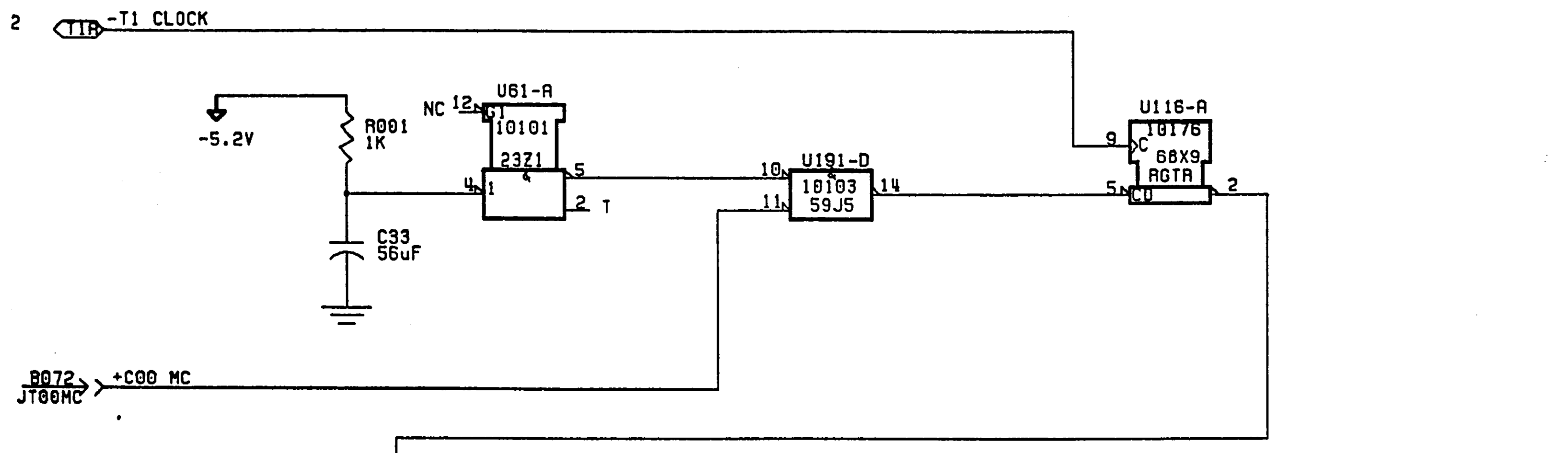
B
DWG NO. 53575512
DATE 04/07/86
REV A
SHEET NO. 8
60462210
PAGE JX-08


CHAN DATA IN AND OUT (3.1)
7 BAE -CHAN DATA
8 FUL +FULL
U45 10197 41C3
U46 10197 41D5
U47 10197 41B1
48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
-CHAN 0 PP DATA BIT 48 B009 JZ0P48
-CHAN 0 PP DATA BIT 49 B012 JZ0P49
-CHAN 0 PP DATA BIT 50 B016 JZ0P50
-CHAN 0 PP DATA BIT 51 A028 JZ0P51
-CHAN 0 PP DATA BIT 52 A031 JZ0P52
-CHAN 0 PP DATA BIT 53 B033 JZ0P53
-CHAN 0 PP DATA BIT 54 B010 JZ0P54
-CHAN 0 PP DATA BIT 55 B013 JZ0P55
-CHAN 0 PP DATA BIT 56 B017 JZ0P56
-CHAN 0 PP DATA BIT 57 A029 JZ0P57
-CHAN 0 PP DATA BIT 58 A032 JZ0P58
-CHAN 0 PP DATA BIT 59 B035 JZ0P59
-CHAN 0 PP DATA BIT 60 B011 JZ0P60
-CHAN 0 PP DATA BIT 61 B015 JZ0P61
-CHAN 0 PP DATA BIT 62 A027 JZ0P62
-CHAN 0 PP DATA BIT 63 A030 JZ0P63
-CHAN 0 PP DATA PAR 0 A036 JZ0PP0
-CHAN 0 PP DATA PAR 1 B036 JZ0PP1
8 PB0 -PARITY BIT 0
8 PB1 -PARITY BIT 1
U53-A =1 10107 23K7 T
-PP I/O DATA 48-63 CHD 4,5,6
-PP I/O DATA P BAP 6
T RGTR DATA IN AND OUT (3.1)
7 RDT -READ T
U48 10173 41E7 RGTR
U49 10173 41F9 RGTR
U50 10173 41H1 RGTR
U51 10173 41I3 RGTR
C G2 G1 2CD 1CD
-CHAN 0 T RGTR DATA BIT 48 B057 C00T48
-CHAN 0 T RGTR DATA BIT 49 A058 C00T49
-CHAN 0 T RGTR DATA BIT 50 B058 C00T50
-CHAN 0 T RGTR DATA BIT 51 A059 C00T51
-CHAN 0 T RGTR DATA BIT 52 B059 C00T52
-CHAN 0 T RGTR DATA BIT 53 A060 C00T53
-CHAN 0 T RGTR DATA BIT 54 B060 C00T54
-CHAN 0 T RGTR DATA BIT 55 A062 C00T55
-CHAN 0 T RGTR DATA BIT 56 B062 C00T56
-CHAN 0 T RGTR DATA BIT 57 A063 C00T57
-CHAN 0 T RGTR DATA BIT 58 B063 C00T58
-CHAN 0 T RGTR DATA BIT 59 A064 C00T59
-CHAN 0 T RGTR DATA BIT 60 B064 C00T60
-CHAN 0 T RGTR DATA BIT 61 A067 C00T61
-CHAN 0 T RGTR DATA BIT 62 B067 C00T62
-CHAN 0 T RGTR DATA BIT 63 A068 C00T63
-CHAN 0 T RGTR DATA PAR A057 C00TP8
P 64
7 CL1 +CLR T
7 CL2 +CLR T
-T RGTR DATA 48-63,P BAC 4,5 6,20
U52-A 10104 41U3
8 CPB -PARITY BIT

3 TERMINATE AT FARTHEST POINT FROM THE CONN PIN

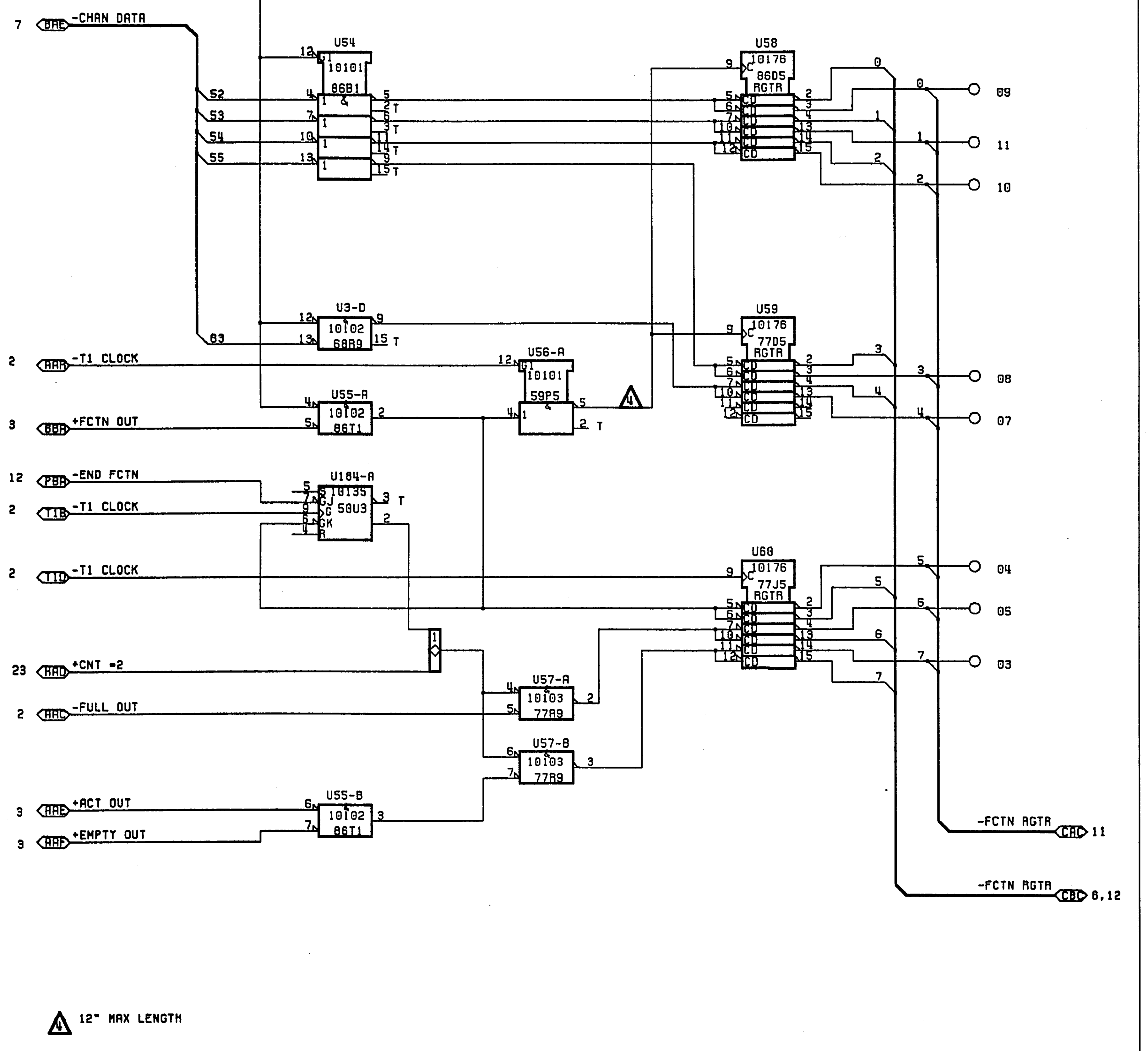
CONTROL DATA	CIO CHANNEL BOARD BAS I/F CHAN DATA IN AND OUT T RGTR DATA IN AND OUT TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
		N SHEET NO. 9	60462210	PAGE JX-09	

POWER ON MASTER CLEAR (3.2)



2 T1A -T1 CLOCK
-5.2V
R001 1K
C33 56uF
NC 12 U61-A 10101 23Z1 4 5 2 T
U191-D 10103 59J5 10 11 14
U116-A 10176 68X9 RGTR 9 C 5 CD 2
8072 JT00MC +C00 MC

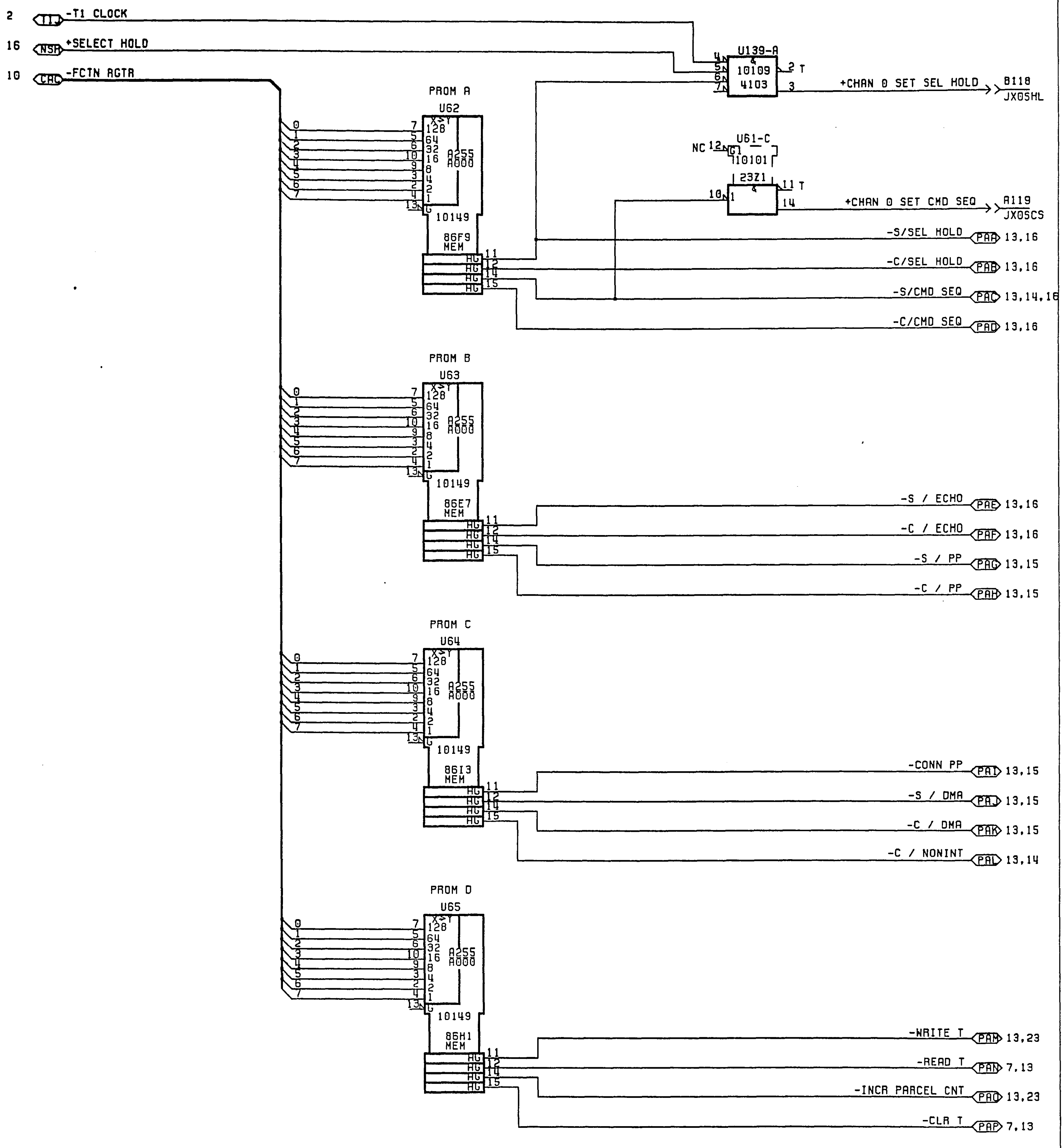
FUNCTION REGISTER (3.2)



△4 12" MAX LENGTH

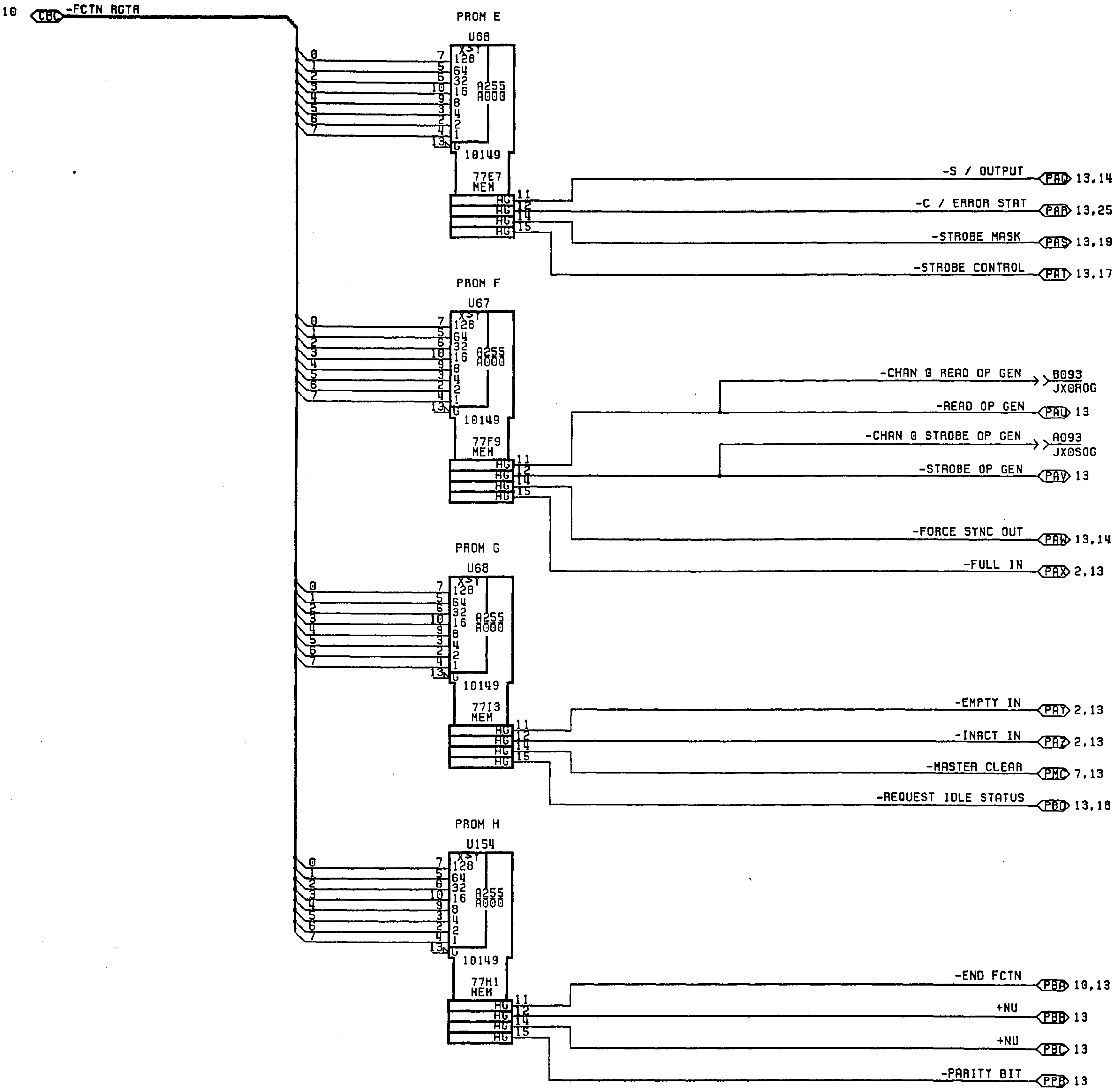
CONTROL DATA	CIO CHANNEL BOARD BAS I/F FUNCTION REGISTER POWER ON MASTER CLEAR TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
		SHEET NO. 10	60462210	PAGE JX-10	

FUNCTION DECODE PROMS A-D (3.2)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F FUNCTION DECODE PROMS A-D	B	DWG NO. 53575512	DATE 04/07/86	REV A
	TYPE 1JXH	N	SHEET NO. 11	60462210	PAGE JX-11

FUNCTION DECODE PROMS E-H (3.2(

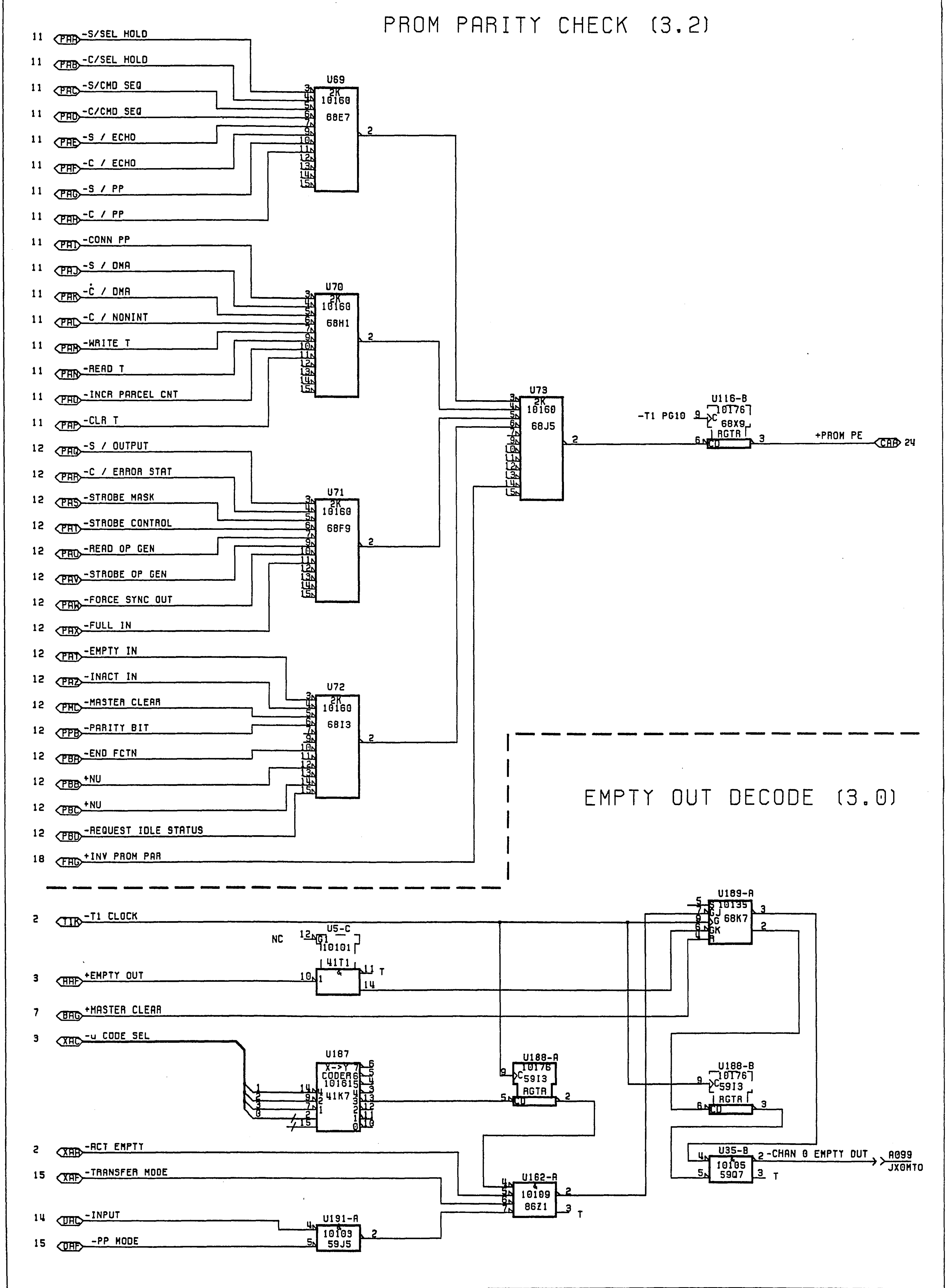


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FUNCTION DECODE PROMS E-H
TYPE 1JXH

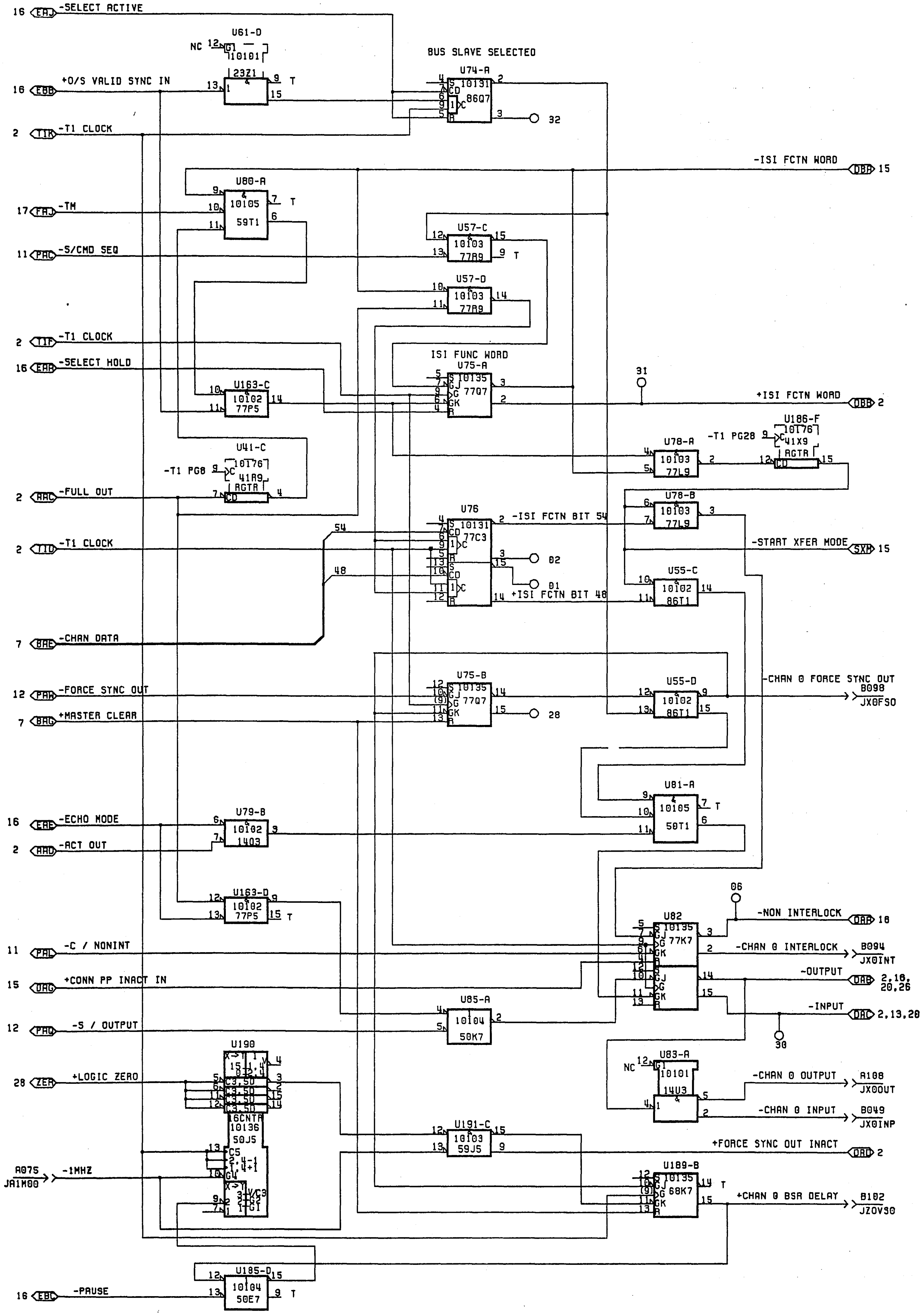
B

DWG NO. 53575512
DATE 04/07/86
REV A
SHEET NO. 12 60462210
PAGE JX-12



CONTROL DATA	CIO CHANNEL BOARD BAS I/F PROM PARITY CHECK EMPTY OUT DECODE TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
		N	SHEET NO. 13	60462210	PAGE JX-13

ADAPTER INTERLOCK/OUTPUT MODE REGISTERS (3.3)

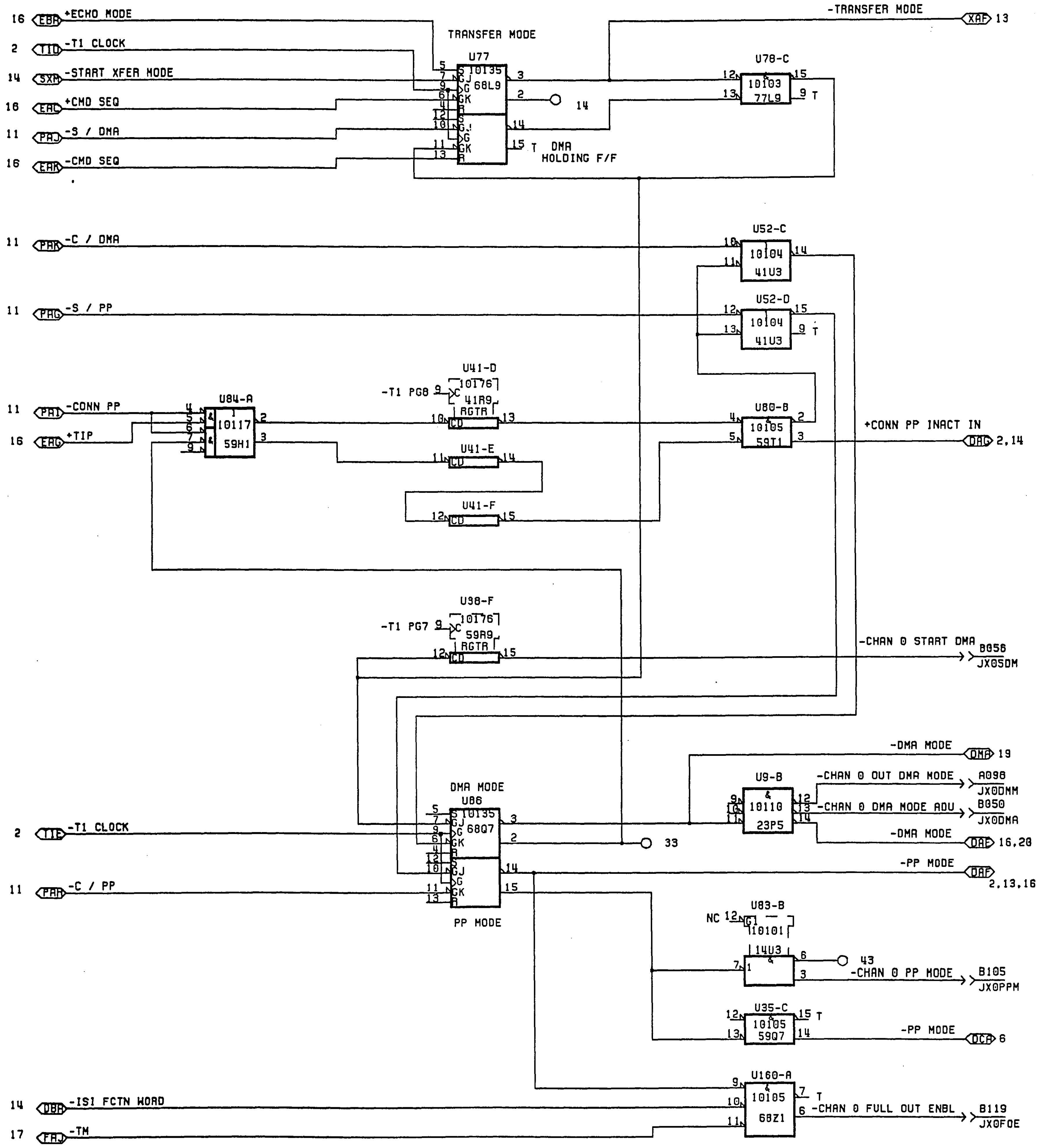


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
ADAPTER NONINTERLOCK/OUTPUT
MODE REGISTERS
TYPE 1JXH

B	DWG NO. 53575512	DATE 04/07/86	REV A
SHEET NO. 14	60462210	PAGE JX-14	

ADAPTER PP/DMA MODE REGISTERS (3.3)

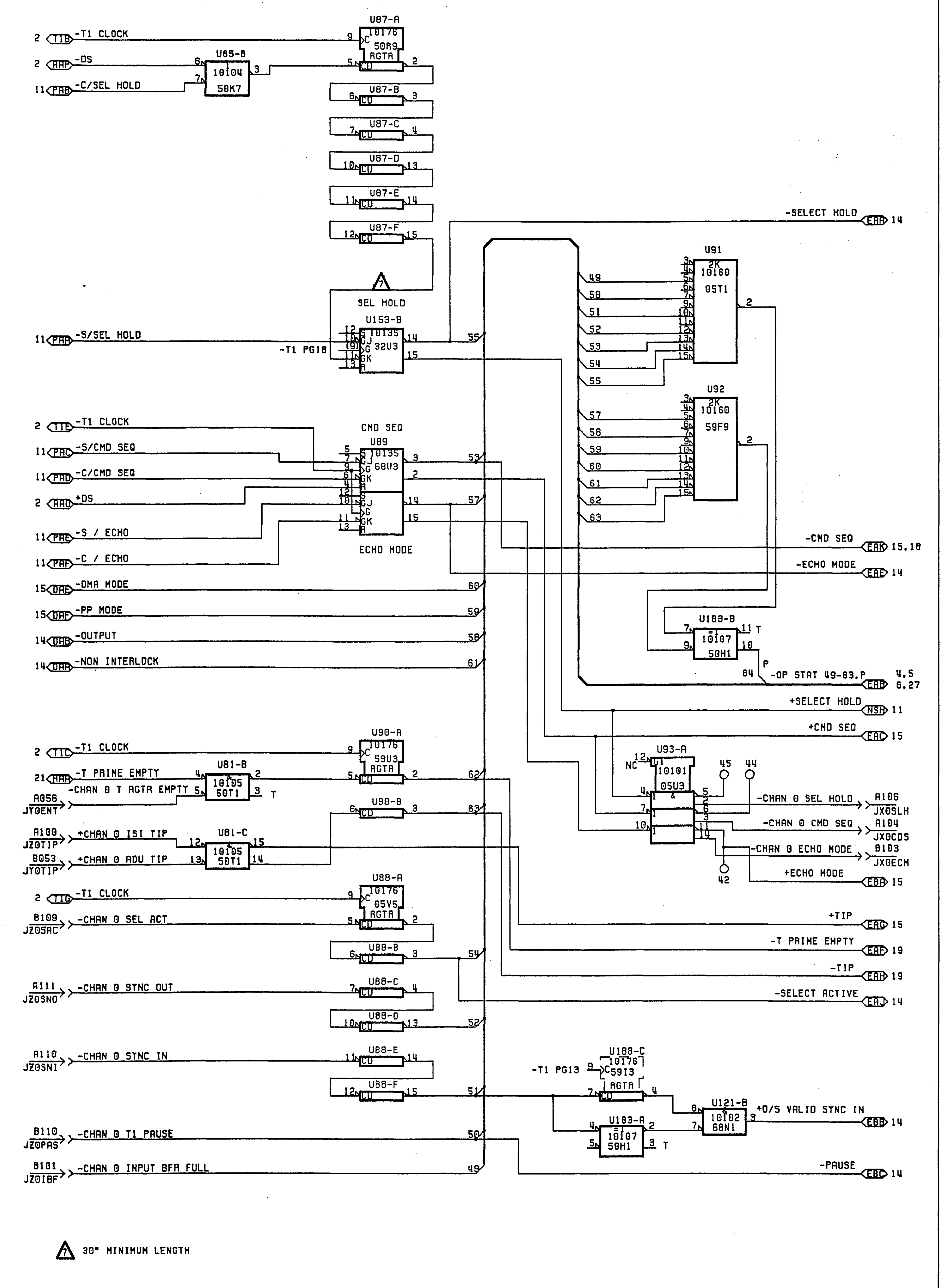


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
ADAPTER PP / DMA
MODE REGISTERS
TYPE 1JXH

B	DWG NO. 53575512	DATE 04/07/86	REV A
SHEET NO. 15	60462210	PAGE JX-15	

OPERATIONAL STATUS NETWORK (3.7)



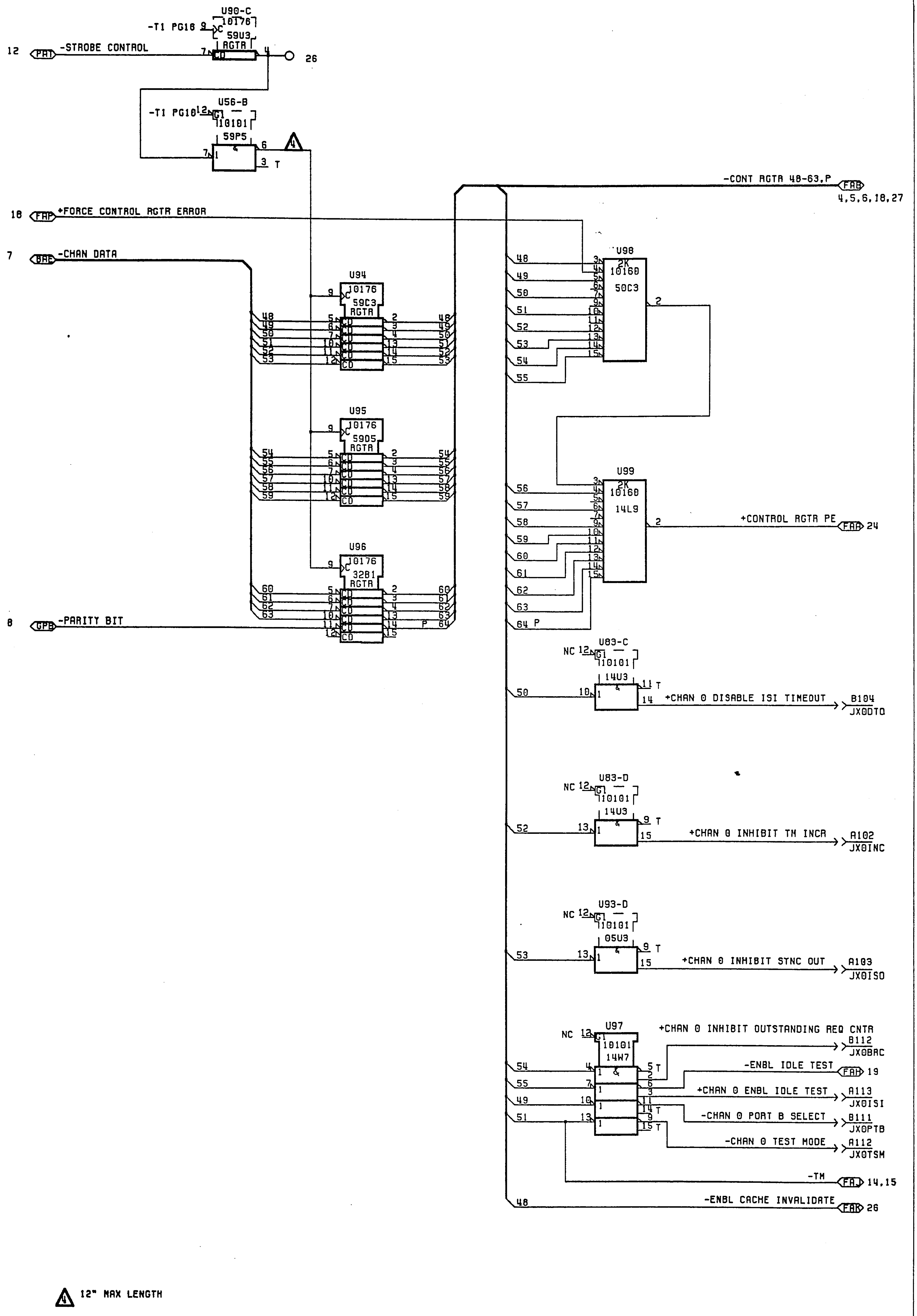
7 30" MINIMUM LENGTH

CONTROL DATA

CIO CHANNEL BOARD BAS I/F
OPERATIONAL STATUS NETWORK
TYPE 1JXH

B	DWG NO. 53575512	DATE 04/07/86	REV A
SHEET NO. 16	60462210	PAGE JX-16	

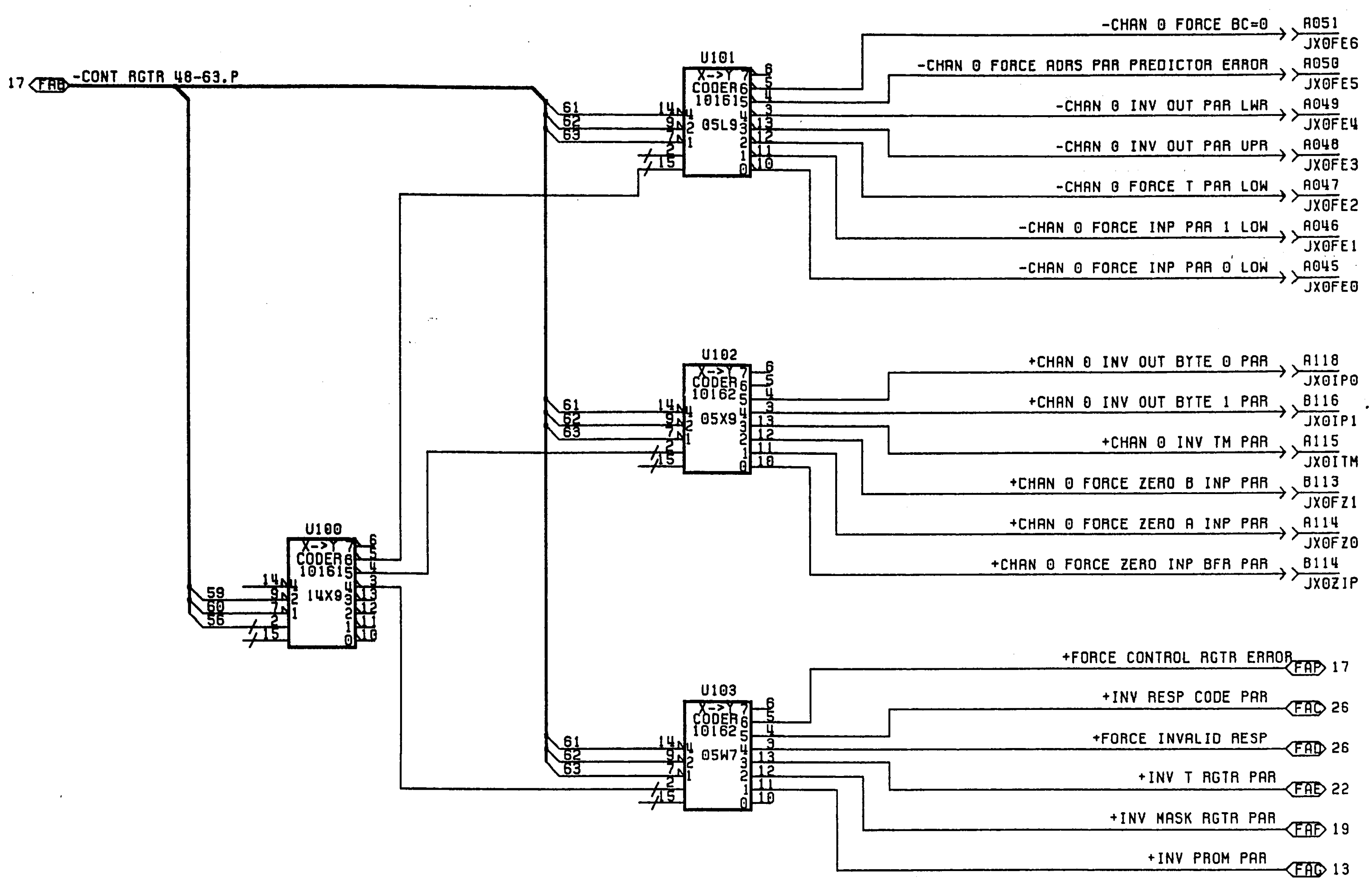
CONTROL REGISTERS (3.4)



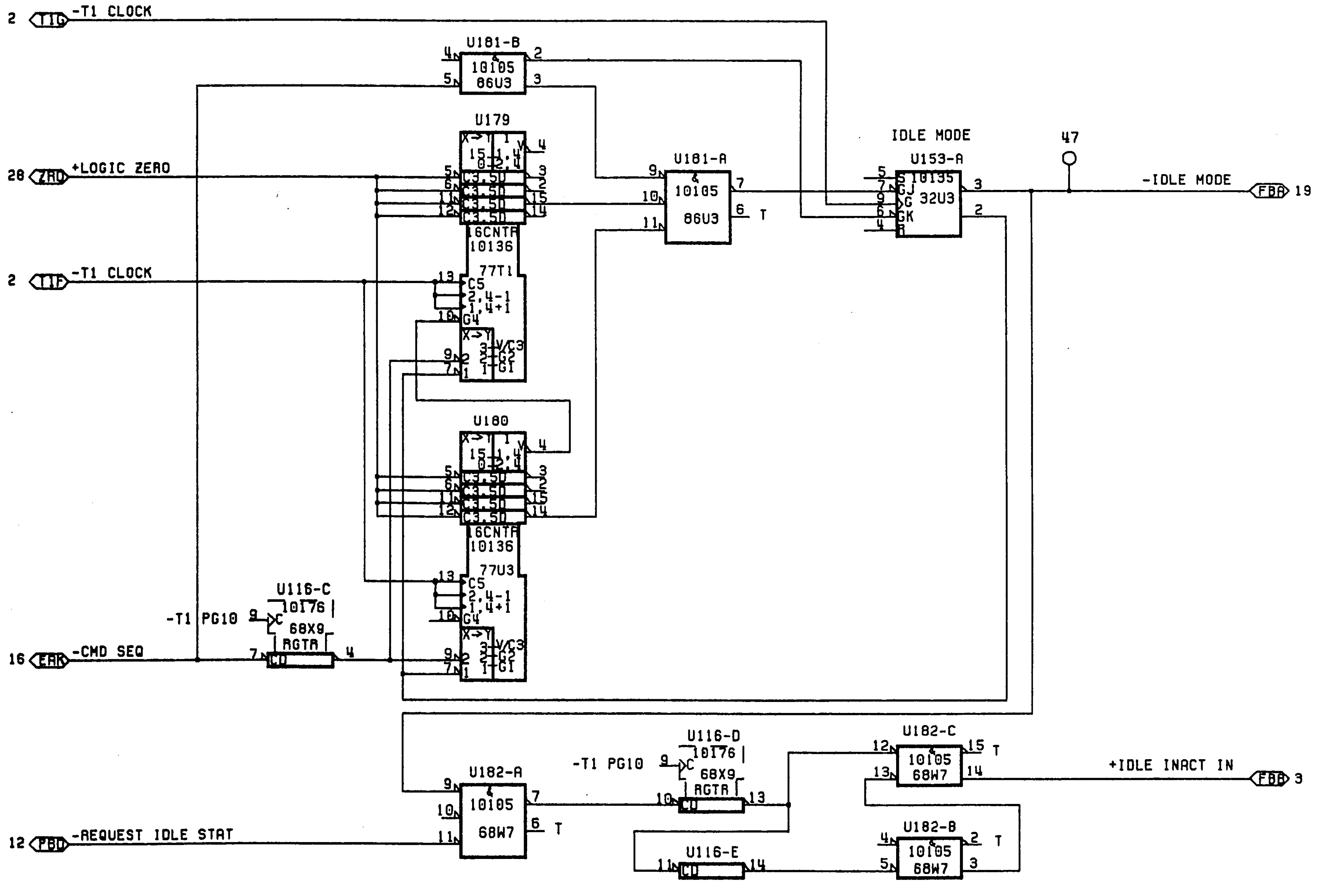
⚠4 12" MAX LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F CONTROL REGISTER TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
			SHEET NO. 17	60462210	PAGE JX-17

FORCE ERROR DECODERS (3.4)


17 FAB -CONT RGTR 48-63.P
U101 X->Y CODER 10161 05L9
U102 X->Y CODER 10162 05X9
U103 X->Y CODER 10162 05W7
U100 X->Y CODER 10161 14X9
59 60 56
61 62 63
-CHAN 0 FORCE BC=0 A051 JX0FE6
-CHAN 0 FORCE ADRS PAR PREDICTOR ERROR A050 JX0FE5
-CHAN 0 INV OUT PAR LWR A049 JX0FE4
-CHAN 0 INV OUT PAR UPR A048 JX0FE3
-CHAN 0 FORCE T PAR LOW A047 JX0FE2
-CHAN 0 FORCE INP PAR 1 LOW A046 JX0FE1
-CHAN 0 FORCE INP PAR 0 LOW A045 JX0FE0
+CHAN 0 INV OUT BYTE 0 PAR A118 JX0IP0
+CHAN 0 INV OUT BYTE 1 PAR B116 JX0IP1
+CHAN 0 INV TM PAR A115 JX0ITM
+CHAN 0 FORCE ZERO B INP PAR B113 JX0FZ1
+CHAN 0 FORCE ZERO A INP PAR A114 JX0FZ0
+CHAN 0 FORCE ZERO INP BFR PAR B114 JX0ZIP
+FORCE CONTROL RGTR ERROR FAP 17
+INV RESP CODE PAR FAC 26
+FORCE INVALID RESP FAD 26
+INV T RGTR PAR FAE 22
+INV MASK RGTR PAR FAF 19
+INV PROM PAR FAG 13

IDLE MODE DELAY (3.4)

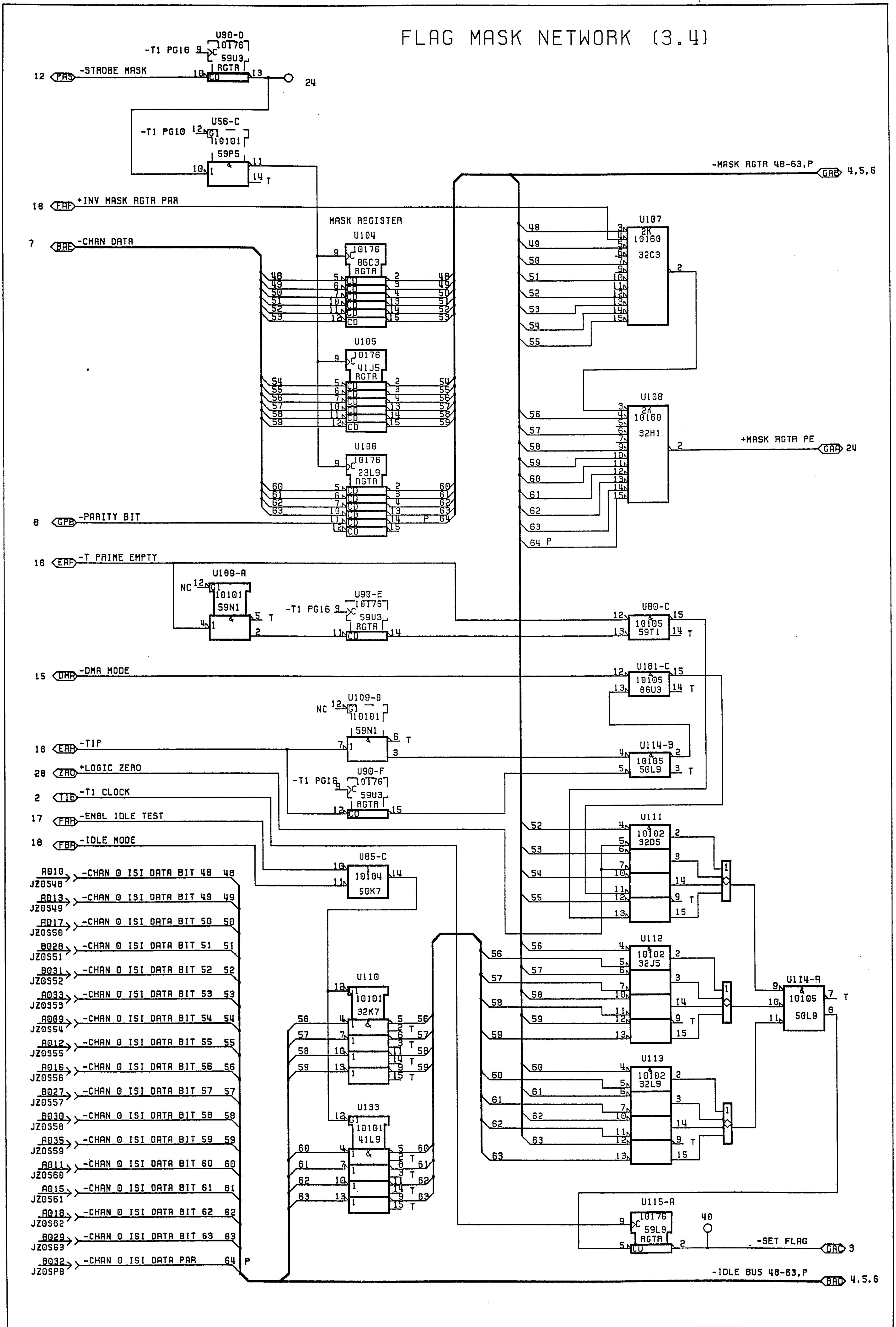


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FORCE ERROR DECODERS
IDLE MODE DELAY
TYPE 1JXH

B	DWG NO. 53575512	DATE 07/07/86	REV C
SHEET NO. 18	60462210	PAGE JX-18	

FLAG MASK NETWORK (3.4)

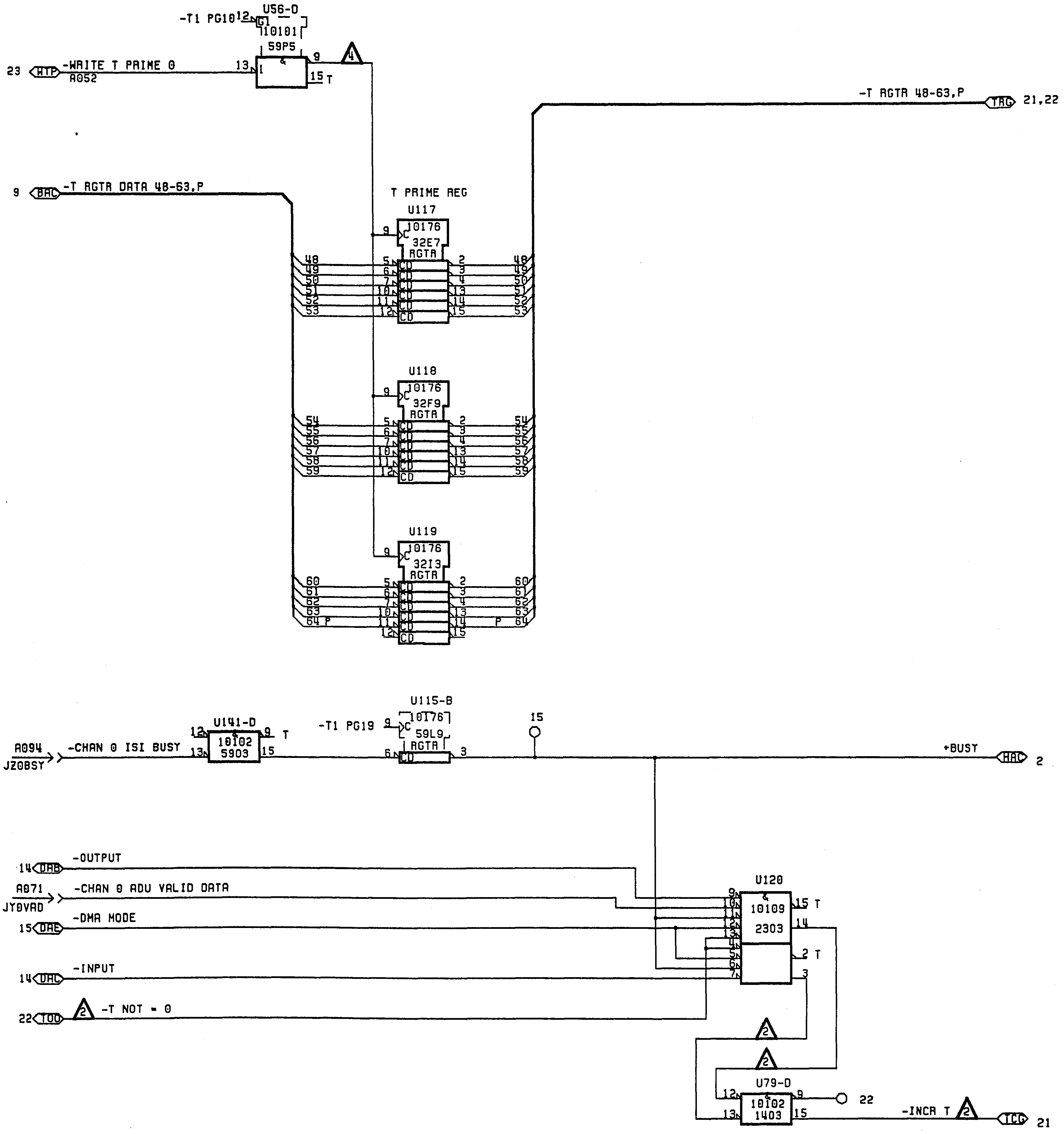

12 PAS -STROBE MASK
U90-D 10176 59U3 RGTR
-T1 PG16
24
U56-C 10101 59P5
-T1 PG10
-MASK RGTR 48-63,P GAB 4,5,6
18 FAF +INV MASK RGTR PAR
MASK REGISTER
U104 10176 86C3 RGTR
7 BAE -CHAN DATA
U105 10176 41J5 RGTR
U106 10176 23L9 RGTR
8 GPB -PARITY BIT
U107 2K 10160 32C3
U108 2K 10160 32H1
+MASK RGTR PE GAA 24
16 EAF -T PRIME EMPTY
U109-A 10101 59N1
NC
U90-E 10176 59U3 RGTR
-T1 PG16
U80-C 10105 59T1
15 DMA -DMA MODE
U101-C 10105 86U3
U109-B 10101 59N1
NC
16 EAB -TIP
U114-B 10105 50L9
28 ZAO +LOGIC ZERO
U90-F 10176 59U3 RGTR
-T1 PG16
2 TIE -T1 CLOCK
17 FAB -ENBL IDLE TEST
18 FBA -IDLE MODE
U85-C 10104 50K7
U111 10102 32D5
U112 10102 32J5
U113 10102 32L9
U114-A 10105 50L9
U110 10101 32K7
U133 10101 41L9
A010 JZ0S48 -CHAN 0 ISI DATA BIT 48 48
A013 JZ0S49 -CHAN 0 ISI DATA BIT 49 49
A017 JZ0S50 -CHAN 0 ISI DATA BIT 50 50
B028 JZ0S51 -CHAN 0 ISI DATA BIT 51 51
B031 JZ0S52 -CHAN 0 ISI DATA BIT 52 52
A033 JZ0S53 -CHAN 0 ISI DATA BIT 53 53
A009 JZ0S54 -CHAN 0 ISI DATA BIT 54 54
A012 JZ0S55 -CHAN 0 ISI DATA BIT 55 55
A016 JZ0S56 -CHAN 0 ISI DATA BIT 56 56
B027 JZ0S57 -CHAN 0 ISI DATA BIT 57 57
B030 JZ0S58 -CHAN 0 ISI DATA BIT 58 58
A035 JZ0S59 -CHAN 0 ISI DATA BIT 59 59
A011 JZ0S60 -CHAN 0 ISI DATA BIT 60 60
A015 JZ0S61 -CHAN 0 ISI DATA BIT 61 61
A018 JZ0S62 -CHAN 0 ISI DATA BIT 62 62
B029 JZ0S63 -CHAN 0 ISI DATA BIT 63 63
B032 JZ0SP8 -CHAN 0 ISI DATA PAR 64 P
U115-A 10176 59L9 RGTR
40
-SET FLAG GAC 3
-IDLE BUS 48-63,P BAD 4,5,6

CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FLAG MASK NETWORK
TYPE 1JXH

B
DWG NO. 53575512
DATE 04/07/86
REV A
SHEET NO. 19
60462210
PAGE JX-19

T PRIME REGISTER (3.5)

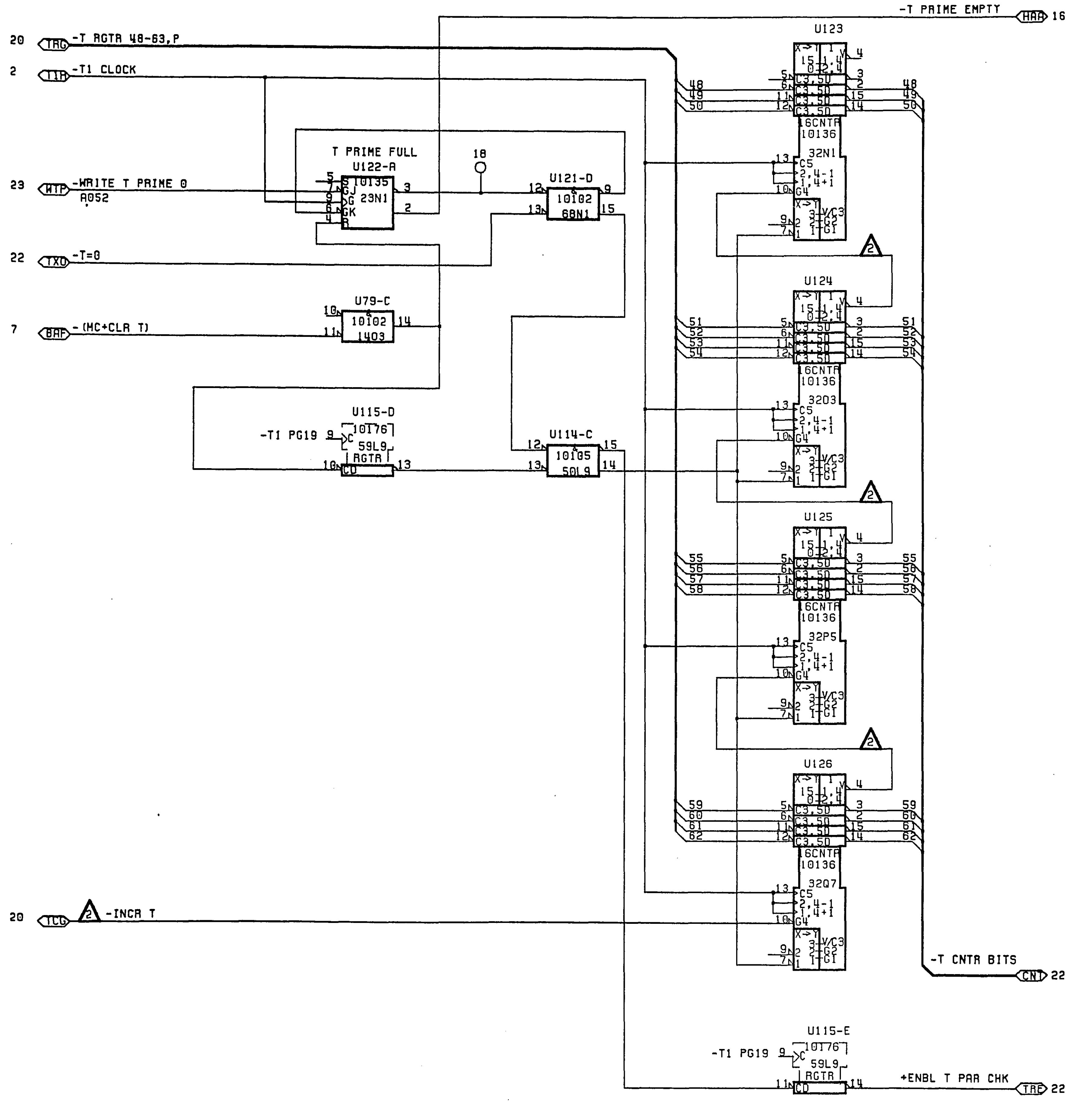


△ 2" MAXIMUM LENGTH

△ 12" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F T PRIME REGISTER TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
	N	SHEET NO. 20	60462210	PAGE JX-20	

T RGTR COUNTER (3.5)



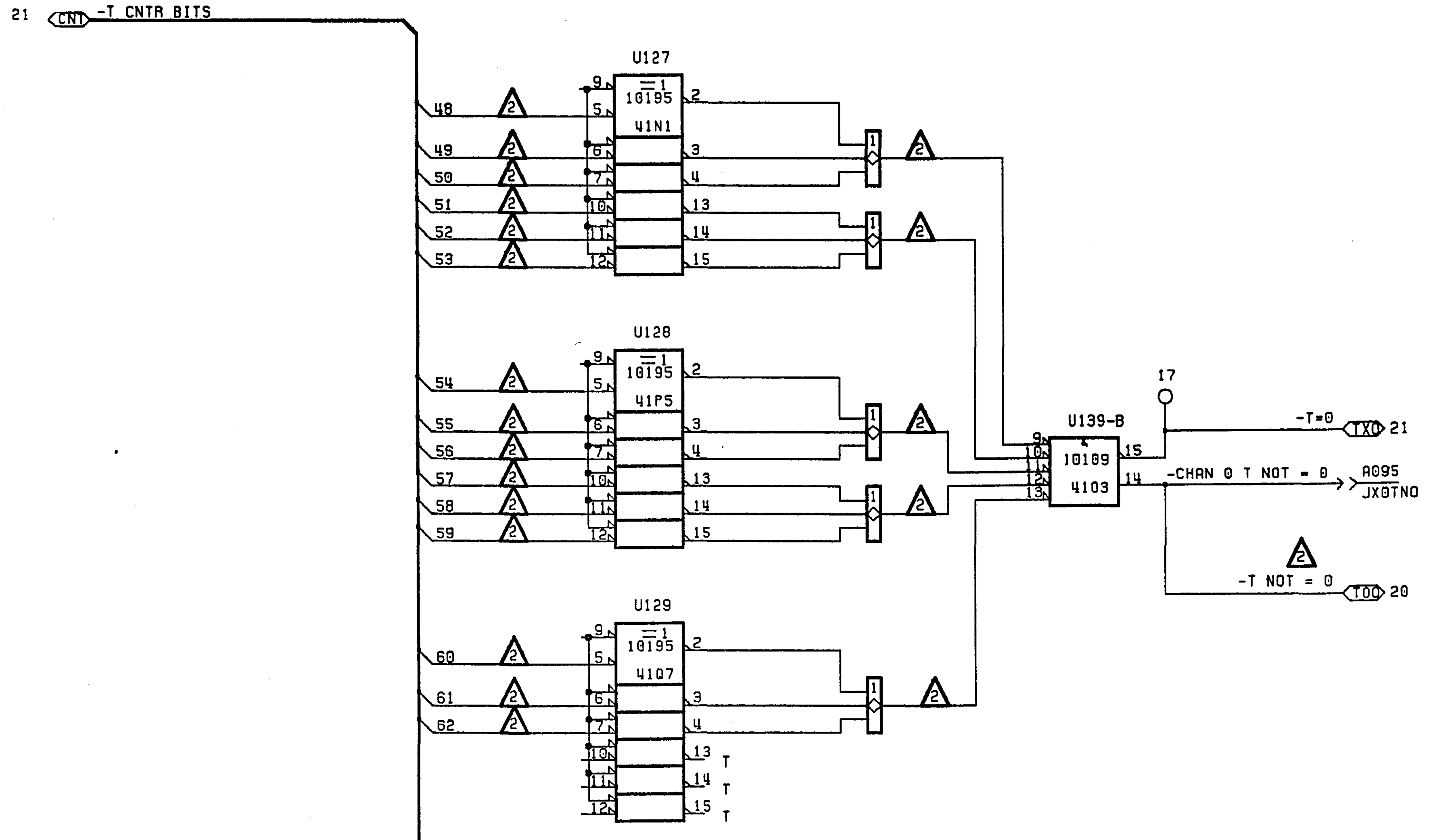
2" MAXIMUN LENGTH

CONTROL DATA

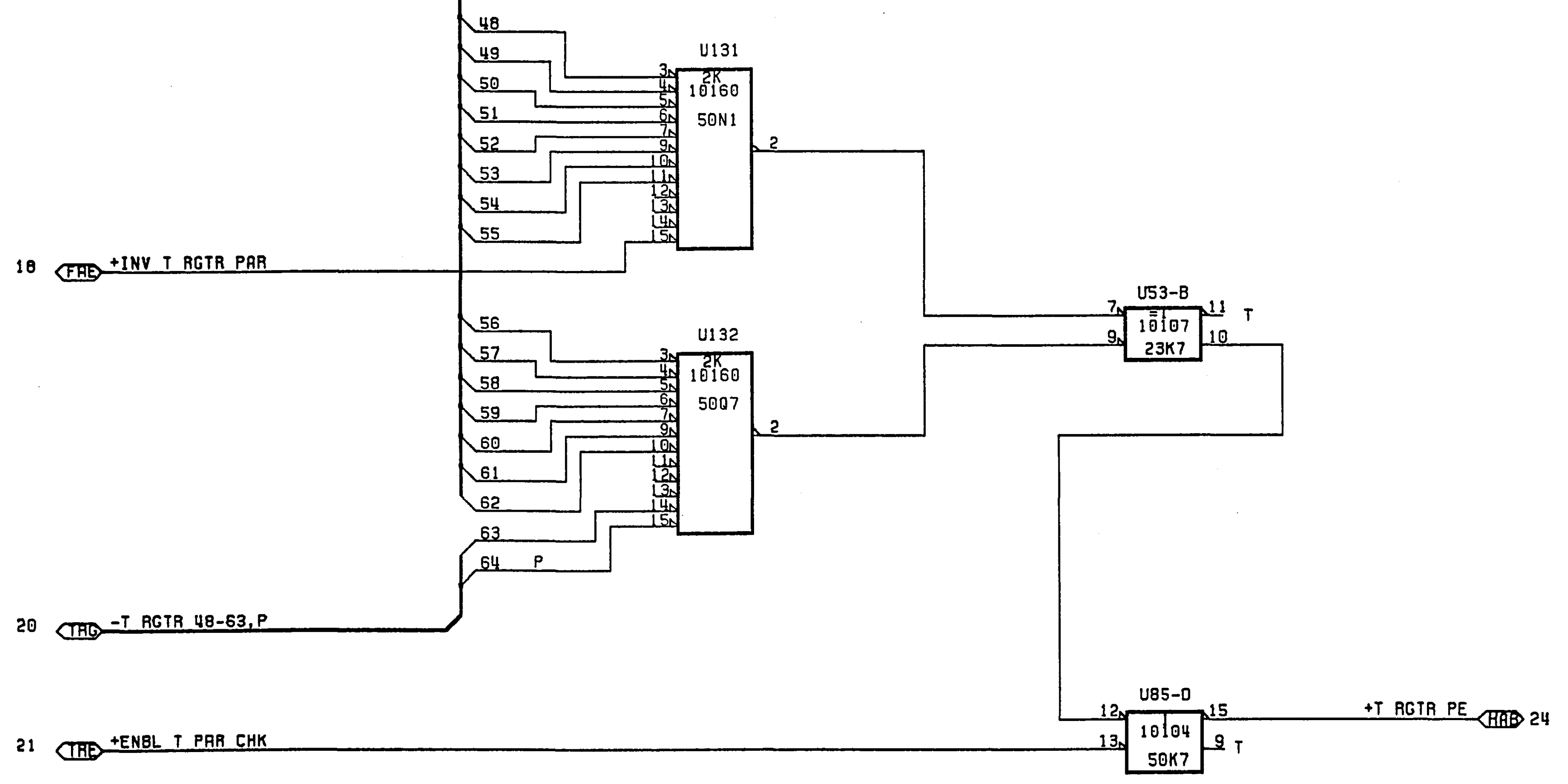
CIO CHANNEL BOARD BAS I/F
T RGTR COUNTER
TYPE 1JXH

B	DWG NO. 53575512	DATE 04/07/86	REV A
SHEET NO. 21	60462210	PAGE JX-21	

T RGTR ZERO TEST (3.5)



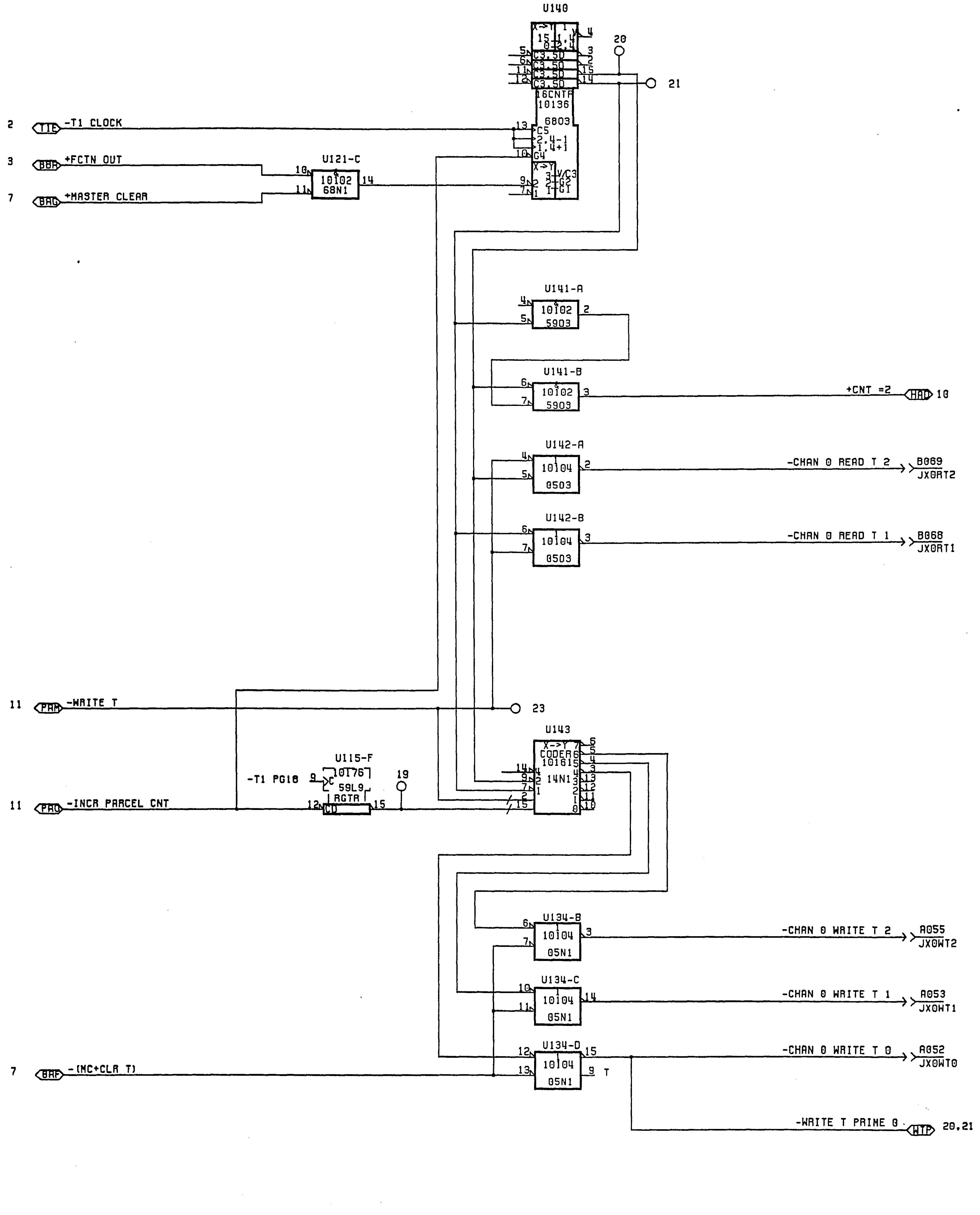
T RGTR PARITY CHECK (3.5)



2" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F T RGTR ZERO TEST & PARITY CHECK TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
			SHEET NO. 22	60462210	PAGE JX-22

T RGTR PARCEL COUNTER (3.5)

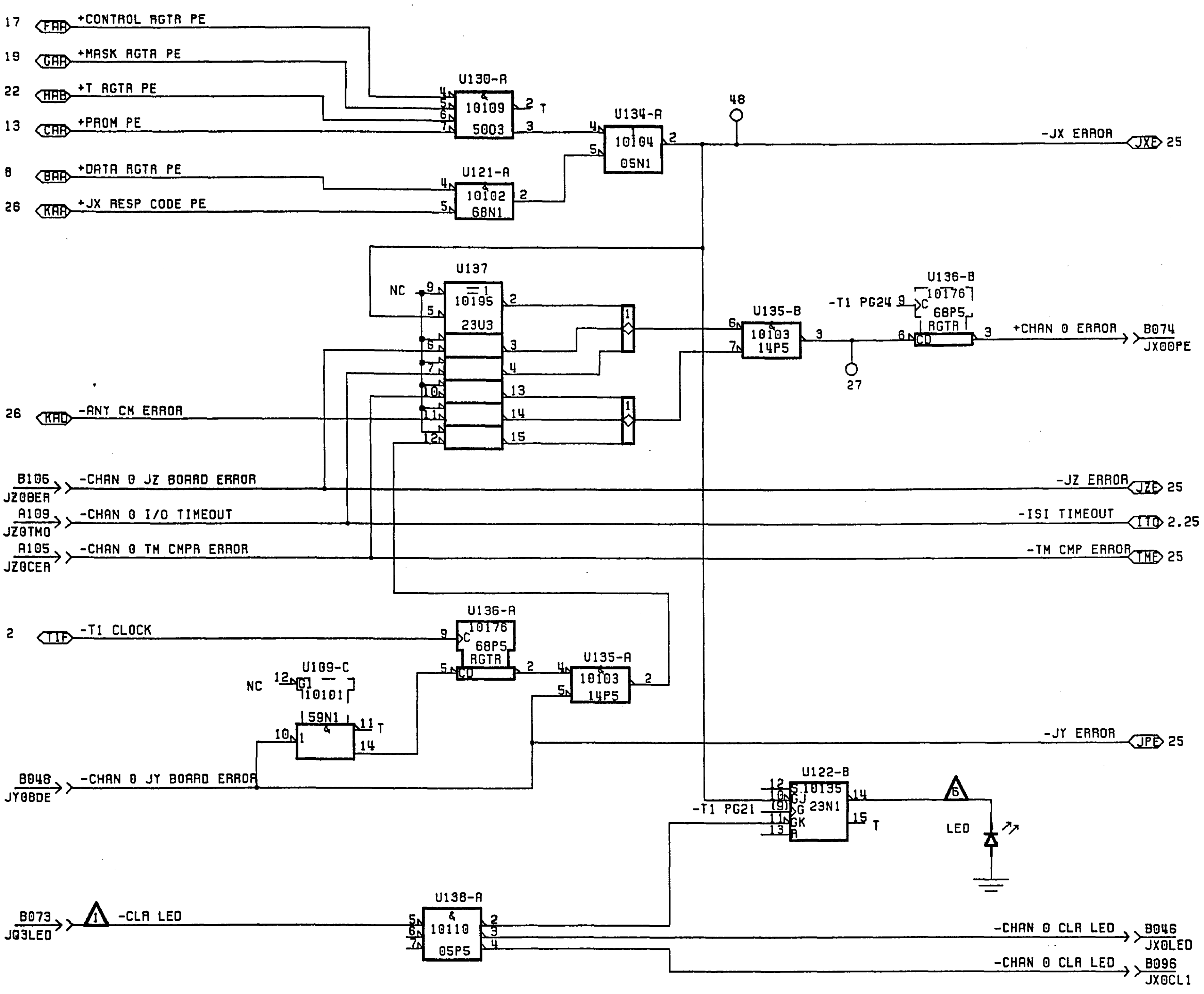


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
T REGISTER PARCEL COUNTER
TYPE 1JXH

B	DWG NO. 53575512		DATE 04/07/86		REV A
SHEET NO. 23		60462210		PAGE JX-23	

ERROR STATUS NETWORK (3.6)



RESERVED FOR FUTURE USE

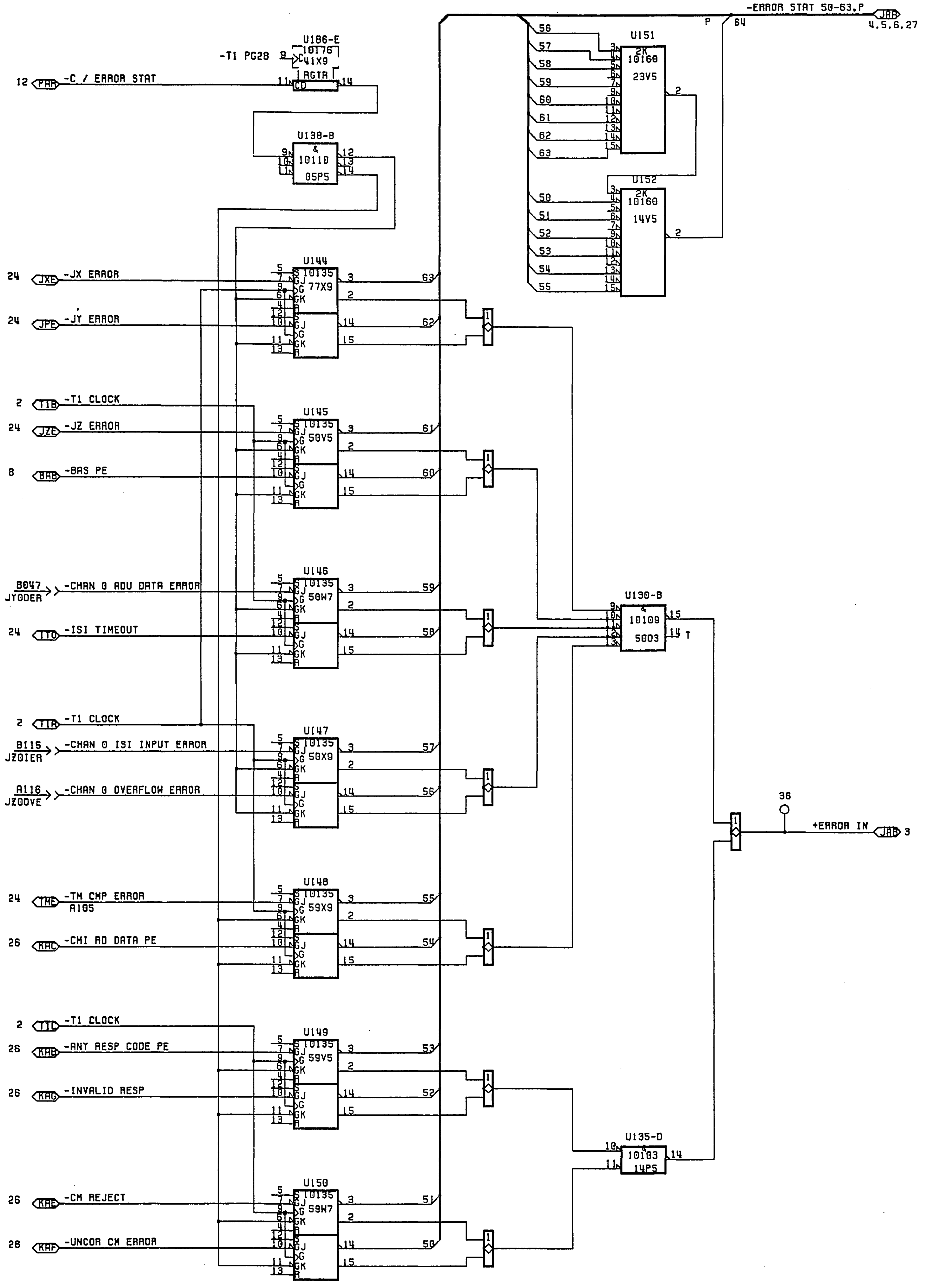
A061	OPEN	RESERVED FOR +5V
B061	OPEN	RESERVED FOR +5V
A070	OPEN	RESERVED FOR +5V
B070	OPEN	RESERVED FOR +5V
A068	RESV20	RESERVED FOR FUTURE USE
A076	RESV30	RESERVED FOR FUTURE USE
A079	JYBC00	RESERVED FOR FUTURE USE
A080	OPEN	RESERVED FOR FUTURE USE
A081	OPEN	RESERVED FOR FUTURE USE
A082	OPEN	RESERVED FOR FUTURE USE
A083	OPEN	RESERVED FOR FUTURE USE
A084	OPEN	RESERVED FOR FUTURE USE
A085	OPEN	RESERVED FOR FUTURE USE
A086	OPEN	RESERVED FOR FUTURE USE
A088	OPEN	RESERVED FOR FUTURE USE
A121	OPEN	RESERVED FOR FUTURE USE
B076	OPEN	RESERVED FOR FUTURE USE
B078	OPEN	RESERVED FOR FUTURE USE
B079	OPEN	RESERVED FOR FUTURE USE
B080	OPEN	RESERVED FOR FUTURE USE
B081	OPEN	RESERVED FOR FUTURE USE
B082	OPEN	RESERVED FOR FUTURE USE
B083	OPEN	RESERVED FOR FUTURE USE
B084	OPEN	RESERVED FOR FUTURE USE
B085	OPEN	RESERVED FOR FUTURE USE
B086	RESV10	RESERVED FOR FUTURE USE
B088	OPEN	RESERVED FOR FUTURE USE
A019	OPEN	RESERVED FOR FUTURE USE
A020	OPEN	RESERVED FOR FUTURE USE
A021	OPEN	RESERVED FOR FUTURE USE
A022	OPEN	RESERVED FOR FUTURE USE
A023	OPEN	RESERVED FOR FUTURE USE
A025	OPEN	RESERVED FOR FUTURE USE
A026	OPEN	RESERVED FOR FUTURE USE
B018	OPEN	RESERVED FOR FUTURE USE
B019	OPEN	RESERVED FOR FUTURE USE
B020	OPEN	RESERVED FOR FUTURE USE
B021	OPEN	RESERVED FOR FUTURE USE
B022	OPEN	RESERVED FOR FUTURE USE
B023	OPEN	RESERVED FOR FUTURE USE
B025	OPEN	RESERVED FOR FUTURE USE
B026	OPEN	RESERVED FOR FUTURE USE
A092	OPEN	RESERVED FOR FUTURE USE
B092	OPEN	RESERVED FOR FUTURE USE

△1 3" MAX LENGTH AND NOT TERMINATED

△6 TERMINATE

CONTROL DATA	CIO CHANNEL BOARD BAS I/F ERROR STATUS NETWORK TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
	N	SHEET NO. 24	60462210	PAGE JX-24	

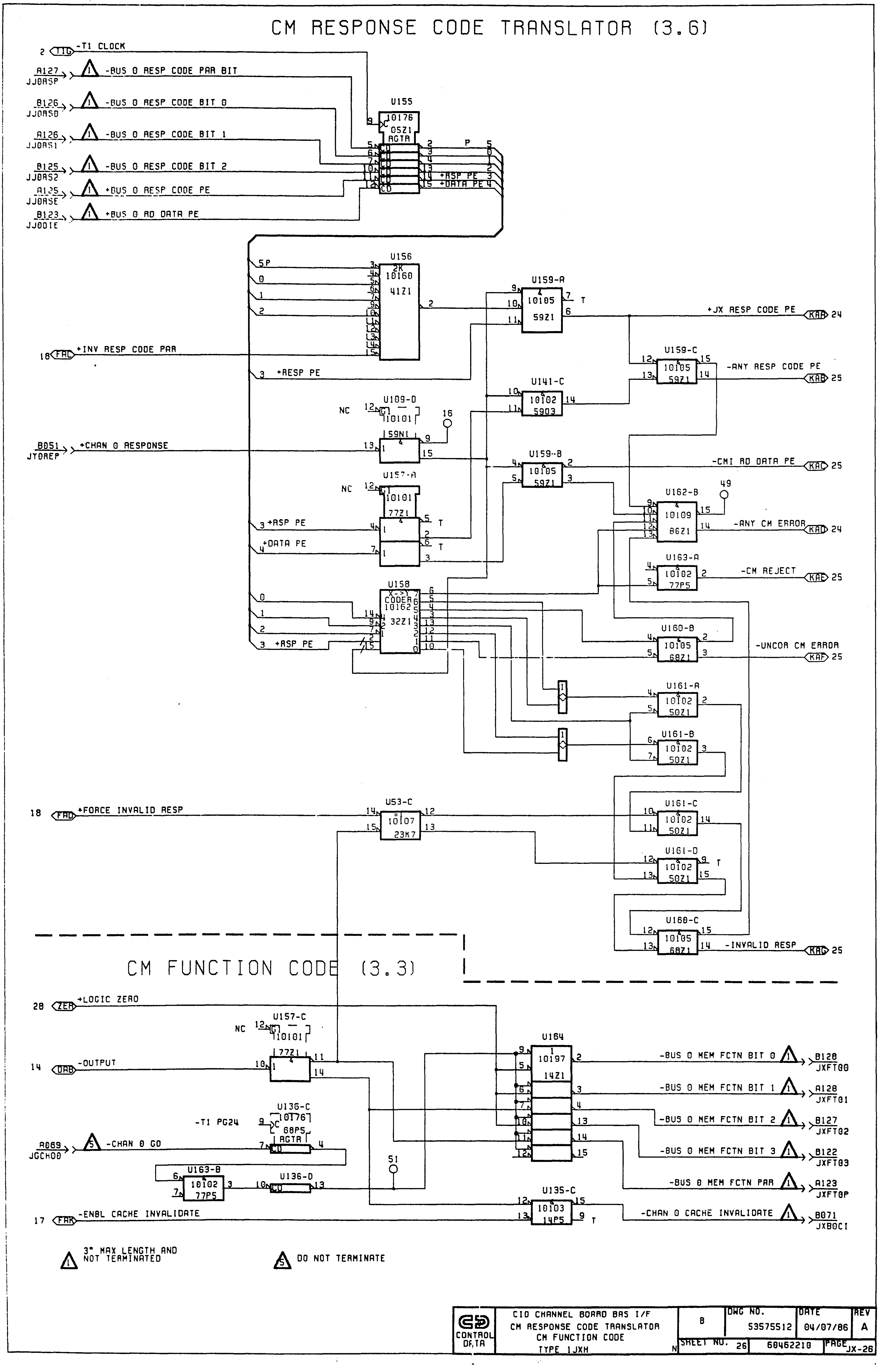
ERROR STATUS NETWORK (3.6)



CONTROL DATA

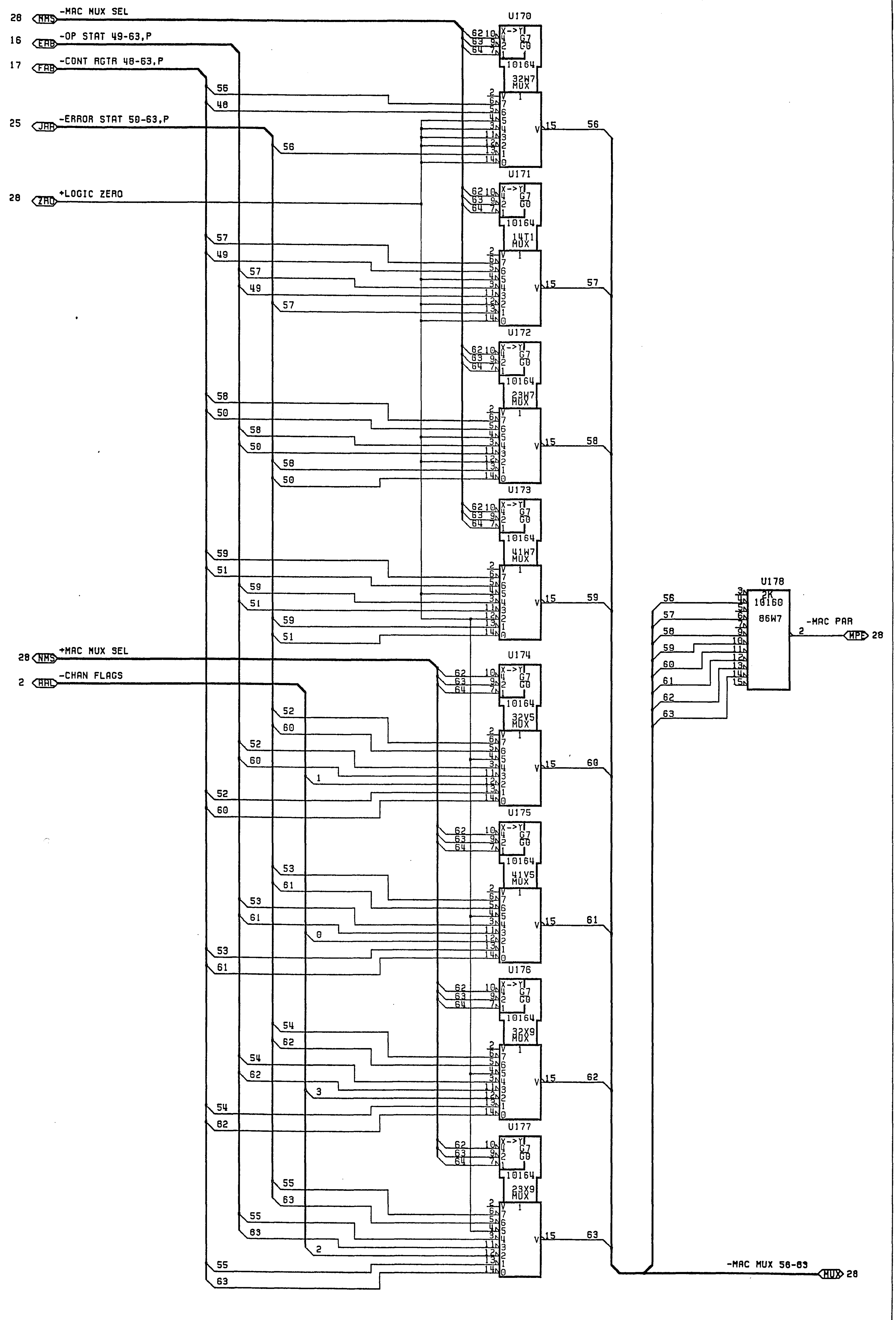
CIO CHANNEL BOARD BAS I/F
ERROR STAT NETWORK
TYPE 1JXH

B
DWG NO. 53575512
DATE 04/07/86
REV A
SHEET NO. 25
60462210
PAGE JX-25



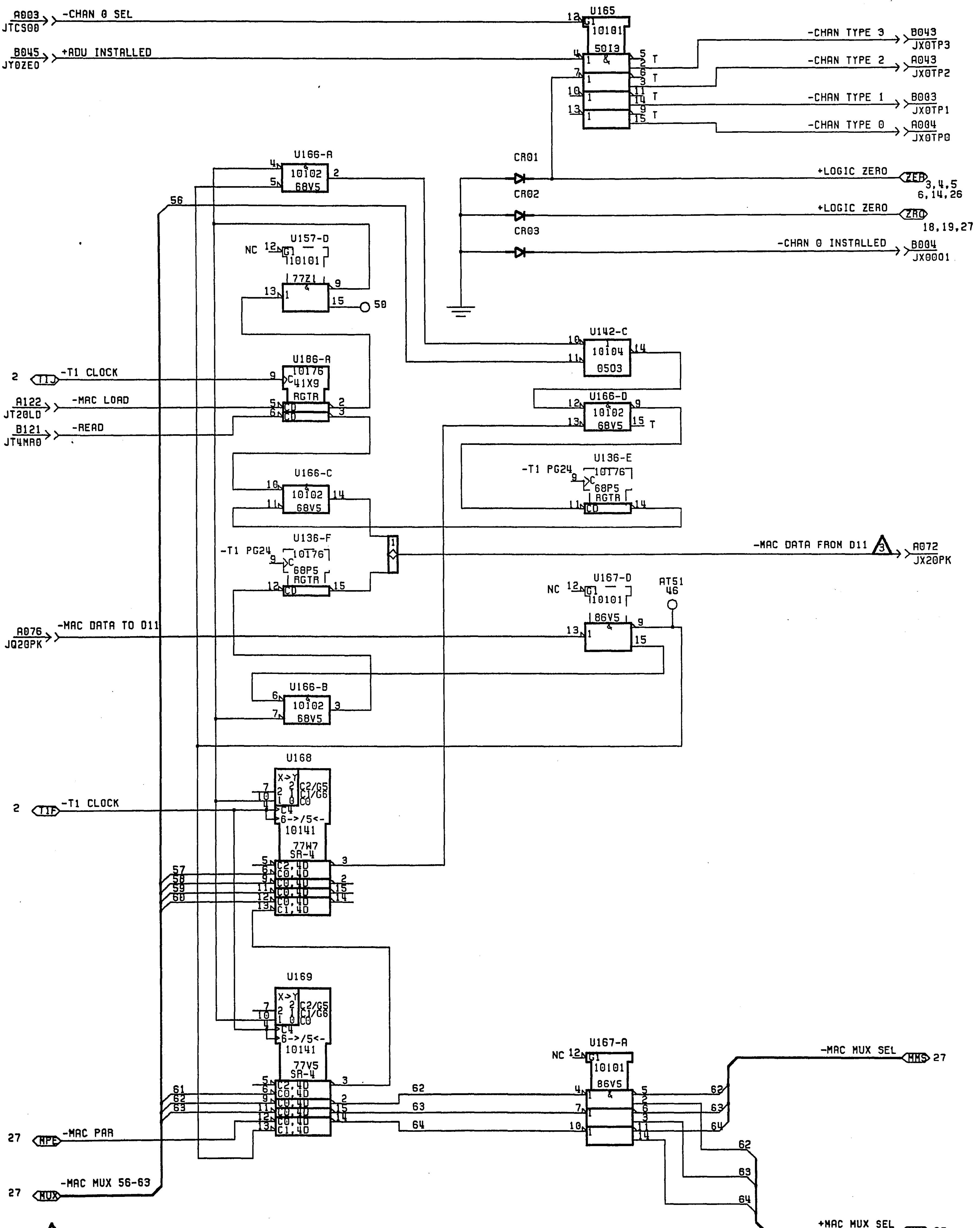
CONTROL DATA	CIO CHANNEL BOARD BAS I/F CM RESPONSE CODE TRANSLATOR CM FUNCTION CODE TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
		N	SHEET NO. 26	60462210	PAGE JX-26

MAC INTERFACE MUX (3.7)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F MAC INTERFACE MUX TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
		SHEET NO. 27	60462210	PAGE JX-27	

MAC INTERFACE (3.7)



3 TERM AT FARTHEST PIONT FROM CONN PIN

CONTROL DATA	CIO CHANNEL BOARD BAS I/F MAC INTERFACE TYPE 1JXH	B	DWG NO. 53575512	DATE 04/07/86	REV A
			SHEET NO. 28	60462210	PAGE JX-28

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	14	-ISI FUNC BIT 48	27	24	+CHANNEL ERROR
02	14	+ISI FUNC BIT 54	28	14	+FORCE SYNC OUT
03	10	-FUNC RGTR BIT 7	29	03	+ACTIVE FLAG
04	10	-FUNC RGTR BIT 5	30	14	-INPUT MODE
05	10	-FUNC RGTR BIT 6	31	14	+ISI FUNC WORD
06	14	-NON INTERLOCK	32	14	+BUS SLAVE SELECTED
07	10	-FUNC RGTR BIT 4	33	15	+DMA MODE
08	10	-FUNC RGTR BIT 3	34	03	+ERROR FLAG
09	10	-FUNC RGTR BIT 0	35	03	+FLAG
10	10	-FUNC RGTR BIT 2	36	25	+ERROR IN
11	10	-FUNC RGTR BIT 1	37	07	-CHAN DATA BIT 63
12	07	-CLEAR T RGTR	38	02	-DEADSTART OR MC
13	07	-MASTER CLEAR	39	03	-CHANNEL SELECT
14	15	+TRANSFER MODE	40	19	-SET FLAG
15	20	+ISI BUSY	41	03	+FULL FLAG
16	26	+CM RESPONSE	42	16	+ECHO MODE
17	22	-T RGTR EQUALS ZERO	43	15	+PP MODE
18	21	-T PRIME RGTR FULL	44	16	+CMD SEQUENCE
19	23	-INC PARCEL CNTR	45	16	+SEL HOLD
20	23	-PARCEL CNTR BIT 0	46	28	-MAC WRITE DATA
21	23	-PARCEL CNTR BIT 1	47	18	-IDLE MODE
22	20	+INCREMENT T CNT	48	24	-JX ERROR
23	23	-WRITE T	49	26	+ANY CM ERROR
24	19	-STROBE MASK RGTR	50	28	+MAC LOAD
25	02	-T1 CLOCK	51	26	-CHAN GO
26	17	-STROBE CONT RGTR			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 (NU)
TERM	NONE
UNUSED	A008,B018,A019,B019,A020,B020,A021,B021,A022,B022,A023,B023,A025,B025,A026,B026,B052,B076,A078,B078,A079,B079,A080,B080,A081,B081,A082,B082,A083,B083,A084,B084,A085,B085,A086,B086,A088,B088,A092,B092,B108,A121

CONTROL DATA

CIO CHANNEL BOARD BAS I/F
TESTPOINTS AND SIGNAL NAMES
AND CONNECTOR PINS
TYPE 1JXH

N

B

DWG NO. 53575512

DATE 02/07/86

REV A

SHEET NO. 29

60462210

PAGE JX-29

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1JXH CIO CHANNEL BOARD BAS I/F

REVISION HISTORY B/M 41652501			
DATE	REV	DESCRIPTION OF CHANGE	INIT
02/28/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	LHJ
07/07/86	B	ECO #47746 CORRECTS SHTS 14 & 18.	LHJ
03/14/88	C	ECO #49487 PAGE 2	SZP
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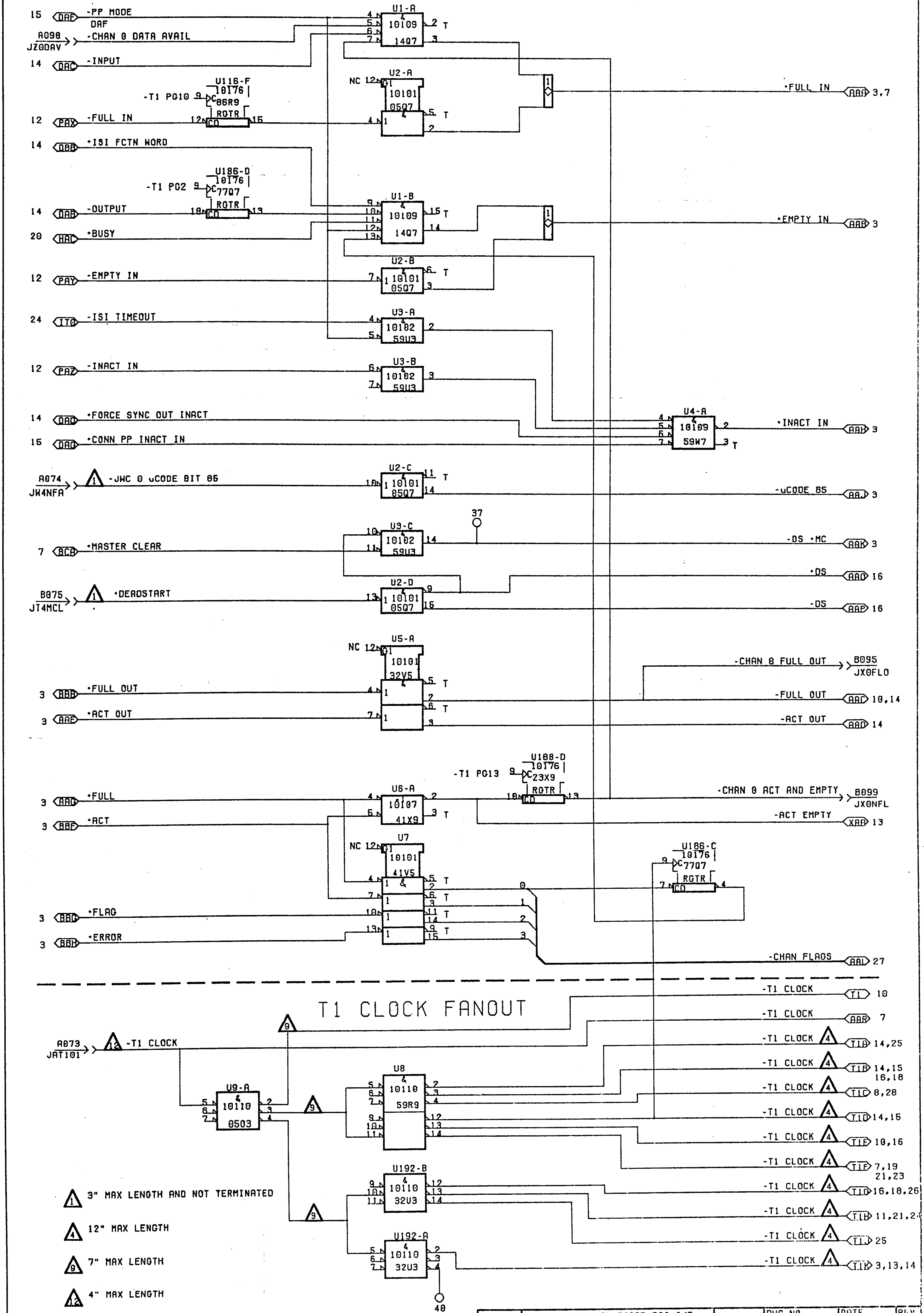
DWN	L H JOHNSON	02/28/86
CHKD	L H JOHNSON	03/11/86
ENG	D A ZAHALAN	03/11/86
PUBS	R K BONDE	03/11/86
APP	D A ZAHALAN	03/11/86

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D11,D14,D17,D20,D23
C11,C14,C17,C20,C23

CONTROL DATA	REVISION HISTORY TYPE 1JXH	B	DWG NO. 22105623	DATE 03/14/88	REV C
		SHEET NO. 1	60462210	PAGE JX-01	

CHANNEL I/O TO MACROCELL (3.0)

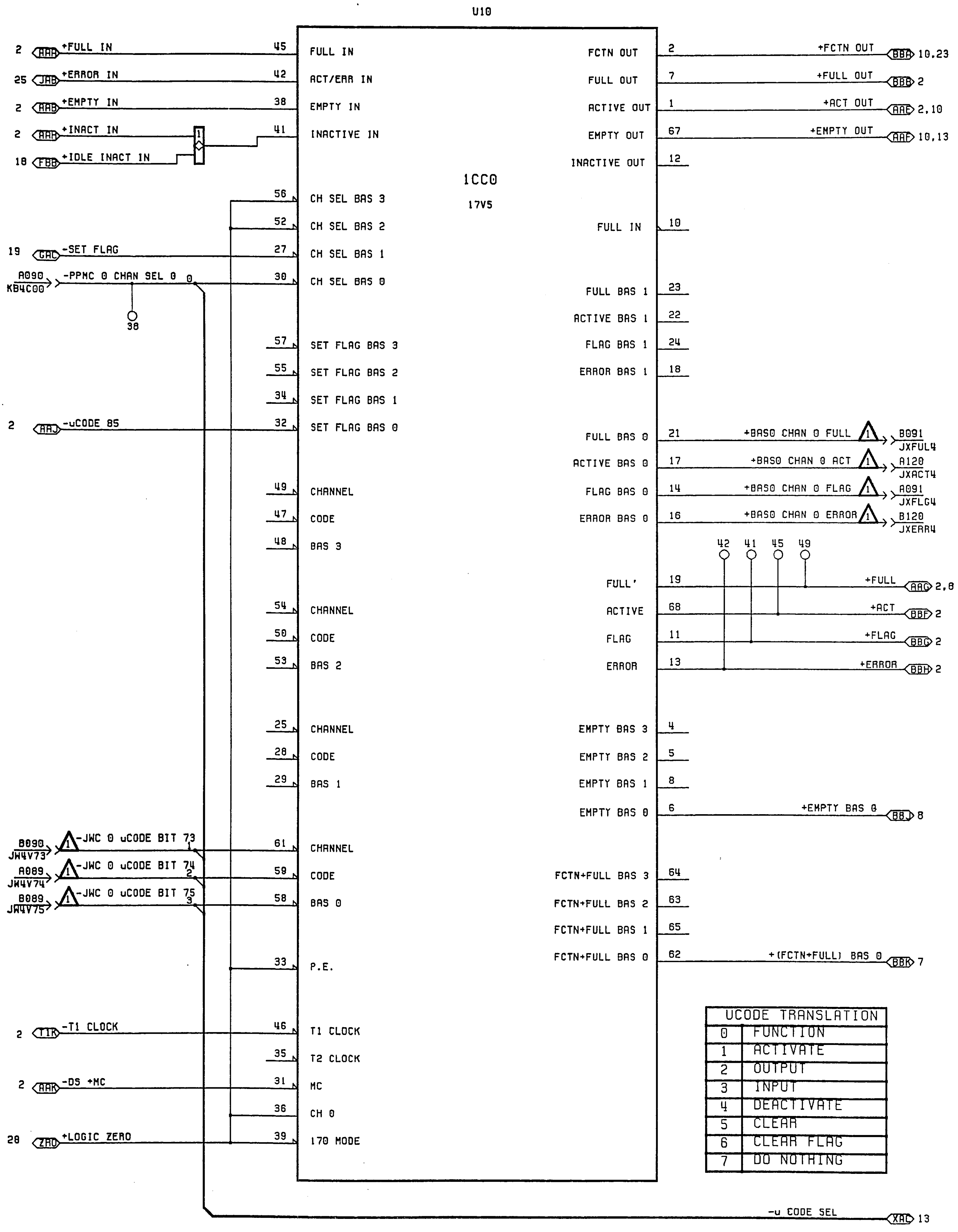


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
CHANNEL I/O TO MACRO
T1 CLOCK FANOUT
TYPE 1JXH

B	DWG NO. 22105623	DATE 03/14/88	REV C
SHEET NO. 2	60462210	PAGE JX-02	

CHANNEL FLAGS AND MICROCODE TRANSLATOR (3.0)

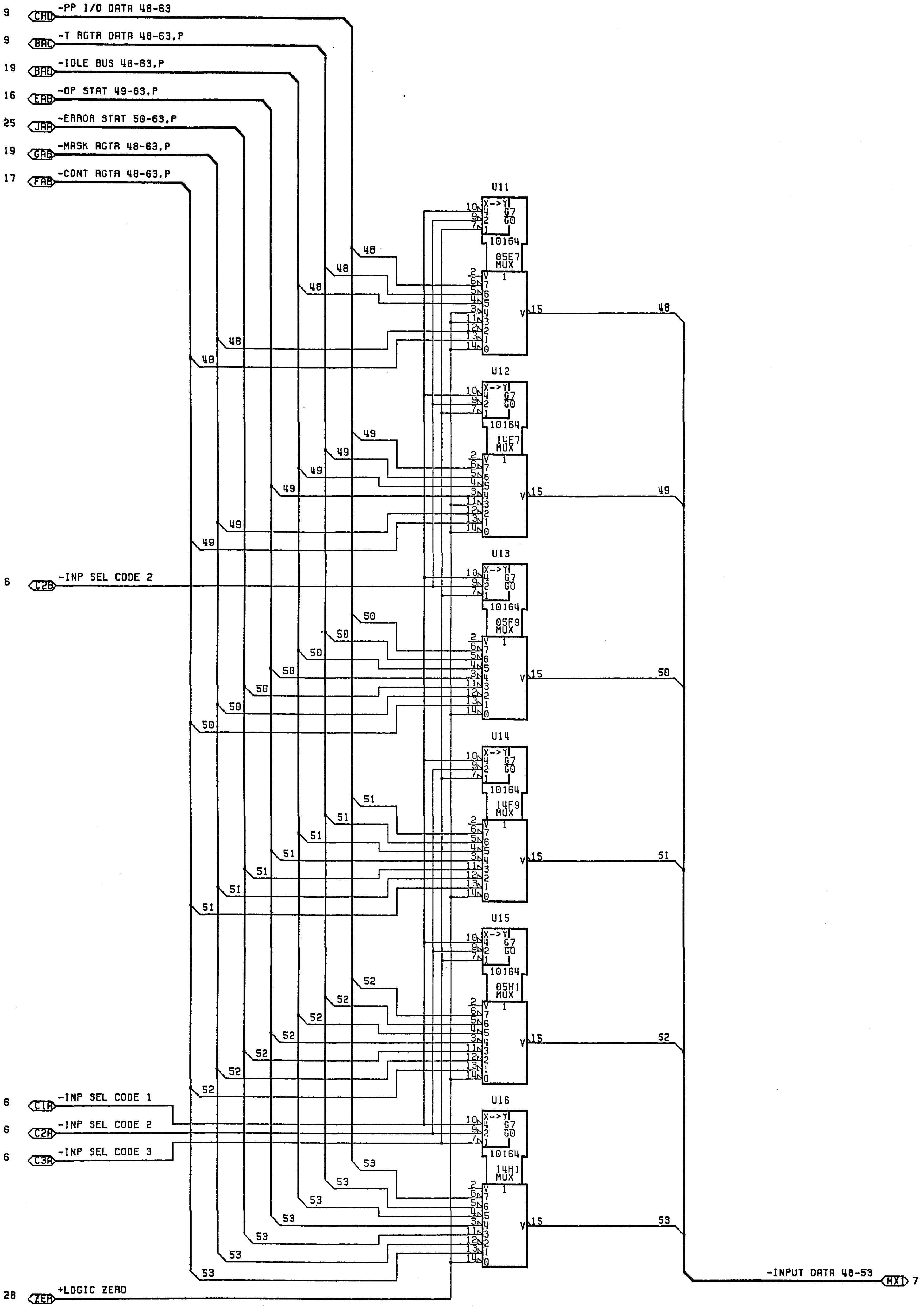

U10
1CC0
17V5
2 AAA +FULL IN 45 FULL IN
25 JAB +ERROR IN 42 ACT/ERR IN
2 AAB +EMPTY IN 38 EMPTY IN
2 AAA +INACT IN 41 INACTIVE IN
18 FBB +IDLE INACT IN
1
56 CH SEL BAS 3
52 CH SEL BAS 2
19 GAC -SET FLAG 27 CH SEL BAS 1
A090 KB4C00 -PPMC 0 CHAN SEL 0 0 30 CH SEL BAS 0
38
57 SET FLAG BAS 3
55 SET FLAG BAS 2
34 SET FLAG BAS 1
2 AAJ -uCODE 85 32 SET FLAG BAS 0
49 CHANNEL
47 CODE
48 BAS 3
54 CHANNEL
50 CODE
53 BAS 2
25 CHANNEL
28 CODE
29 BAS 1
B090 JW4V73 1 -JWC 0 uCODE BIT 73 1 61 CHANNEL
A089 JW4V74 1 -JWC 0 uCODE BIT 74 2 59 CODE
B089 JW4V75 1 -JWC 0 uCODE BIT 75 3 58 BAS 0
33 P.E.
2 T1K -T1 CLOCK 46 T1 CLOCK
35 T2 CLOCK
2 AAK -DS +MC 31 MC
36 CH 0
28 ZRO +LOGIC ZERO 39 170 MODE
FCTN OUT 2 +FCTN OUT BBA 10,23
FULL OUT 7 +FULL OUT BBB 2
ACTIVE OUT 1 +ACT OUT AAE 2,10
EMPTY OUT 67 +EMPTY OUT AAF 10,13
INACTIVE OUT 12
FULL IN 10
FULL BAS 1 23
ACTIVE BAS 1 22
FLAG BAS 1 24
ERROR BAS 1 18
FULL BAS 0 21 +BAS0 CHAN 0 FULL 1 B091 JXFUL4
ACTIVE BAS 0 17 +BAS0 CHAN 0 ACT 1 A120 JXACT4
FLAG BAS 0 14 +BAS0 CHAN 0 FLAG 1 A091 JXFLG4
ERROR BAS 0 16 +BAS0 CHAN 0 ERROR 1 B120 JXERR4
42 41 45 49
FULL' 19 +FULL AAC 2,8
ACTIVE 68 +ACT BBF 2
FLAG 11 +FLAG BBG 2
ERROR 13 +ERROR BBH 2
EMPTY BAS 3 4
EMPTY BAS 2 5
EMPTY BAS 1 8
EMPTY BAS 0 6 +EMPTY BAS 0 BBJ 8
FCTN+FULL BAS 3 64
FCTN+FULL BAS 2 63
FCTN+FULL BAS 1 65
FCTN+FULL BAS 0 62 +(FCTN+FULL) BAS 0 BBK 7
-u CODE SEL XAC 13

UCODE TRANSLATION	
0	FUNCTION
1	ACTIVATE
2	OUTPUT
3	INPUT
4	DEACTIVATE
5	CLEAR
6	CLEAR FLAG
7	DO NOTHING

1 3" MAX LENGTH AND NOT TERMINATED

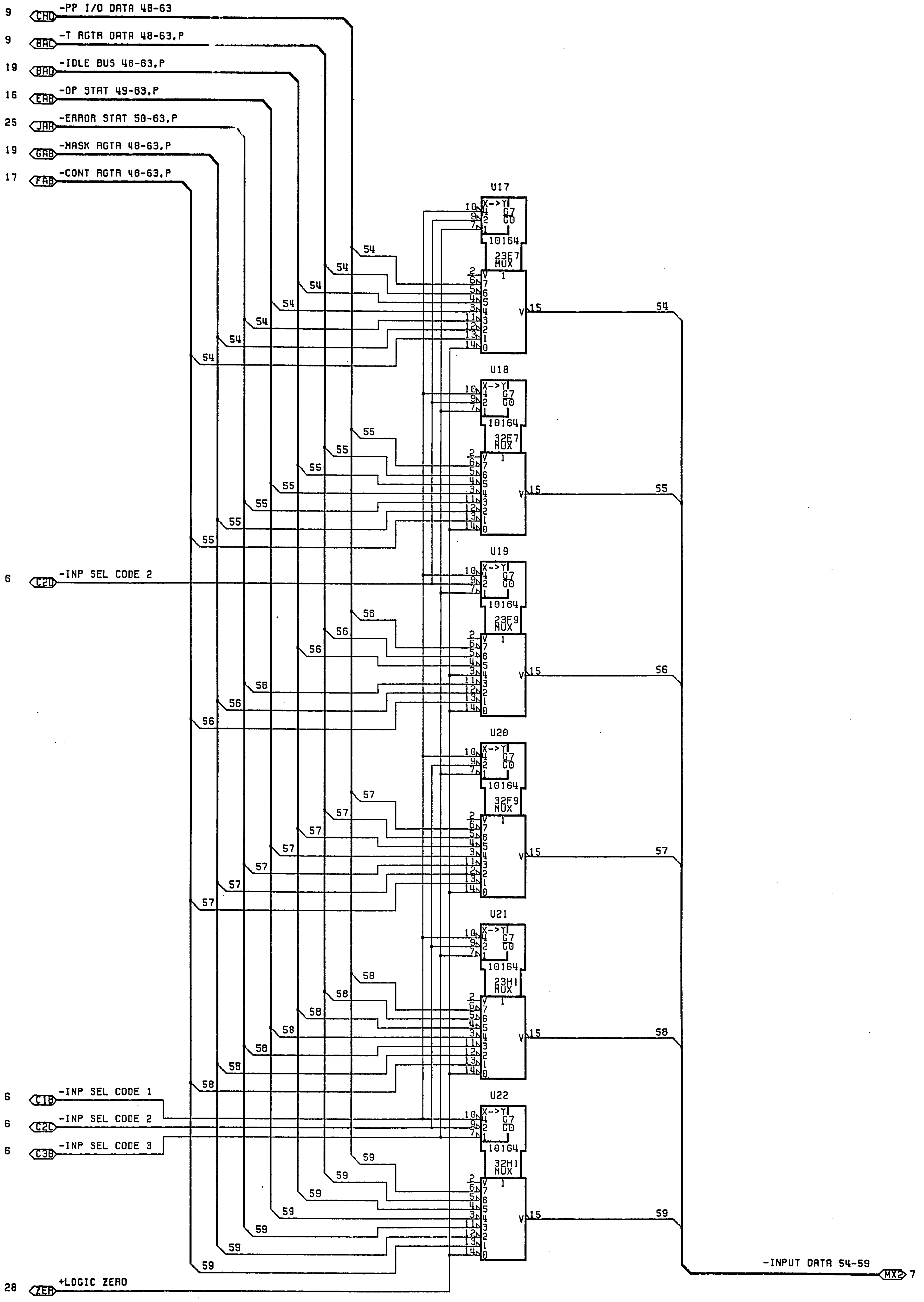
CONTROL DATA	CIO CHANNEL BOARD BAS I/F MACROCELL TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		SHEET NO. 3	60462210	PAGE JX-03	

INPUT DATA MUX BITS 48-53 (3.1)


9 CAD -PP I/O DATA 48-63
9 BAC -T RGTR DATA 48-63,P
19 BAD -IDLE BUS 48-63,P
16 EAB -OP STAT 49-63,P
25 JAA -ERROR STAT 50-63,P
19 GAB -MASK RGTR 48-63,P
17 FAB -CONT RGTR 48-63,P
6 C2B -INP SEL CODE 2
6 C1A -INP SEL CODE 1
6 C2A -INP SEL CODE 2
6 C3A -INP SEL CODE 3
28 ZEA +LOGIC ZERO
U11 X->Y G7 G0 10164 05E7 MUX
U12 X->Y G7 G0 10164 14E7 MUX
U13 X->Y G7 G0 10164 05F9 MUX
U14 X->Y G7 G0 10164 14F9 MUX
U15 X->Y G7 G0 10164 05H1 MUX
U16 X->Y G7 G0 10164 14H1 MUX
10 9 7 4 2 1
2 6 5 4 3 11 12 13 14
V 7 6 5 4 3 2 1 0
V 15
48
49
50
51
52
53
-INPUT DATA 48-53 MX1 7

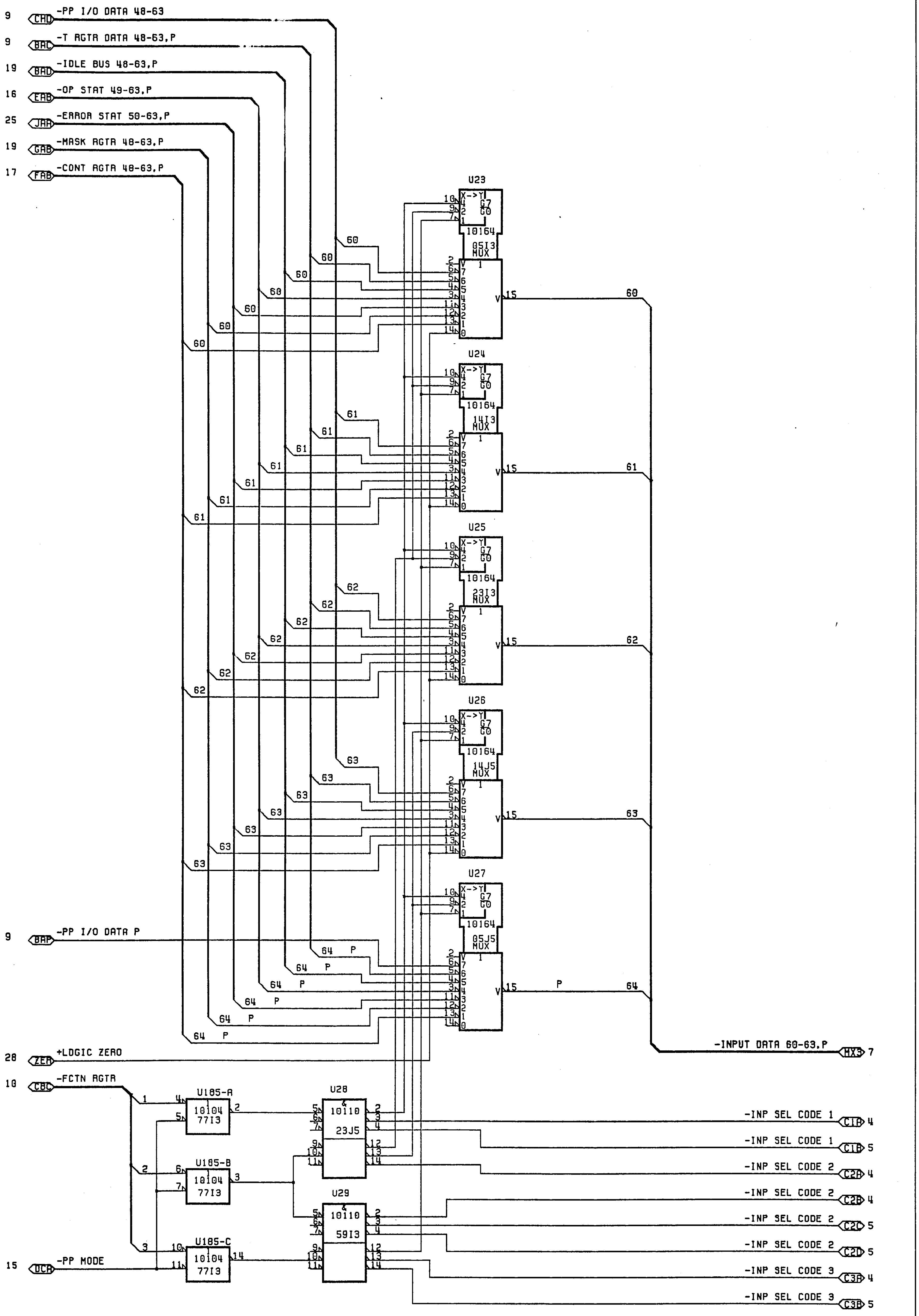
CONTROL DATA	CIO CHANNEL BOARD BAS I/F INPUT DATA MUX BITS 48-53	B	DWG NO. 22105623	DATE 02/28/86	REV A
	TYPE 1JXH	N	SHEET NO. 4	60462210	PAGE JX-04

INPUT DATA MUX BITS 54-59 (3.1)



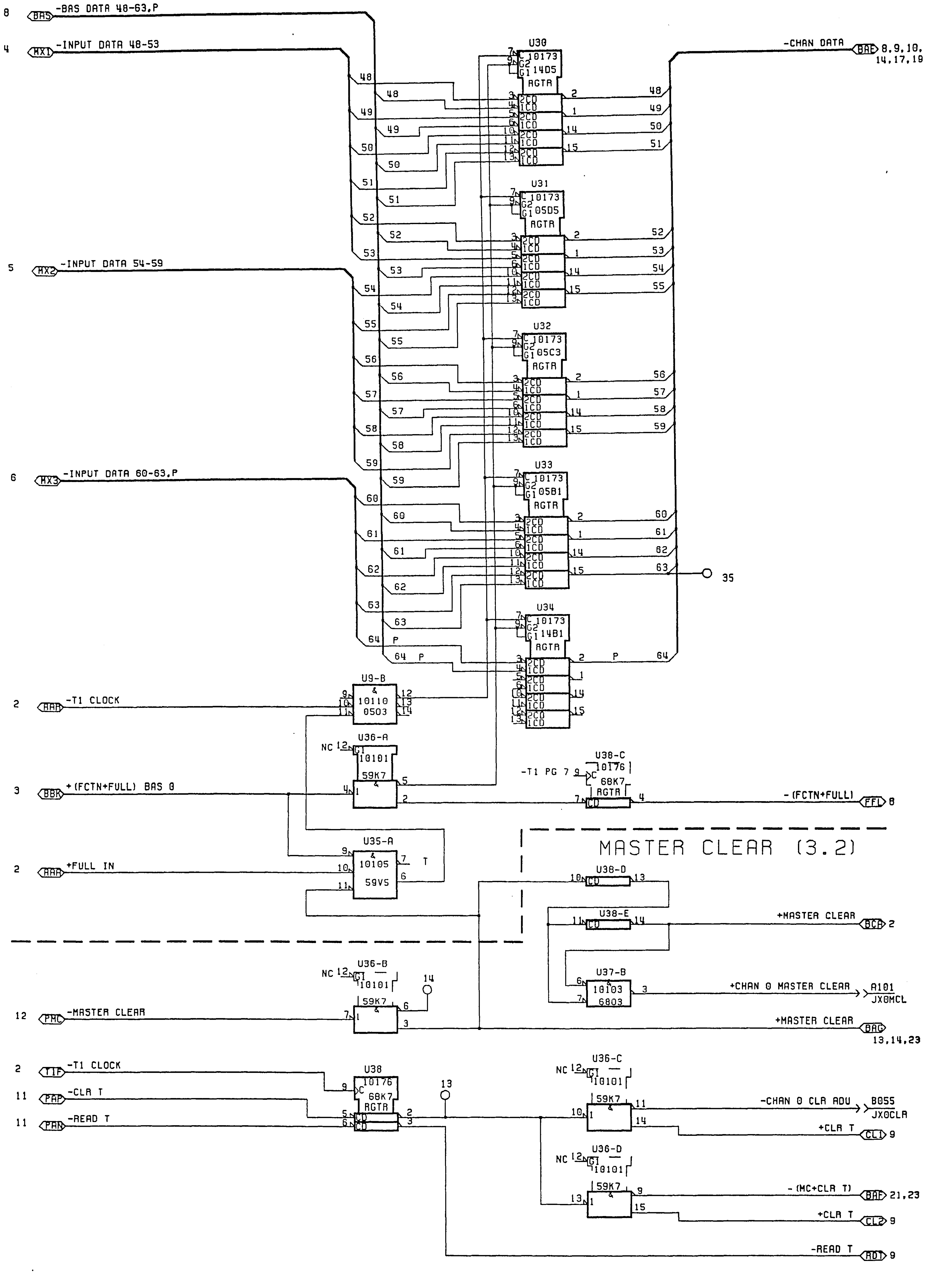
CONTROL DATA	CIO CHANNEL BOARD BAS I/F INPUT DATA MUX BITS 54-59 TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		N	SHEET NO. 5	60462210	PAGE JX-05

INPUT MUX BITS 60-63,PAR (3.1)



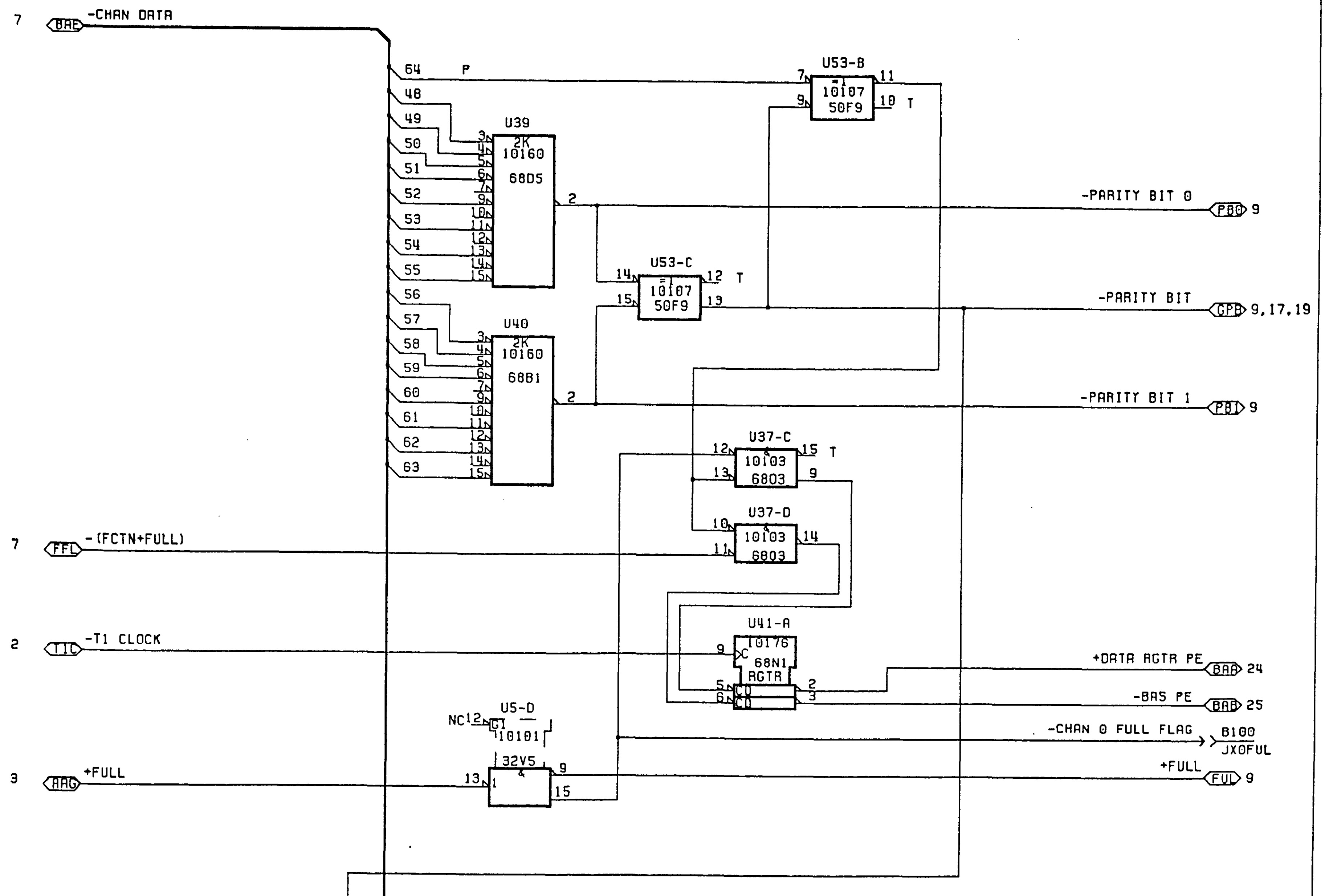
CONTROL DATA	CIO CHANNEL BOARD BAS I/F INPUT MUX BIT 60-63,P TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		SHEET NO. 6	60462210	PAGE JX-86	

CHANNEL DATA REGISTER 48-63 & PAR (3.1)

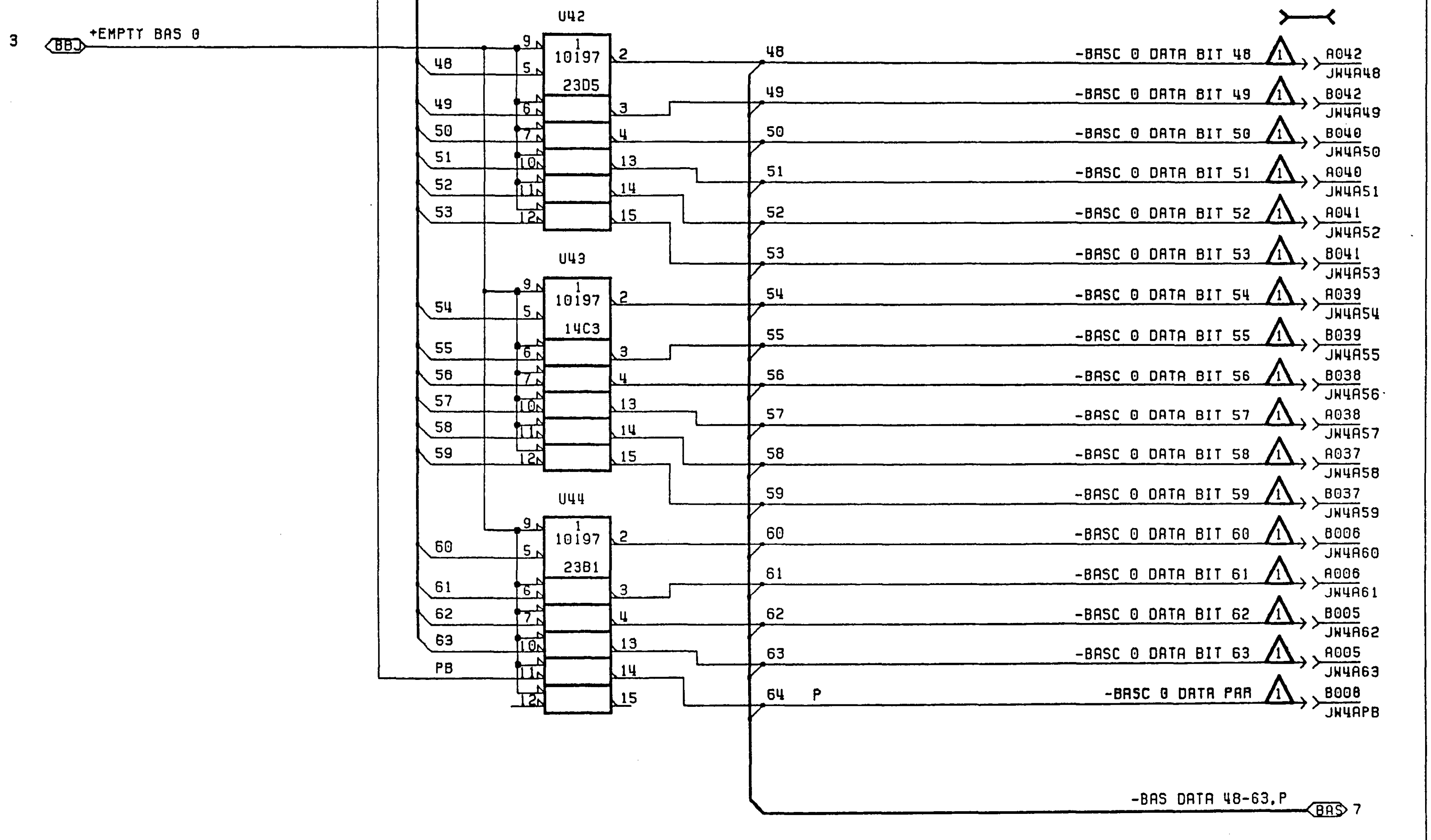


CONTROL DATA	CIO CHANNEL BOARD BAS I/F CHANNEL DATA REGISTER 48-63 & P TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		N	SHEET NO. 7	60462210	PAGE JX-07

DATA RGTR PARITY CHECK AND GEN (3.1)

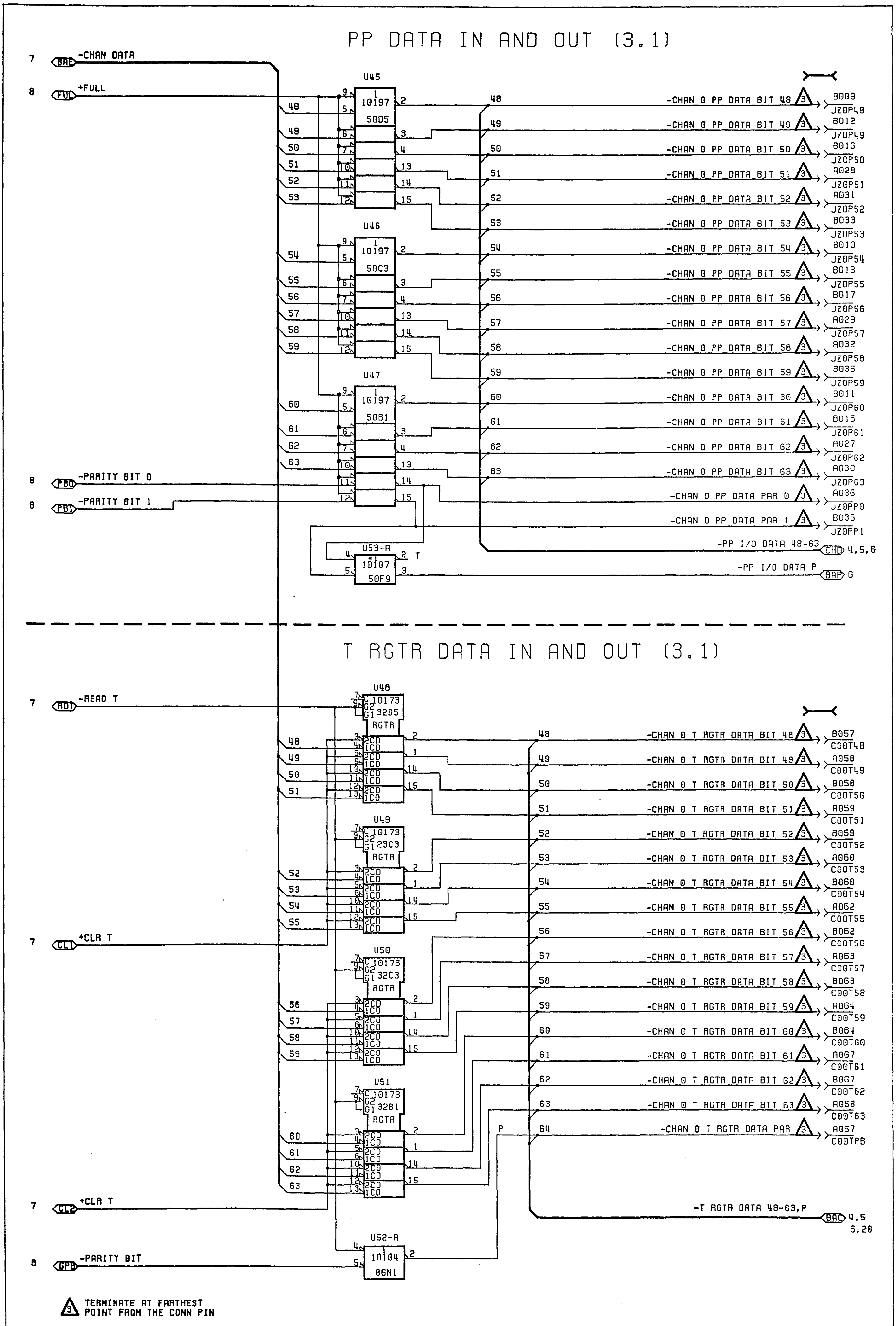


BAS DATA IN AND OUT (3.1)


3 BBJ +EMPTY BAS 0
U42 10197 23D5
U43 10197 14C3
U44 10197 23B1
PB
-BASC 0 DATA BIT 48 A042 JW4A48
-BASC 0 DATA BIT 49 B042 JW4A49
-BASC 0 DATA BIT 50 B040 JW4A50
-BASC 0 DATA BIT 51 A040 JW4A51
-BASC 0 DATA BIT 52 A041 JW4A52
-BASC 0 DATA BIT 53 B041 JW4A53
-BASC 0 DATA BIT 54 A039 JW4A54
-BASC 0 DATA BIT 55 B039 JW4A55
-BASC 0 DATA BIT 56 B038 JW4A56
-BASC 0 DATA BIT 57 A038 JW4A57
-BASC 0 DATA BIT 58 A037 JW4A58
-BASC 0 DATA BIT 59 B037 JW4A59
-BASC 0 DATA BIT 60 B006 JW4A60
-BASC 0 DATA BIT 61 A006 JW4A61
-BASC 0 DATA BIT 62 B005 JW4A62
-BASC 0 DATA BIT 63 A005 JW4A63
64 P -BASC 0 DATA PAR B008 JW4APB
-BAS DATA 48-63,P BAS 7

1 4" MAX LENGTH AND NOT TERMINATED

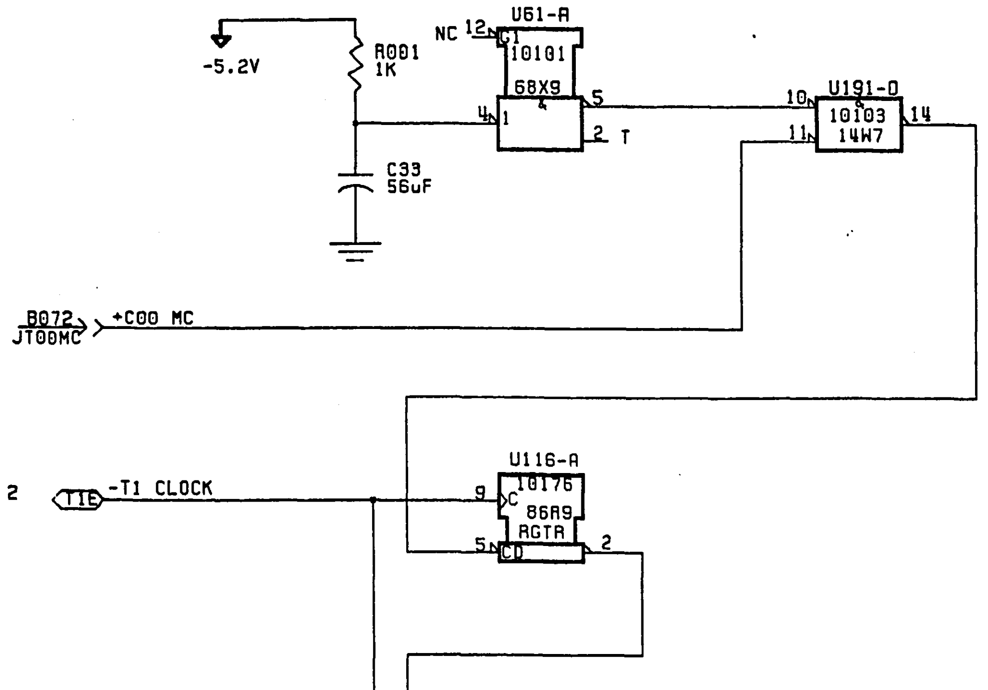
CONTROL DATA	CIO CHANNEL BOARD BAS I/F DATA RGTR PARITY CHECK AND GEN BAS DATA IN AND OUT TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		SHEET NO. 8	60462210	PAGE JX-08	


PP DATA IN AND OUT (3.1)
7 BAE -CHAN DATA
8 FUL +FULL
U45 10197 50D5
U46 10197 50C3
U47 10197 50B1
8 PB0 -PARITY BIT 0
8 PB1 -PARITY BIT 1
U53-A 10107 50F9
-CHAN 0 PP DATA BIT 48 B009 JZ0P48
-CHAN 0 PP DATA BIT 49 B012 JZ0P49
-CHAN 0 PP DATA BIT 50 B016 JZ0P50
-CHAN 0 PP DATA BIT 51 A028 JZ0P51
-CHAN 0 PP DATA BIT 52 A031 JZ0P52
-CHAN 0 PP DATA BIT 53 B033 JZ0P53
-CHAN 0 PP DATA BIT 54 B010 JZ0P54
-CHAN 0 PP DATA BIT 55 B013 JZ0P55
-CHAN 0 PP DATA BIT 56 B017 JZ0P56
-CHAN 0 PP DATA BIT 57 A029 JZ0P57
-CHAN 0 PP DATA BIT 58 A032 JZ0P58
-CHAN 0 PP DATA BIT 59 B035 JZ0P59
-CHAN 0 PP DATA BIT 60 B011 JZ0P60
-CHAN 0 PP DATA BIT 61 B015 JZ0P61
-CHAN 0 PP DATA BIT 62 A027 JZ0P62
-CHAN 0 PP DATA BIT 63 A030 JZ0P63
-CHAN 0 PP DATA PAR 0 A036 JZ0PP0
-CHAN 0 PP DATA PAR 1 B036 JZ0PP1
-PP I/O DATA 48-63 CHD 4,5,6
-PP I/O DATA P BAP 6
T RGTR DATA IN AND OUT (3.1)
7 RDT -READ T
U48 10173 32D5 RGTR
U49 10173 23C3 RGTR
U50 10173 32C3 RGTR
U51 10173 32B1 RGTR
7 CL1 +CLR T
7 CL2 +CLR T
8 GPB -PARITY BIT
U52-A 10104 86N1
-CHAN 0 T RGTR DATA BIT 48 B057 C00T48
-CHAN 0 T RGTR DATA BIT 49 A058 C00T49
-CHAN 0 T RGTR DATA BIT 50 B058 C00T50
-CHAN 0 T RGTR DATA BIT 51 A059 C00T51
-CHAN 0 T RGTR DATA BIT 52 B059 C00T52
-CHAN 0 T RGTR DATA BIT 53 A060 C00T53
-CHAN 0 T RGTR DATA BIT 54 B060 C00T54
-CHAN 0 T RGTR DATA BIT 55 A062 C00T55
-CHAN 0 T RGTR DATA BIT 56 B062 C00T56
-CHAN 0 T RGTR DATA BIT 57 A063 C00T57
-CHAN 0 T RGTR DATA BIT 58 B063 C00T58
-CHAN 0 T RGTR DATA BIT 59 A064 C00T59
-CHAN 0 T RGTR DATA BIT 60 B064 C00T60
-CHAN 0 T RGTR DATA BIT 61 A067 C00T61
-CHAN 0 T RGTR DATA BIT 62 B067 C00T62
-CHAN 0 T RGTR DATA BIT 63 A068 C00T63
-CHAN 0 T RGTR DATA PAR A057 C00TPB
-T RGTR DATA 48-63,P BAC 4,5 6,20

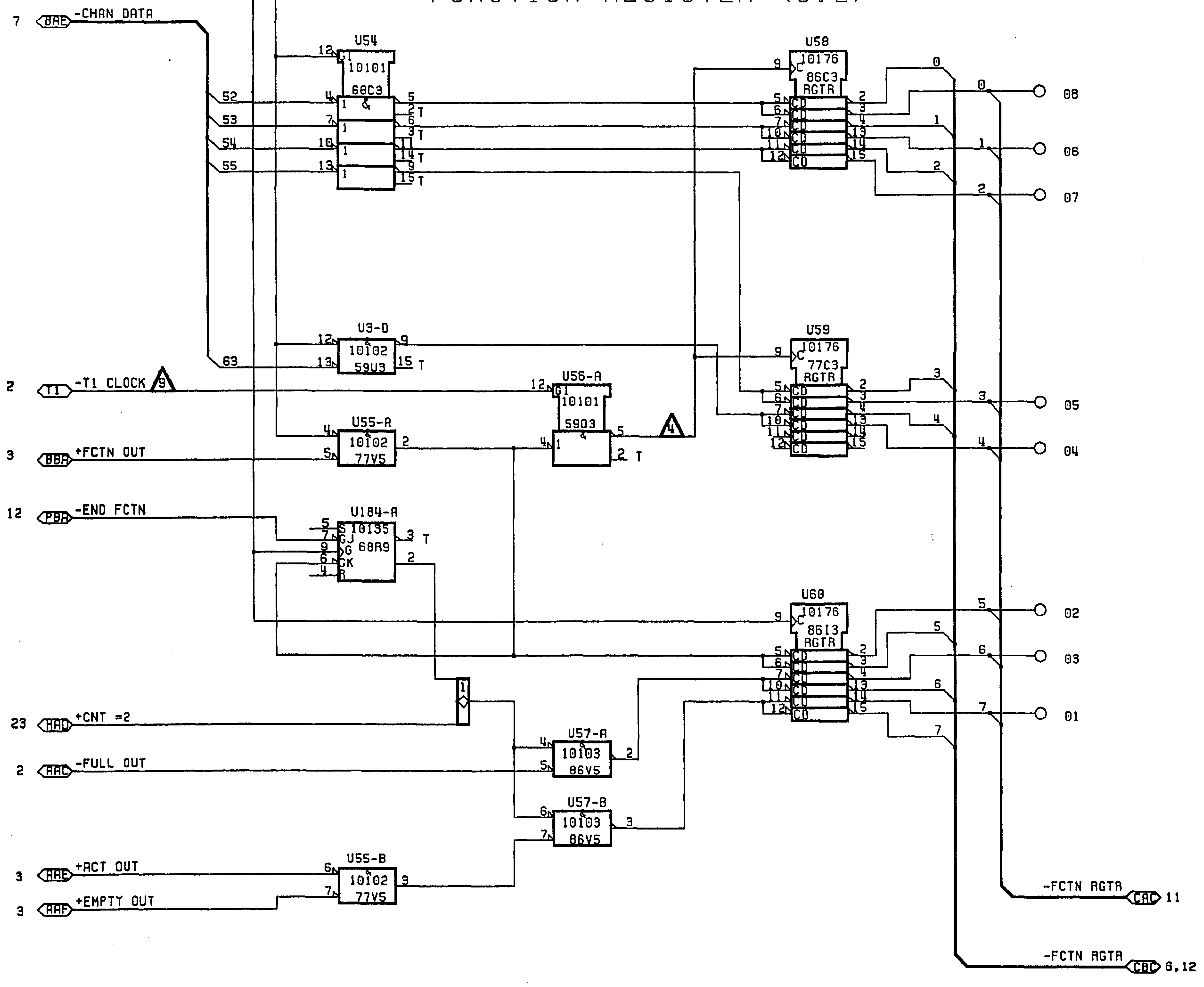
3 TERMINATE AT FARTHEST POINT FROM THE CONN PIN

CONTROL DATA	CIO CHANNEL BOARD BAS I/F CHAN DATA IN AND OUT T RGTR DATA IN AND OUT TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
			SHEET NO. 9	60462210	PAGE JX-09

POWER ON MASTER CLEAR (3.2)



FUNCTION REGISTER (3.2)

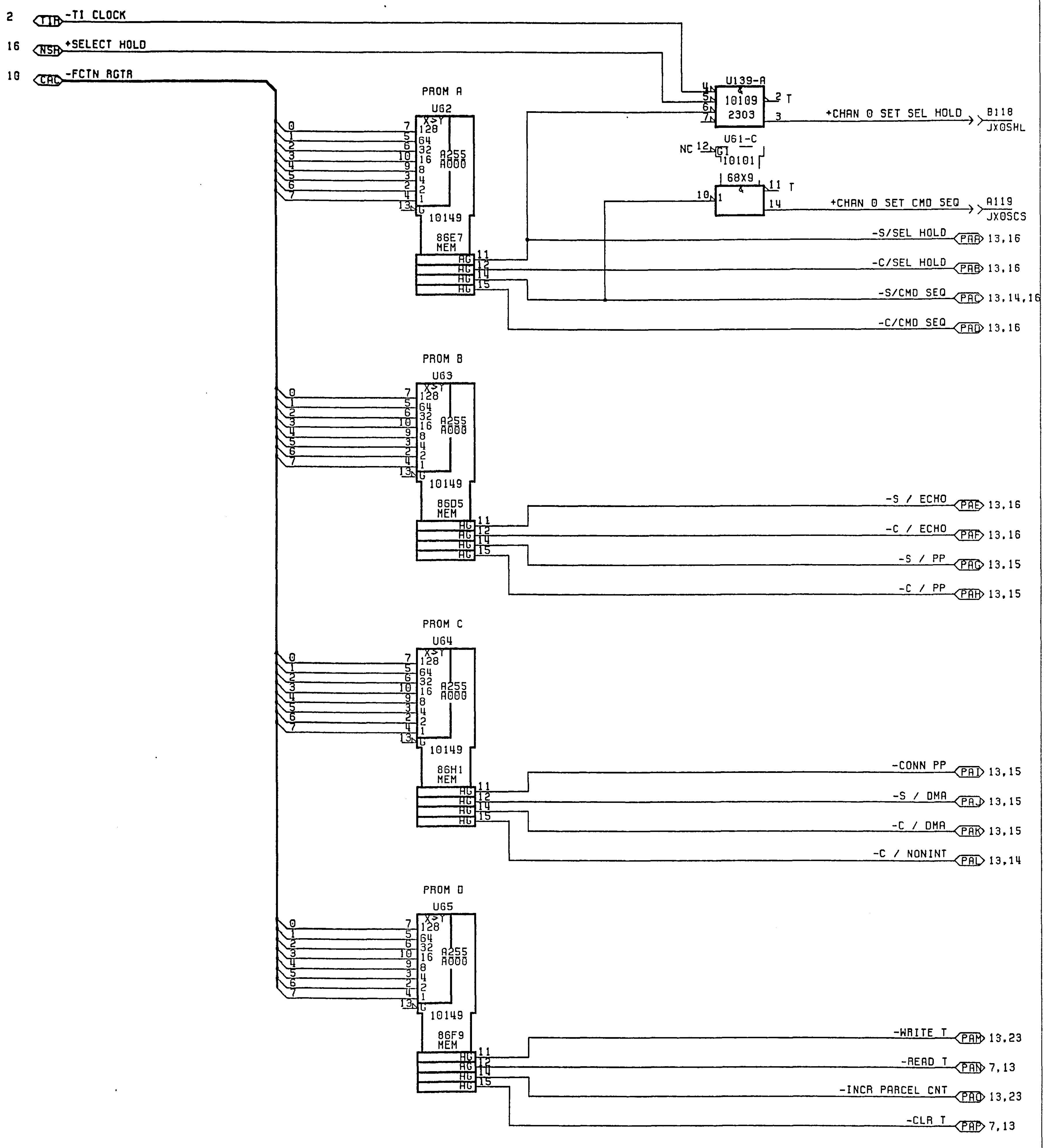


4 12" MAX LENGTH

9 7" MAX LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F FUNCTION REGISTER POWER ON MASTER CLEAR TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
	N	SHEET NO. 10	60462210	PAGE JX-10	

FUNCTION DECODE PROMS A-D (3.2)



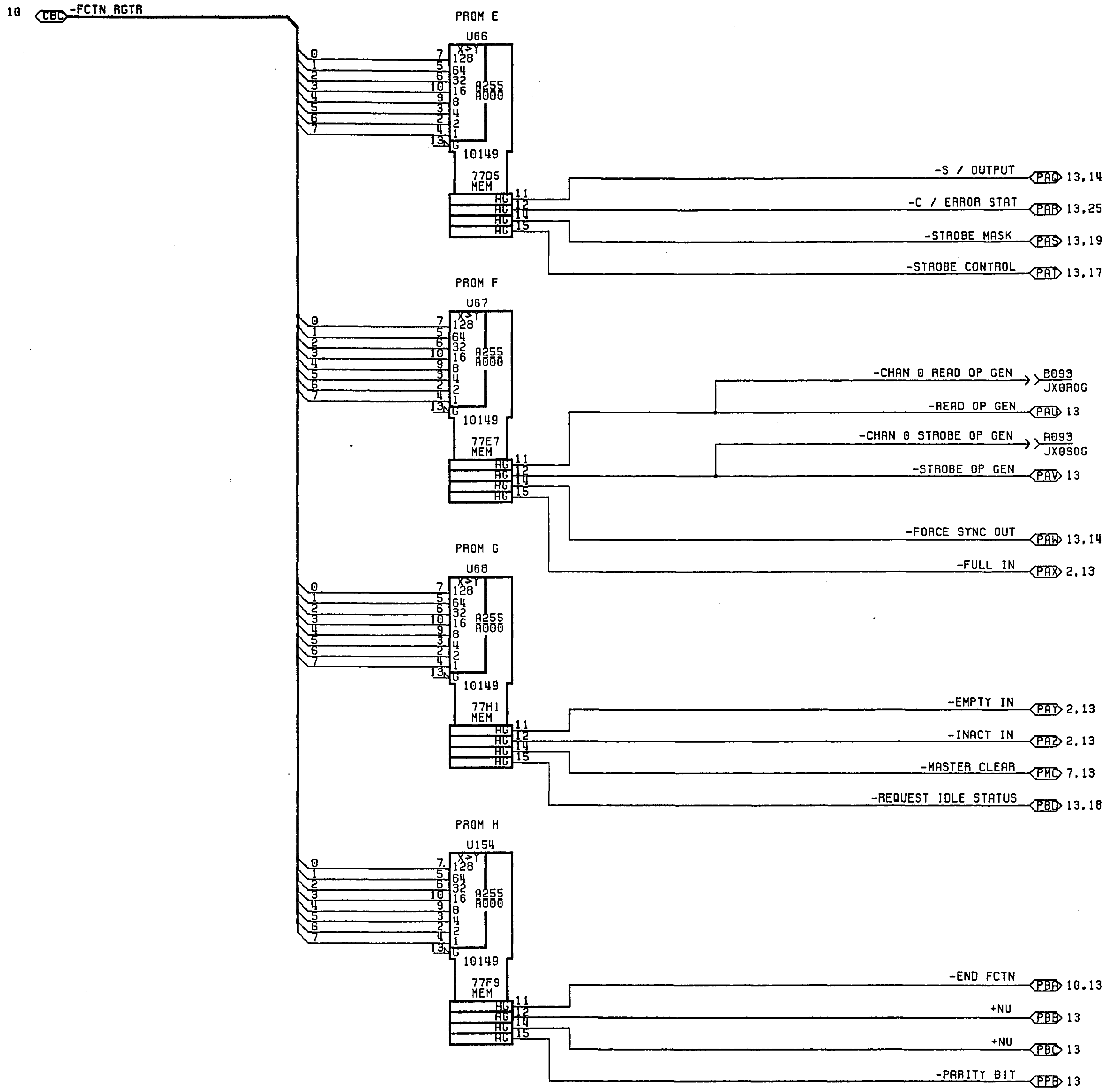
CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FUNCTION DECODE PROMS A-D

TYPE 1JXH

B	DWG NO. 22185623	DATE 02/28/86	REV A
SHEET NO. 11	60462210	PAGE JX-11	

FUNCTION DECODE PROMS E-H (3.2)



CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FUNCTION DECODE PROMS E-H
TYPE 1JXH

N

B

DWG NO. 22105623

DATE 02/28/86

REV A

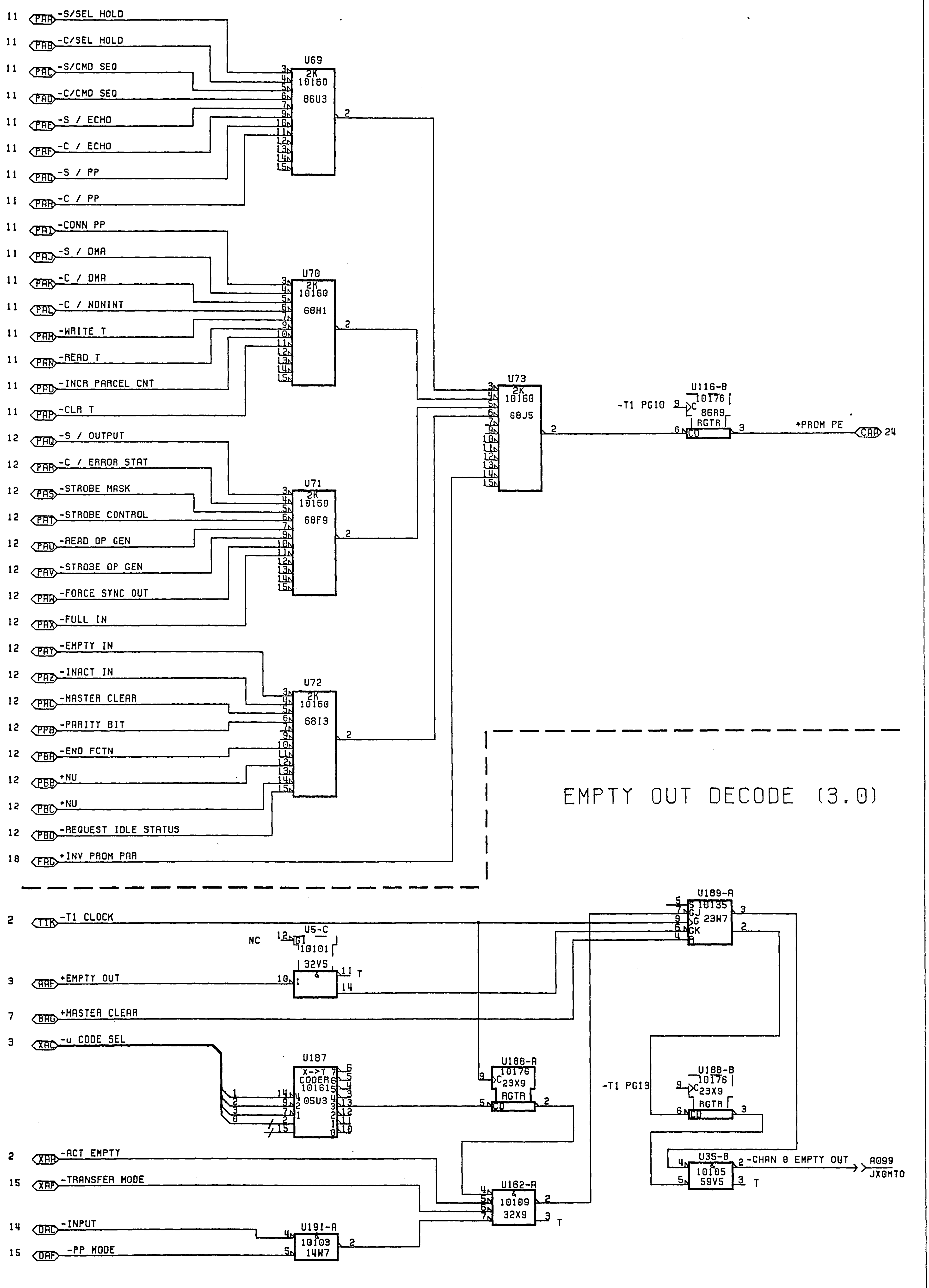
SHEET NO. 12

60462210

PAGE JX-12

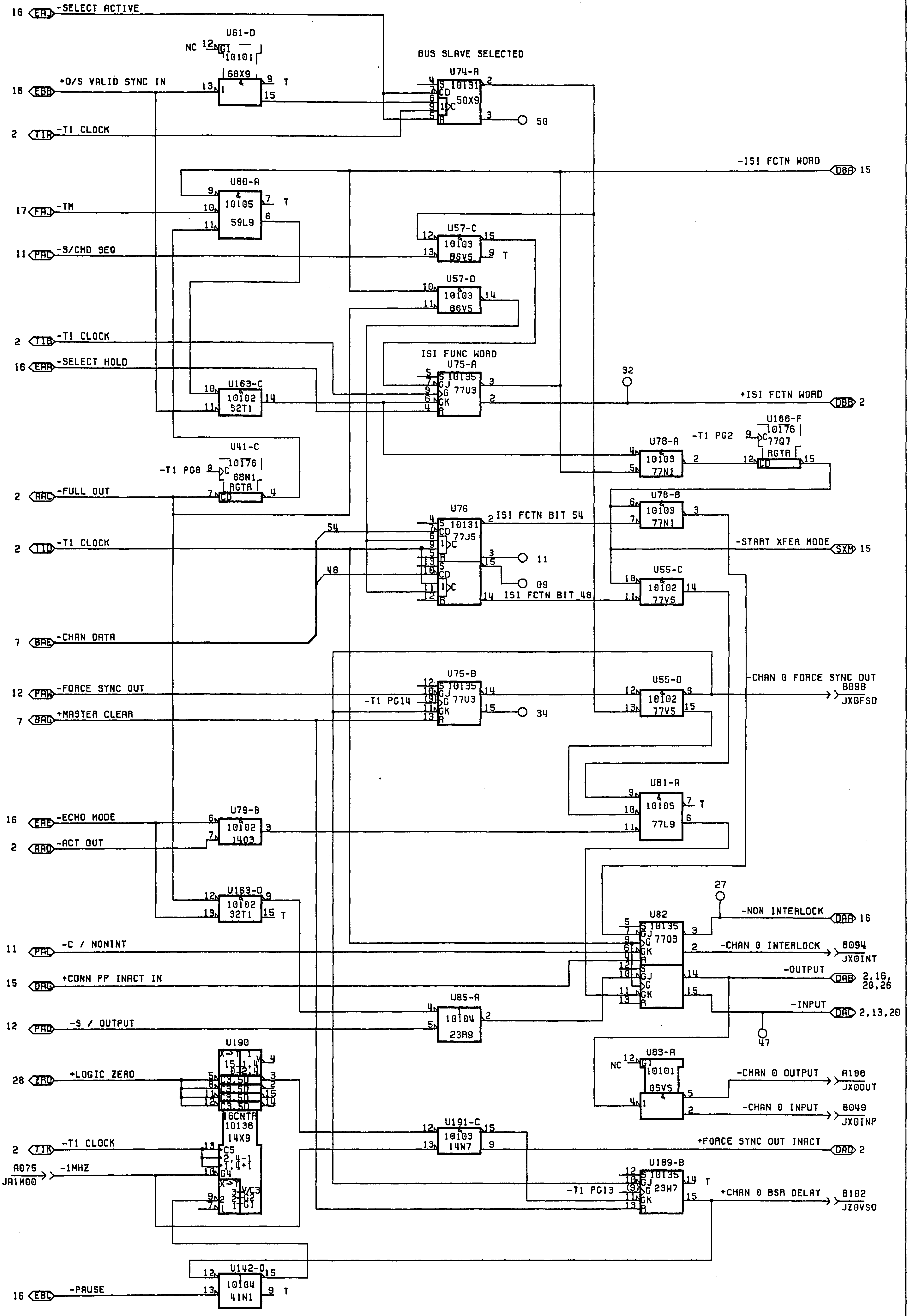
PROM PARITY CHECK (3.2)

EMPTY OUT DECODE (3.0)



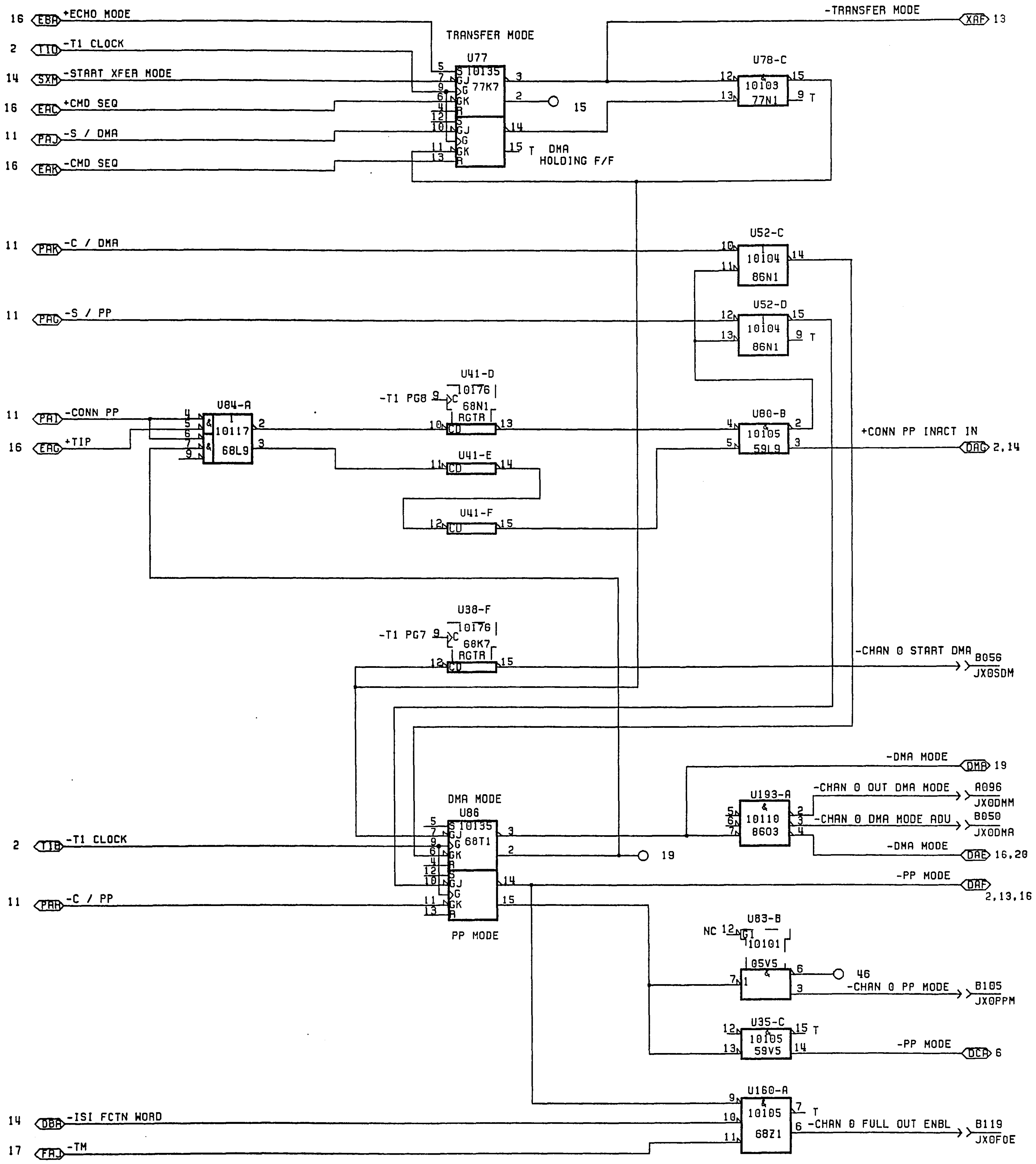
CONTROL DATA	CIO CHANNEL BOARD BAS I/F PROM PARITY CHECK EMPTY OUT DECODE TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		N	SHEET NO. 13	60462210	PAGE JX-13

ADAPTER INTERLOCK/OUTPUT MODE REGISTERS (3.3)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F ADAPTER NONINTERLOCK/OUTPUT MODE REGISTERS TYPE 1JXH	B	DWG NO. 22105623	DATE 07/07/86	REV B
		N	SHEET NO. 14	60462210	PAGE JX-14

ADAPTER PP/DMA MODE REGISTERS (3.3)

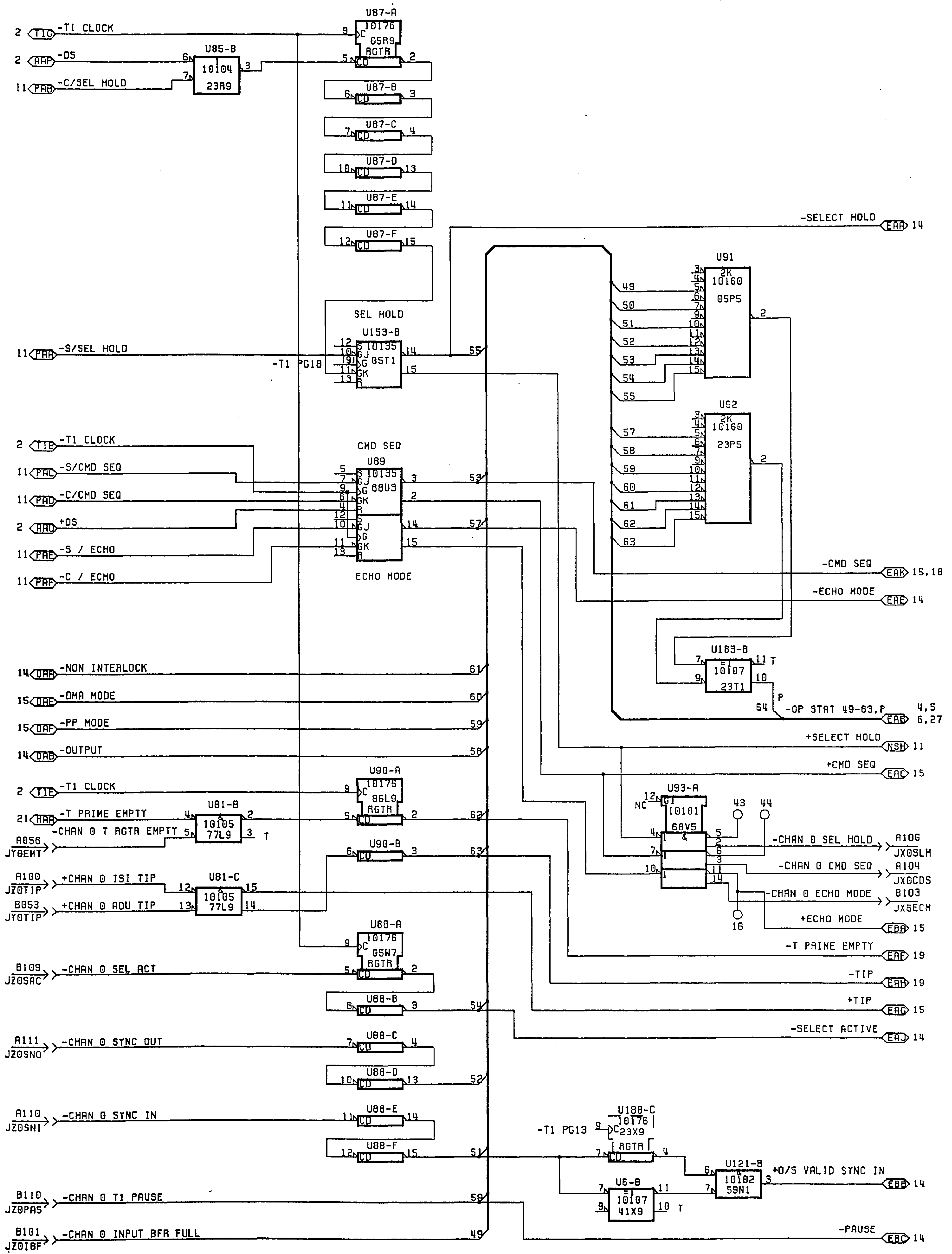


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
ADAPTER PP / DMA
MODE REGISTERS
TYPE 1JXH

B	DWG NO. 22105623	DATE 02/28/86	REV A
SHEET NO. 15	60462210	PAGE JX-15	

OPERATIONAL STATUS NETWORK (3.7)

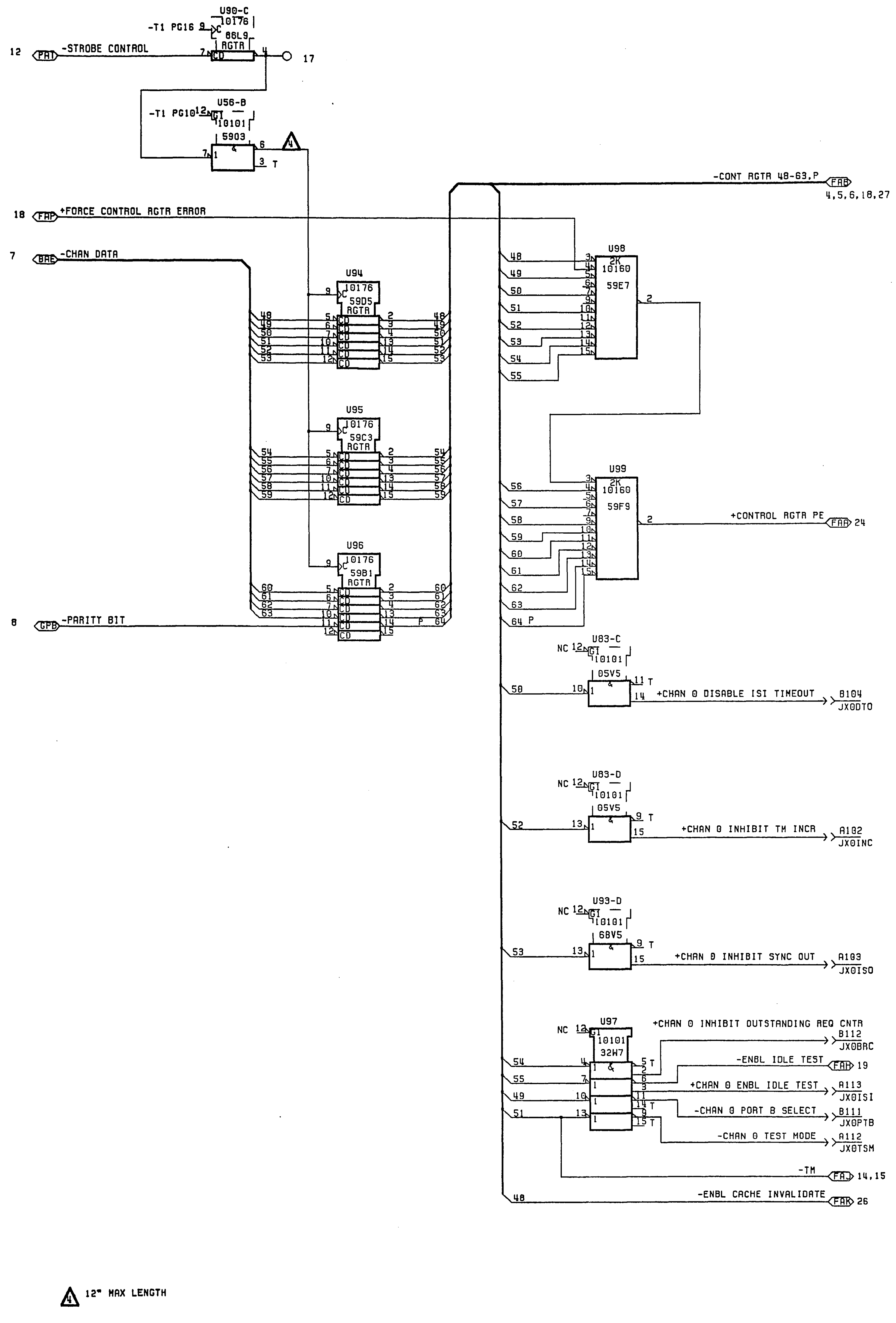


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
OPERATIONAL STATUS NETWORK
TYPE 1JXH

B	DWG NO. 22105623	DATE 02/28/86	REV A
SHEET NO. 16	60462210	PAGE JX-16	

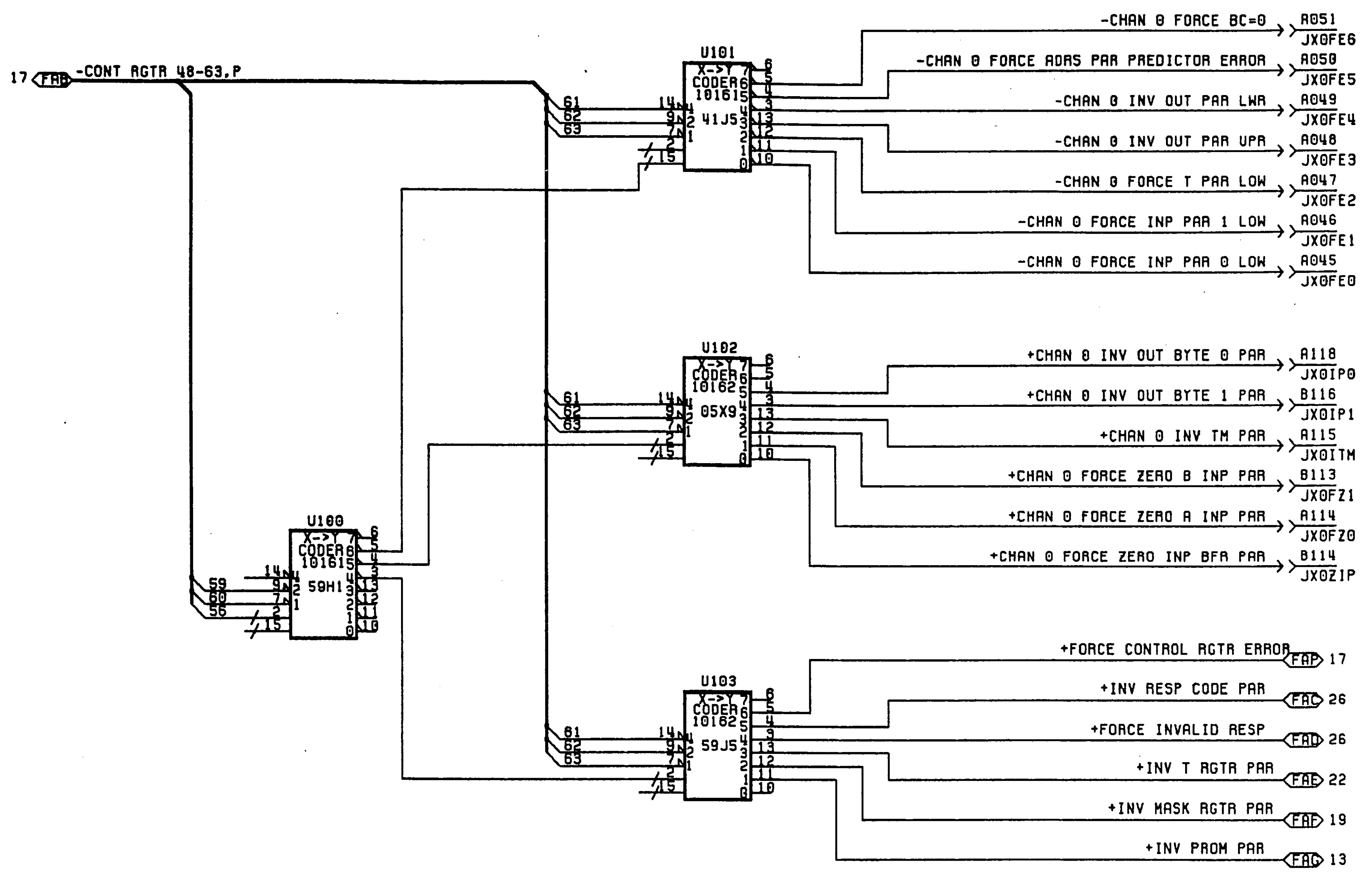
CONTROL REGISTERS (3.4)



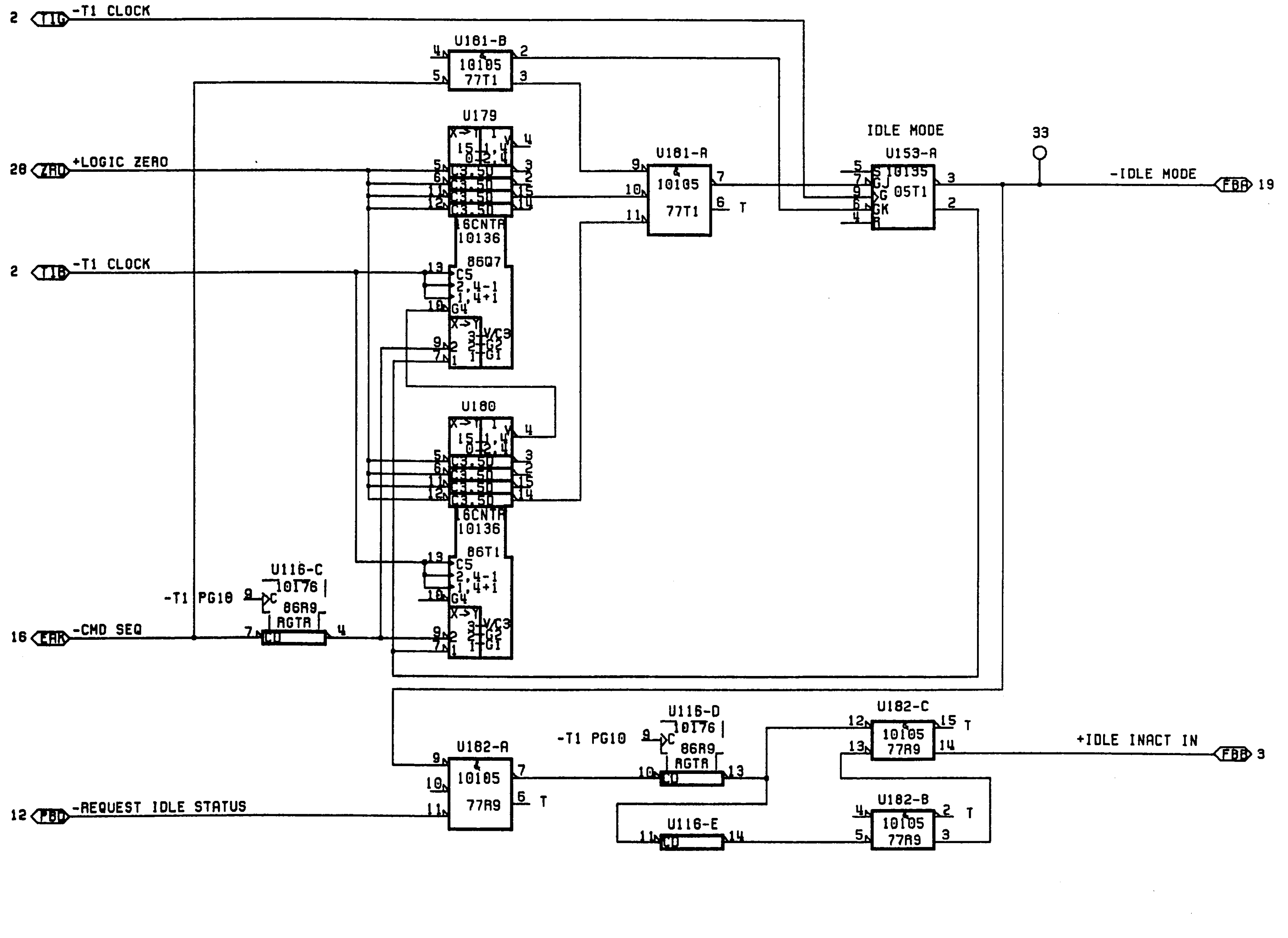
4 12" MAX LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F CONTROL REGISTER TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		SHEET NO. 17	60462210	PAGE JX-17	

FORCE ERROR DECODERS (3.4)


17 FAB -CONT RGTR 48-63,P
U101
X->Y
CODER
10161
41J53
U102
CODER
10162
05X9
U100
CODER
10161
59H1
U103
CODER
10162
59J5
-CHAN 0 FORCE BC=0 A051 JX0FE6
-CHAN 0 FORCE ADRS PAR PREDICTOR ERROR A050 JX0FE5
-CHAN 0 INV OUT PAR LWR A049 JX0FE4
-CHAN 0 INV OUT PAR UPR A048 JX0FE3
-CHAN 0 FORCE T PAR LOW A047 JX0FE2
-CHAN 0 FORCE INP PAR 1 LOW A046 JX0FE1
-CHAN 0 FORCE INP PAR 0 LOW A045 JX0FE0
+CHAN 0 INV OUT BYTE 0 PAR A118 JX0IP0
+CHAN 0 INV OUT BYTE 1 PAR B116 JX0IP1
+CHAN 0 INV TM PAR A115 JX0ITM
+CHAN 0 FORCE ZERO B INP PAR B113 JX0FZ1
+CHAN 0 FORCE ZERO A INP PAR A114 JX0FZ0
+CHAN 0 FORCE ZERO INP BFR PAR B114 JX0ZIP
+FORCE CONTROL RGTR ERROR FAP 17
+INV RESP CODE PAR FAC 26
+FORCE INVALID RESP FAD 26
+INV T RGTR PAR FAE 22
+INV MASK RGTR PAR FAF 19
+INV PROM PAR FAG 13
61
62
63
59
60
56

IDLE MODE DELAY (3.4)

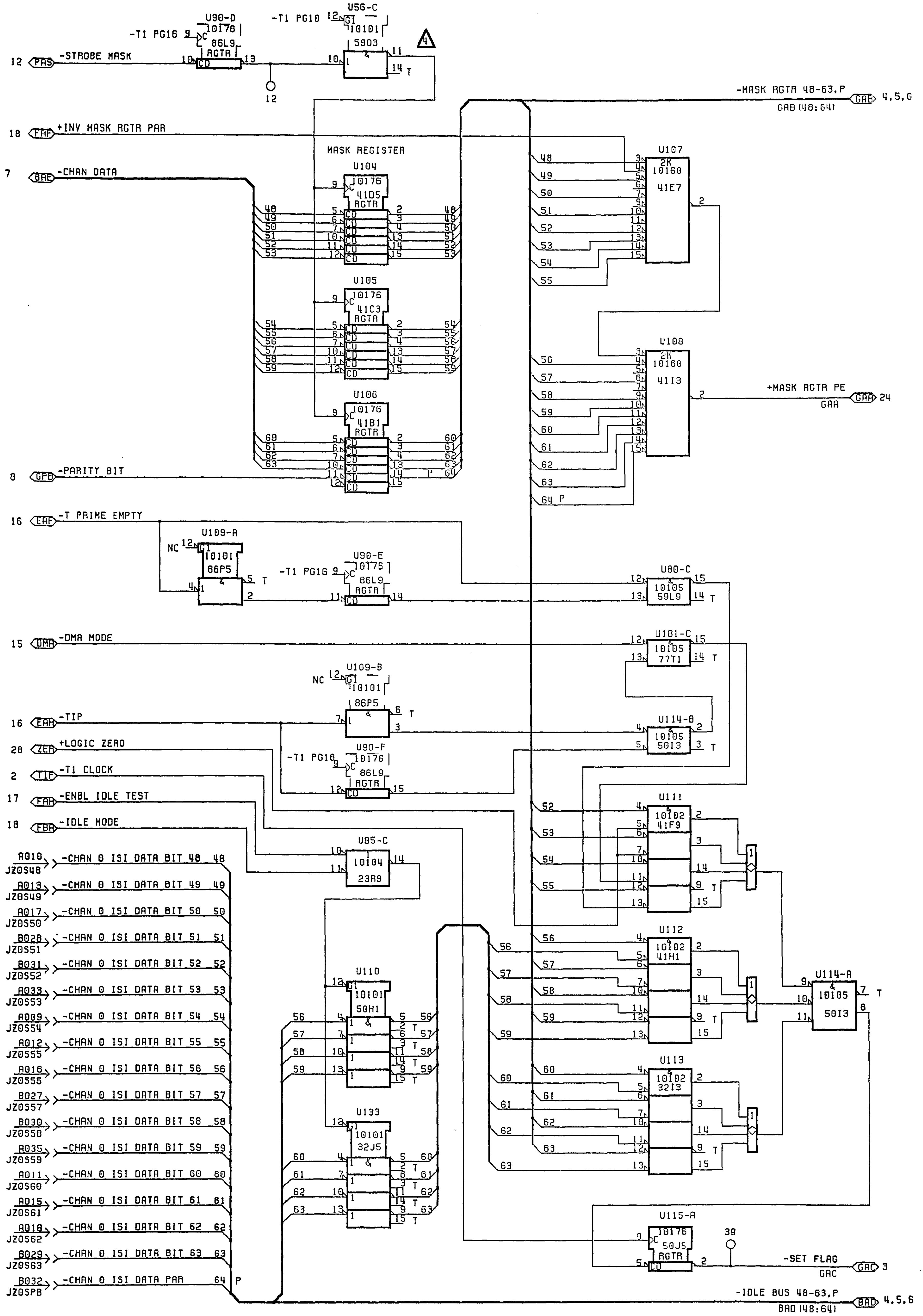


CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FORCE ERROR DECODERS
IDLE MODE DELAY
TYPE 1JXH

B
DWG NO. 22105623
DATE 07/07/86
REV B
SHEET NO. 18 60462210 PAGE JX-18

FLAG MASK NETWORK (3.4)



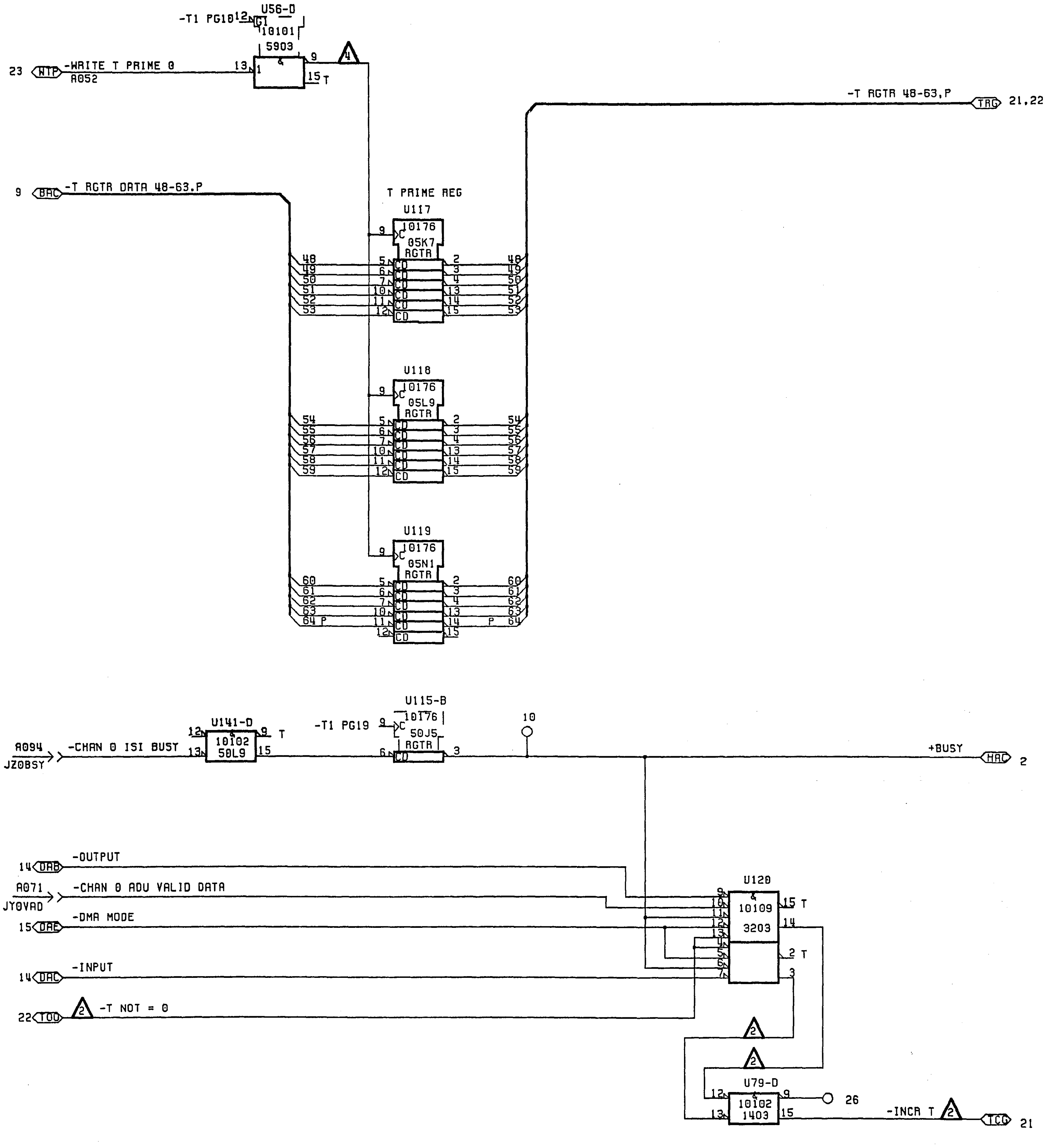
4 12 INCH MAX LENGTH

CONTROL DATA

CIO CHANNEL BOARD BAS I/F
FLAG MASK NETWORK
TYPE 1JXH

	DWG NO.	DATE	REV
B	22105623	02/28/86	A
SHEET NO. 19	60462210	PAGE JX-19	

T PRIME REGISTER (3.5)

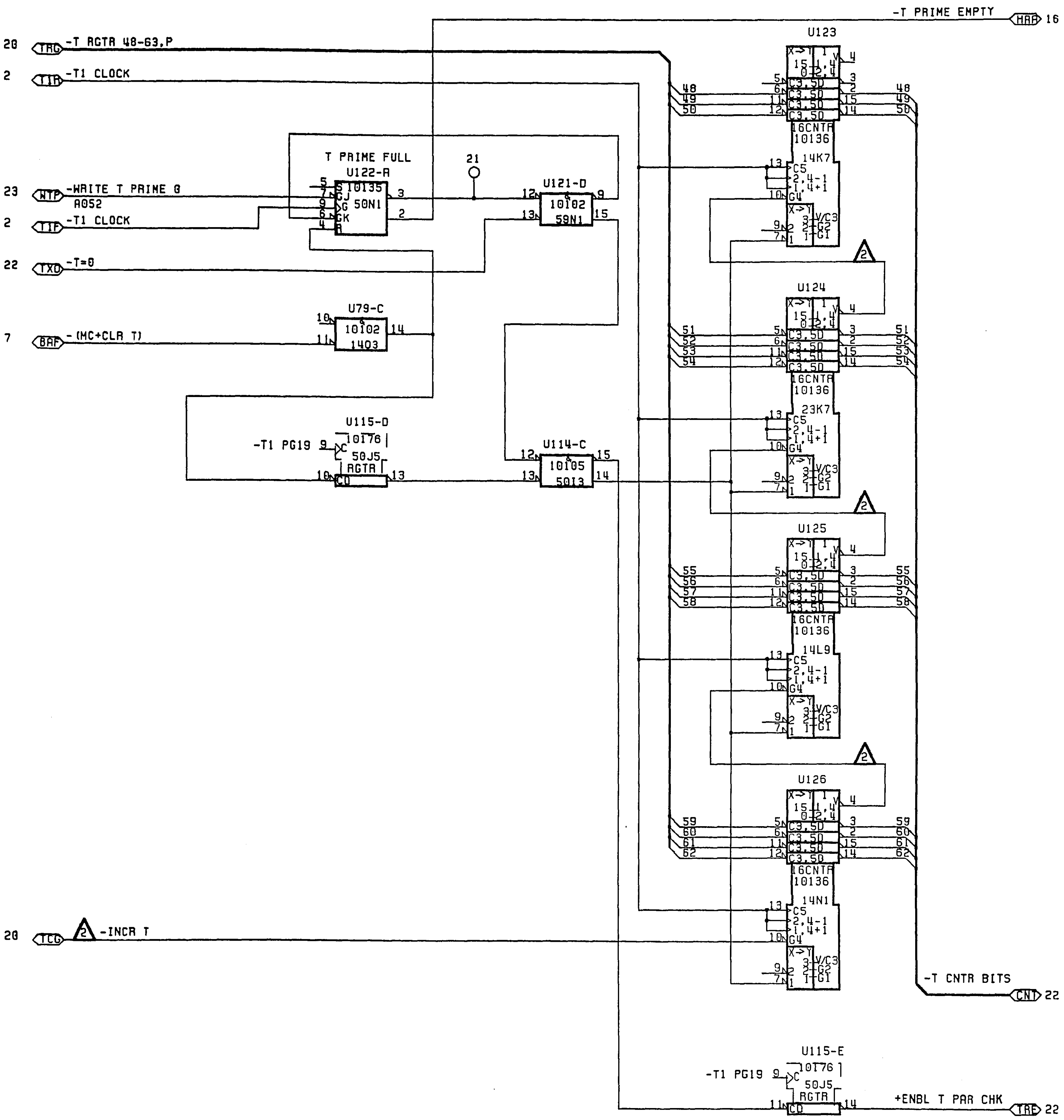


2" MAXIMUM LENGTH

12" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD BAS I/F T PRIME REGISTER TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		SHEET NO. 20	60462210	PAGE JX-20	

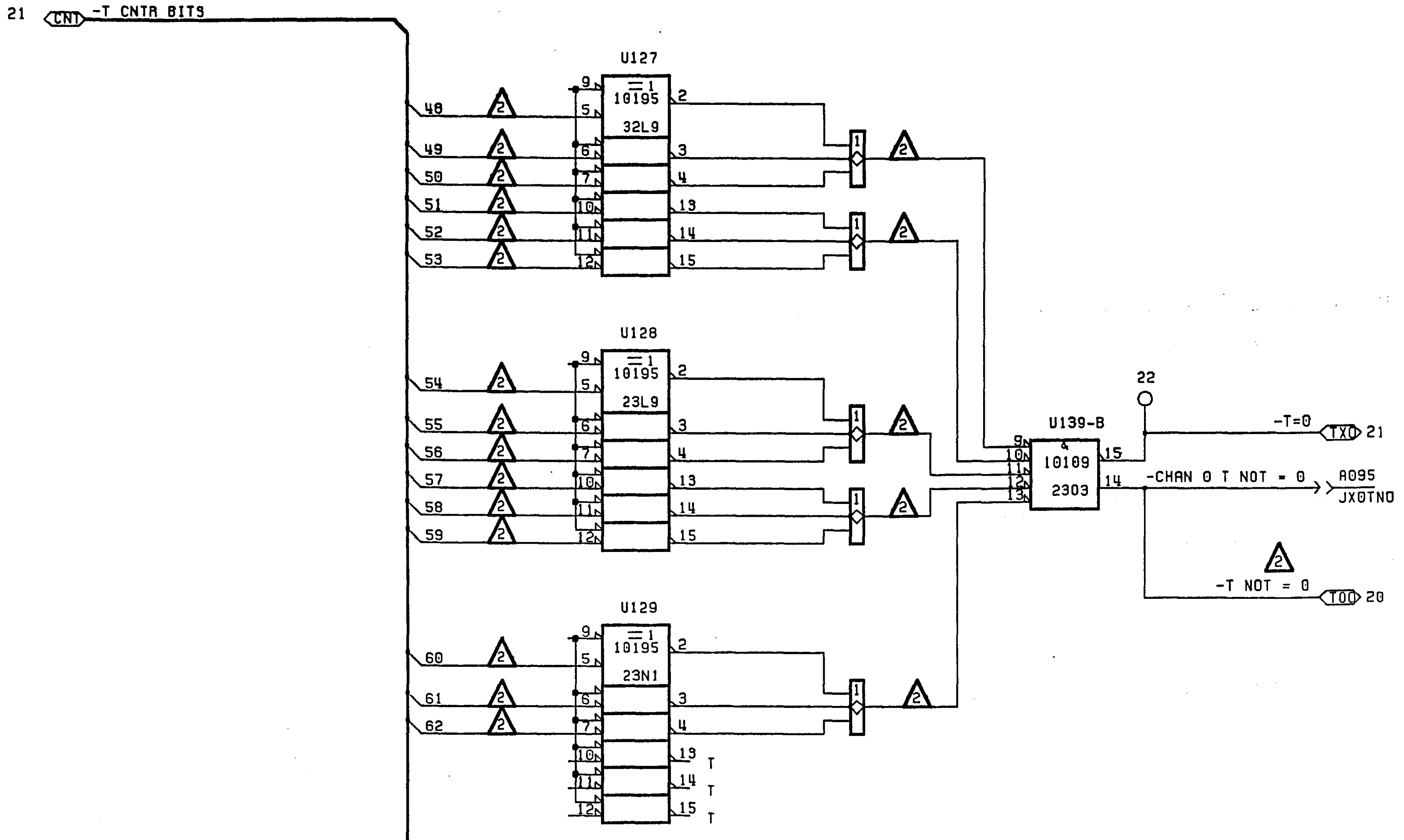
T RGTR COUNTER (3.5)



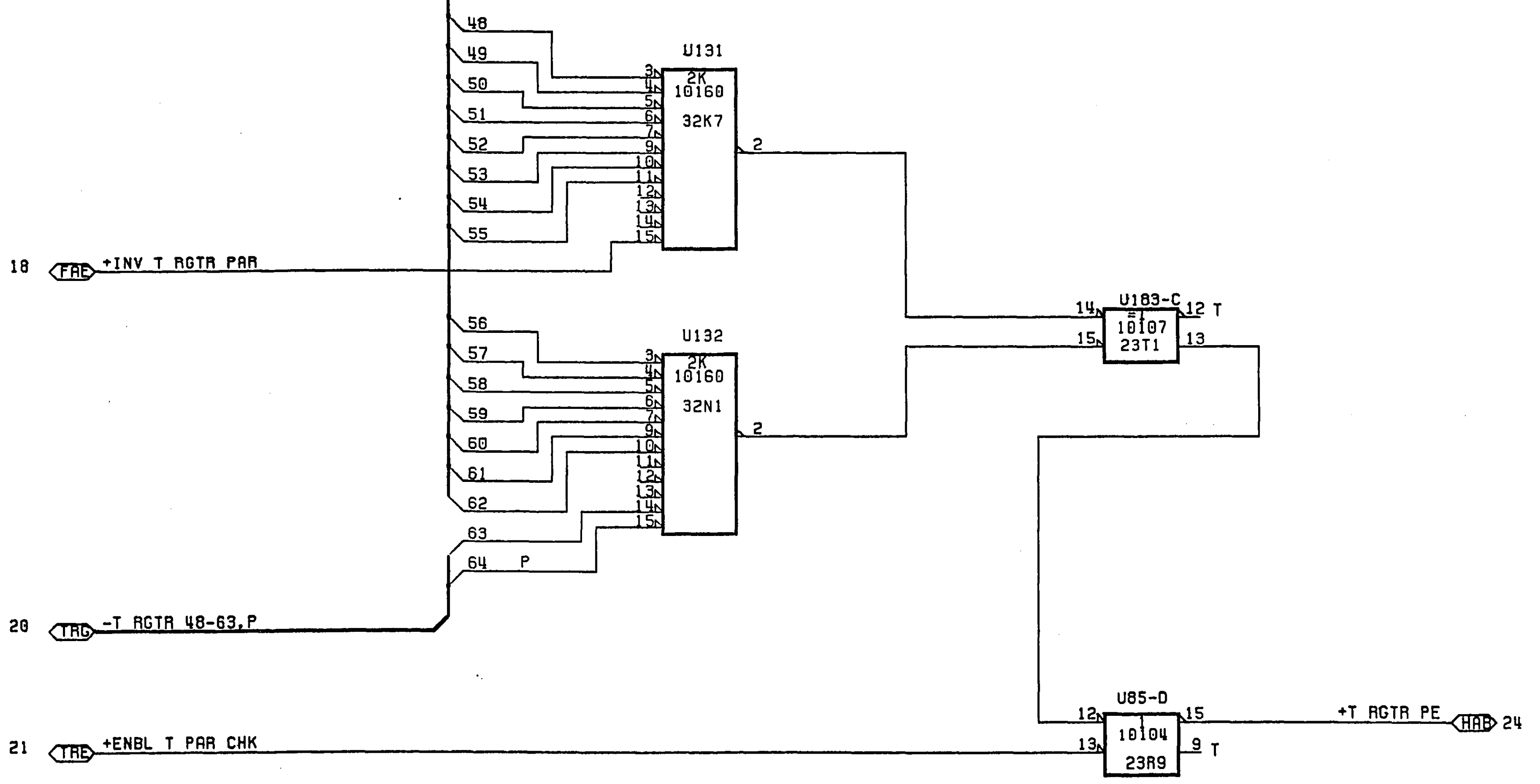
2" MAXIMUN LENGTH

CONTROL DATA
CIO CHANNEL BOARD BAS I/F
T RGTR COUNTER
TYPE 1JXH
B
DWG NO. 22105623
DATE 02/28/86
REV A
SHEET NO. 21
60462210
PAGE JX-21

T RGTR ZERO TEST (3.5)



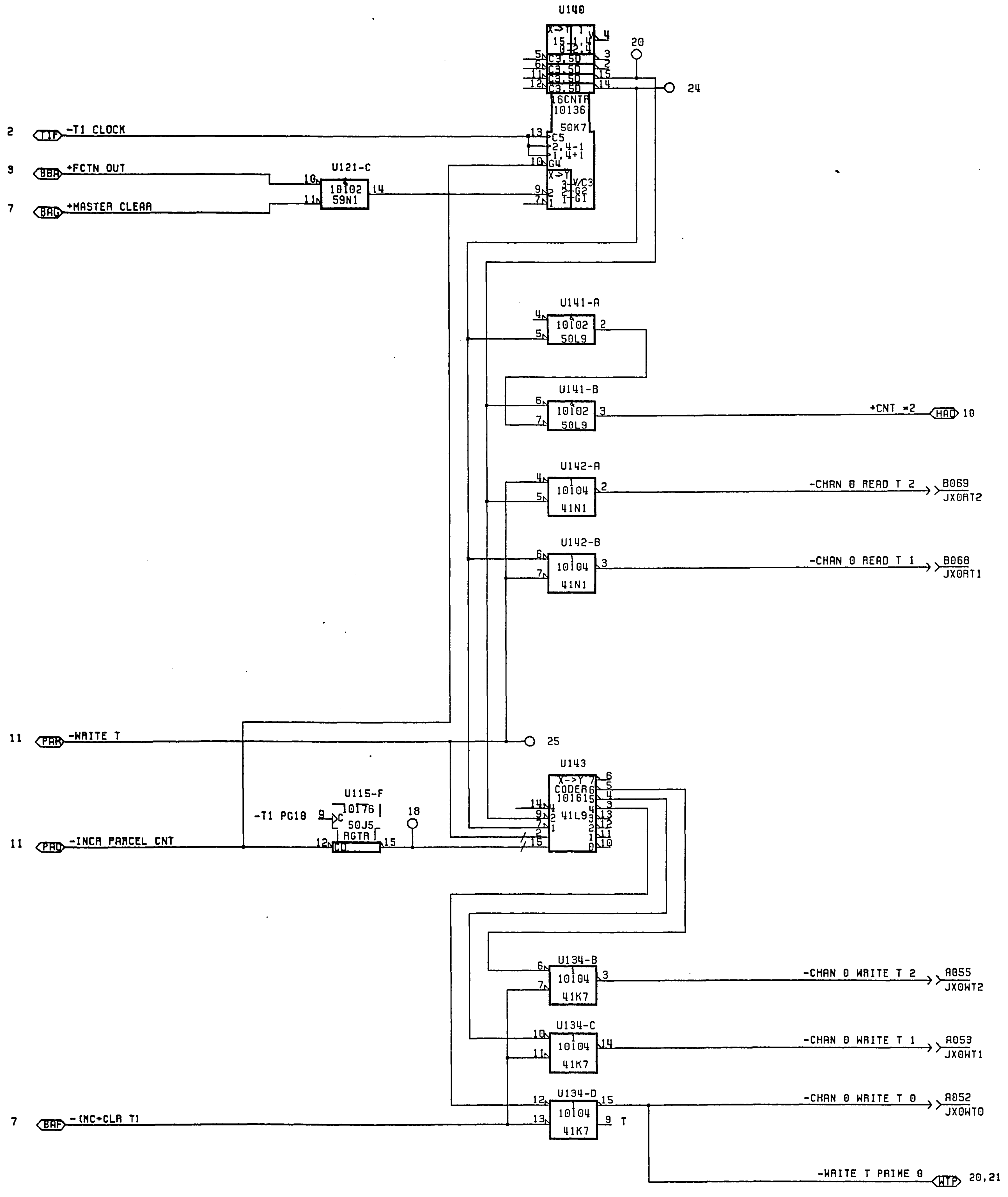
T RGTR PARITY CHECK (3.5)



△2 2" MAXIMUM LENGTH

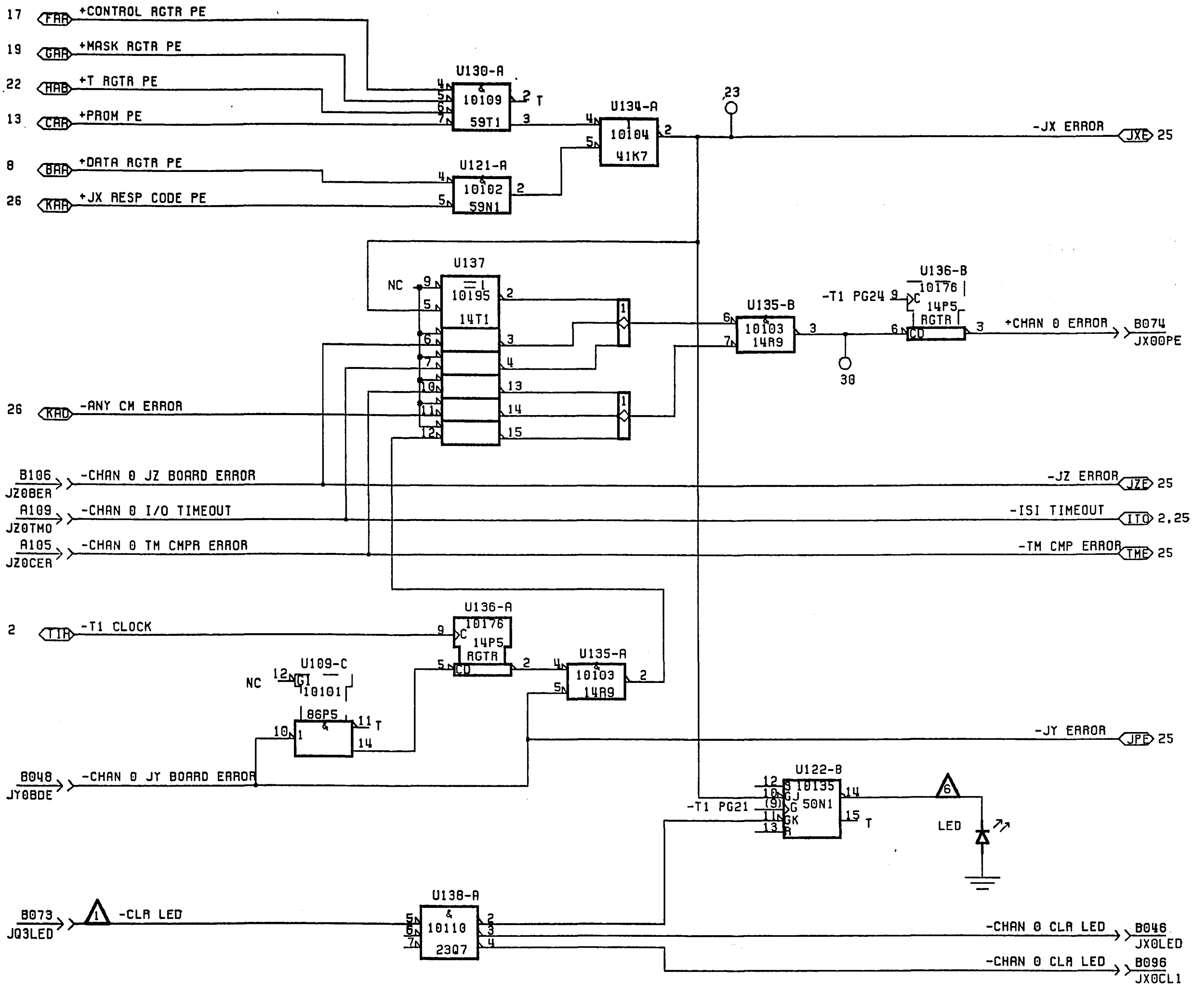
CONTROL DATA	CIO CHANNEL BOARD BAS I/F T RGTR ZERO TEST & PARITY CHECK	B	DWG NO. 22105623	DATE 02/28/86	REV A
	TYPE 1JXH N	SHEET NO. 22	60462210	PAGE JX-22	

T RGTR PARCEL COUNTER (3.5)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F T REGISTER PARCEL COUNTER TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
	N	SHEET NO. 23	60462210	PAGE JX-23	

ERROR STATUS NETWORK (3.6)



RESERVED FOR FUTURE USE

A061 OPEN RESERVED FOR +5V
B061 OPEN RESERVED FOR +5V
A070 OPEN RESERVED FOR +5V
B070 OPEN RESERVED FOR +5V

A008 RESV20 RESERVED FOR FUTURE USE
A078 RESV30 RESERVED FOR FUTURE USE
A079 JYBC00 RESERVED FOR FUTURE USE
A080 OPEN RESERVED FOR FUTURE USE
A081 OPEN RESERVED FOR FUTURE USE
A082 OPEN RESERVED FOR FUTURE USE
A083 OPEN RESERVED FOR FUTURE USE
A084 OPEN RESERVED FOR FUTURE USE
A085 OPEN RESERVED FOR FUTURE USE
A086 OPEN RESERVED FOR FUTURE USE
A088 OPEN RESERVED FOR FUTURE USE
A121 OPEN RESERVED FOR FUTURE USE

B076 OPEN RESERVED FOR FUTURE USE
B078 OPEN RESERVED FOR FUTURE USE
B079 OPEN RESERVED FOR FUTURE USE
B080 OPEN RESERVED FOR FUTURE USE
B081 OPEN RESERVED FOR FUTURE USE
B082 OPEN RESERVED FOR FUTURE USE
B083 OPEN RESERVED FOR FUTURE USE
B084 OPEN RESERVED FOR FUTURE USE
B085 OPEN RESERVED FOR FUTURE USE
B086 RESV10 RESERVED FOR FUTURE USE
B088 OPEN RESERVED FOR FUTURE USE

A019 OPEN RESERVED FOR FUTURE USE
A020 OPEN RESERVED FOR FUTURE USE
A021 OPEN RESERVED FOR FUTURE USE
A022 OPEN RESERVED FOR FUTURE USE
A023 OPEN RESERVED FOR FUTURE USE
A025 OPEN RESERVED FOR FUTURE USE
A026 OPEN RESERVED FOR FUTURE USE

B018 OPEN RESERVED FOR FUTURE USE
B019 OPEN RESERVED FOR FUTURE USE
B020 OPEN RESERVED FOR FUTURE USE
B021 OPEN RESERVED FOR FUTURE USE
B022 OPEN RESERVED FOR FUTURE USE
B023 OPEN RESERVED FOR FUTURE USE
B025 OPEN RESERVED FOR FUTURE USE
B026 OPEN RESERVED FOR FUTURE USE

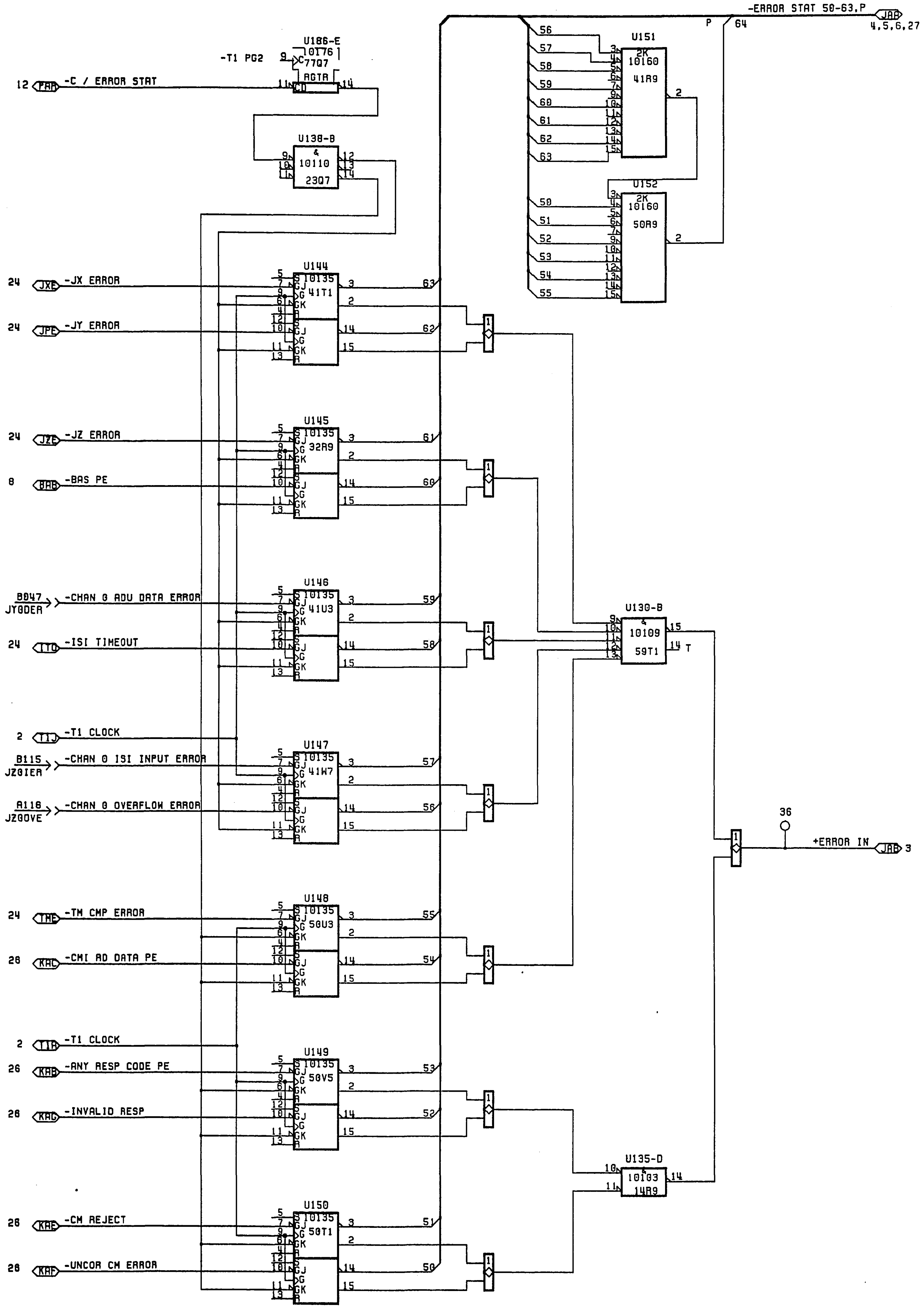
A092 OPEN RESERVED FOR FUTURE USE
B092 OPEN RESERVED FOR FUTURE USE

⚠1 3" MAX LENGTH AND NOT TERMINATED

⚠6 TERMINATE

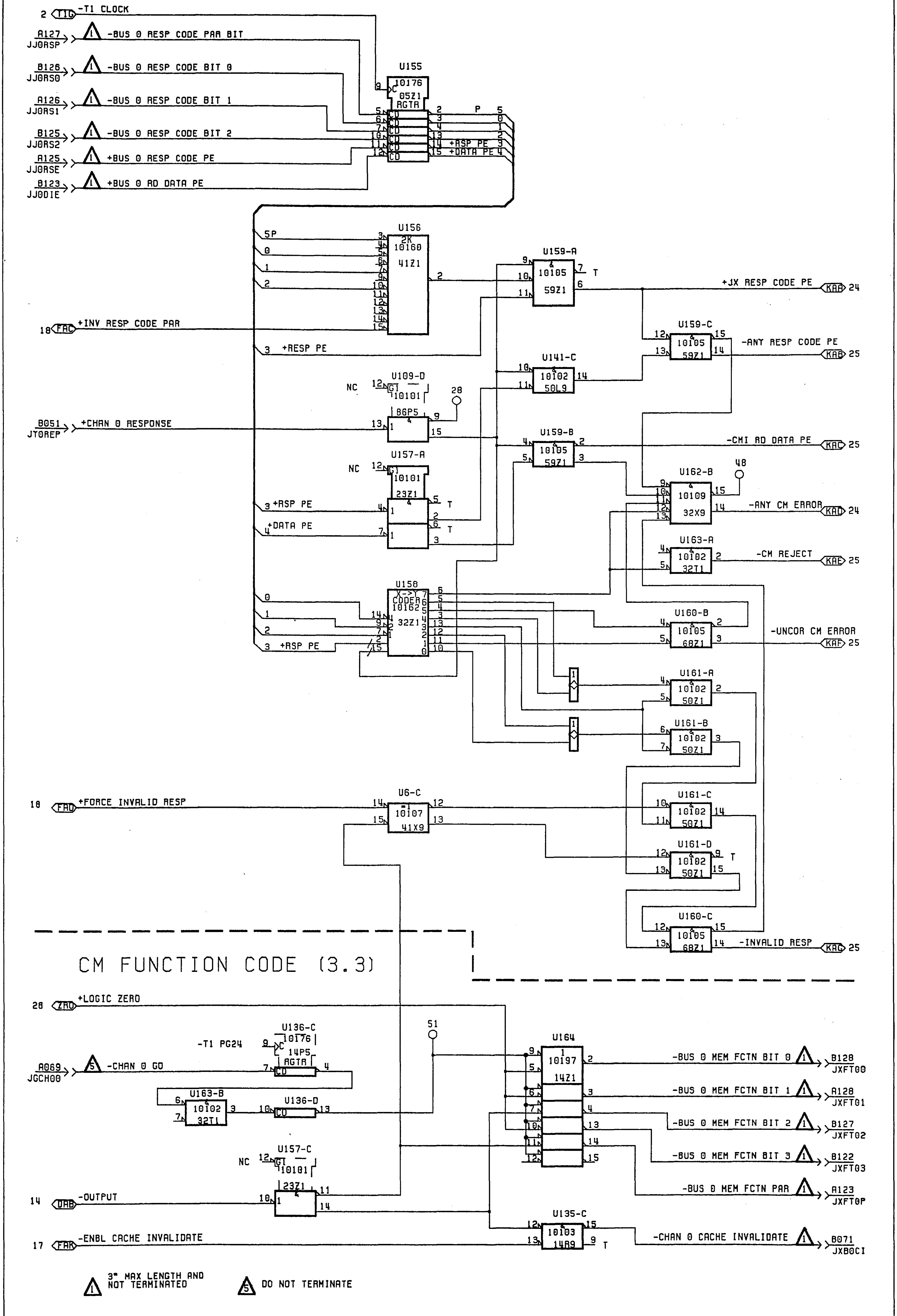
CONTROL DATA	CIO CHANNEL BOARD BAS I/F ERROR STATUS NETWORK	B	DWG NO. 22105623	DATE 02/28/86	REV A
	TYPE 1JXH	N	SHEET NO. 24	60462210	PAGE JX-24

ERROR STATUS NETWORK (3.6)



CONTROL DATA	CIO CHANNEL BOARD BAS I/F ERROR STAT NETWORK TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		SHEET NO. 25	60462210	PAGE JX-25	

CM RESPONSE CODE TRANSLATOR (3.6)



1 3" MAX LENGTH AND NOT TERMINATED

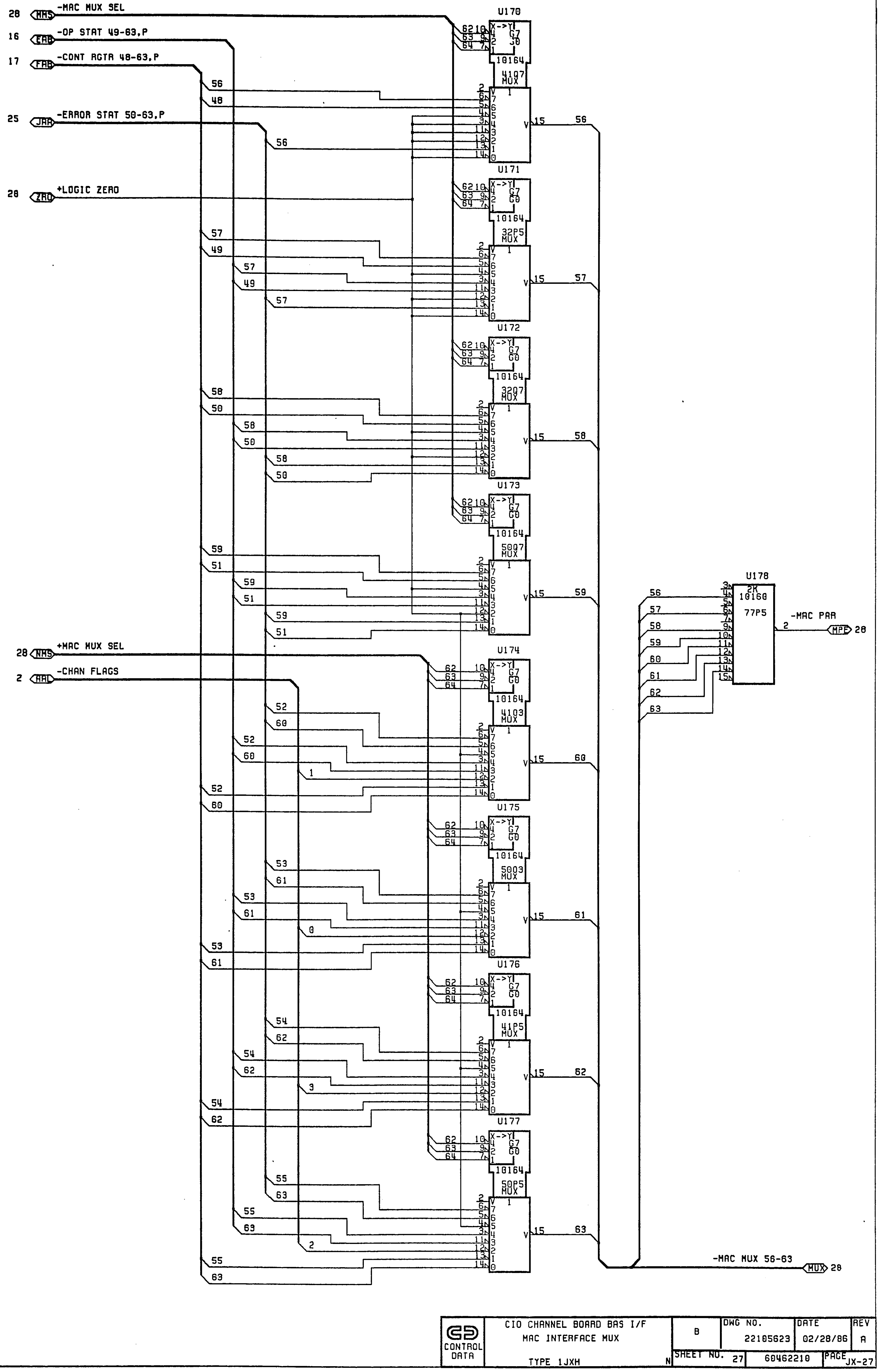
5 DO NOT TERMINATE

CONTROL DATA

CIO CHANNEL BOARD BAS I/F
CM RESPONSE CODE TRANSLATOR
CM FUNCTION CODE
TYPE 1JXH

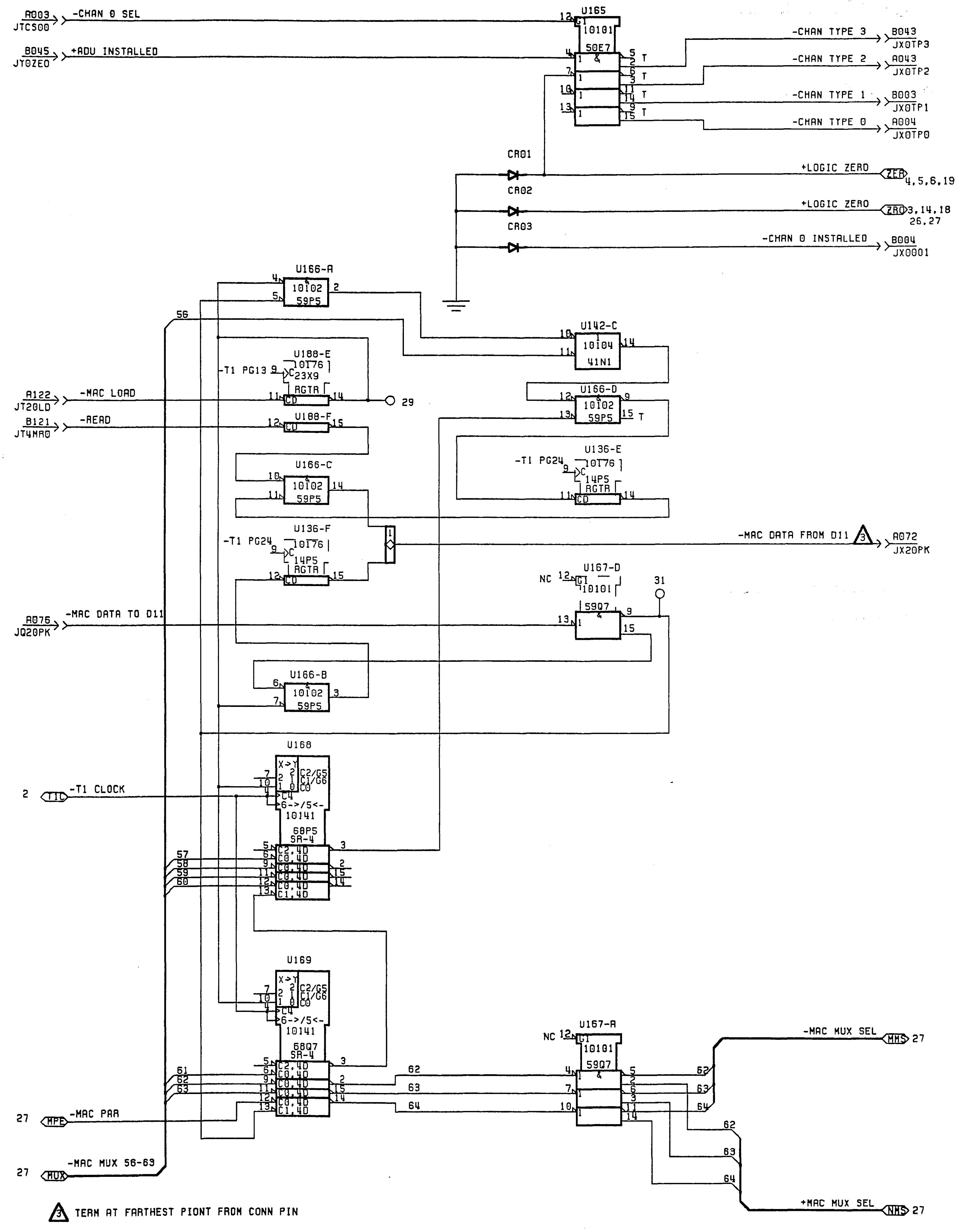
	DWG NO.	DATE	REV
B	22105623	02/28/86	A
SHEET NO. 26	60462210	PAGE JX-26	

MAC INTERFACE MUX (3.7)



	CIO CHANNEL BOARD BAS I/F MAC INTERFACE MUX TYPE 1JXH	B	DWG NO. 22185623	DATE 02/28/86	REV A
CONTROL DATA		N	SHEET NO. 27	60462210	PAGE JX-27

MAC INTERFACE (3.7)



3 TERM AT FARTHEST PIONT FROM CONN PIN

CONTROL DATA	CIO CHANNEL BOARD BAS I/F MAC INTERFACE TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		N	SHEET NO. 28	60462210	PAGE JX-28

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	10	-FUNC REG BIT 7	27	14	-NON INTERLOCK
02	10	-FUNC REG BIT 5	28	26	+CM RESPONSE
03	10	-FUNC REG BIT 6	29	28	+MAC LOAD
04	10	-FUNC REG BIT 4	30	24	+CHANNEL ERROR
05	10	-FUNC REG BIT 3	31	28	-MAC WRITE DATA
06	10	-FUNC REG BIT 1	32	14	+ISI FUNC WORD
07	10	-FUNC REG BIT 2	33	18	-IDLE MODE
08	10	-FUNC REG BIT 0	34	14	+FORCE SYNC OUT
09	14	-ISI FUNC BIT 48	35	07	-CHAN DATA BIT 63
10	20	+ISI BUSY	36	25	+ERROR IN
11	14	+ISI FUNC BIT 54	37	02	-DEADSTART OR MC
12	19	-STROBE MASK RGTR	38	03	-CHANNEL SELECT
13	07	-CLEAR T RGTR	39	19	-SET FLAG
14	07	-MASTER CLEAR	40	02	-T1 CLOCK
15	15	+TRANSFER MODE	41	03	+FLAG
16	16	+ECHO MODE	42	03	+ERROR FLAG
17	17	-STROBE CNTL RGTR	43	16	+SEL HOLD
18	23	-INC PARCEL CNTR	44	16	+CMD SEQUENCE
19	15	+DMA MODE	45	03	+ACTIVE FLAG
20	23	-PARCEL CNTR BIT 1	46	15	+PP MODE
21	21	-T PRIME RGTR FULL	47	14	-INPUT MODE
22	22	-T RGTR EQUALS ZERO	48	26	+ANY CM ERROR
23	24	-JX ERROR	49	03	+FULL FLAG
24	23	-PARCEL CNTR BIT 1	50	14	+BUS SLAVE SELECTED
25	23	-WRITE T	51	26	-CHAN GO
26	20	+INCREMENT T CNT			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 (NU)
TERM	NONE
UNUSED	A008,B018,A019,B019,A020,B020,A021,B021,A022,B022,A023,B023,A025,B025,A026,B026,B052,B076,A078,B078,A079,B079,A080,B080,A081,B081,A082,B082,A083,B083,A084,B084,A085,B085,A086,B086,A088,B088,A092,B092,B108,A121

CONTROL DATA	CIO CHANNEL BOARD BAS I/F TESTPOINTS AND SIGNAL NAMES AND CONNECTOR PINS TYPE 1JXH	B	DWG NO. 22105623	DATE 02/28/86	REV A
		N	SHEET NO. 29	60462210	PAGE JX-29

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1JYH CIO CHANNEL BOARD

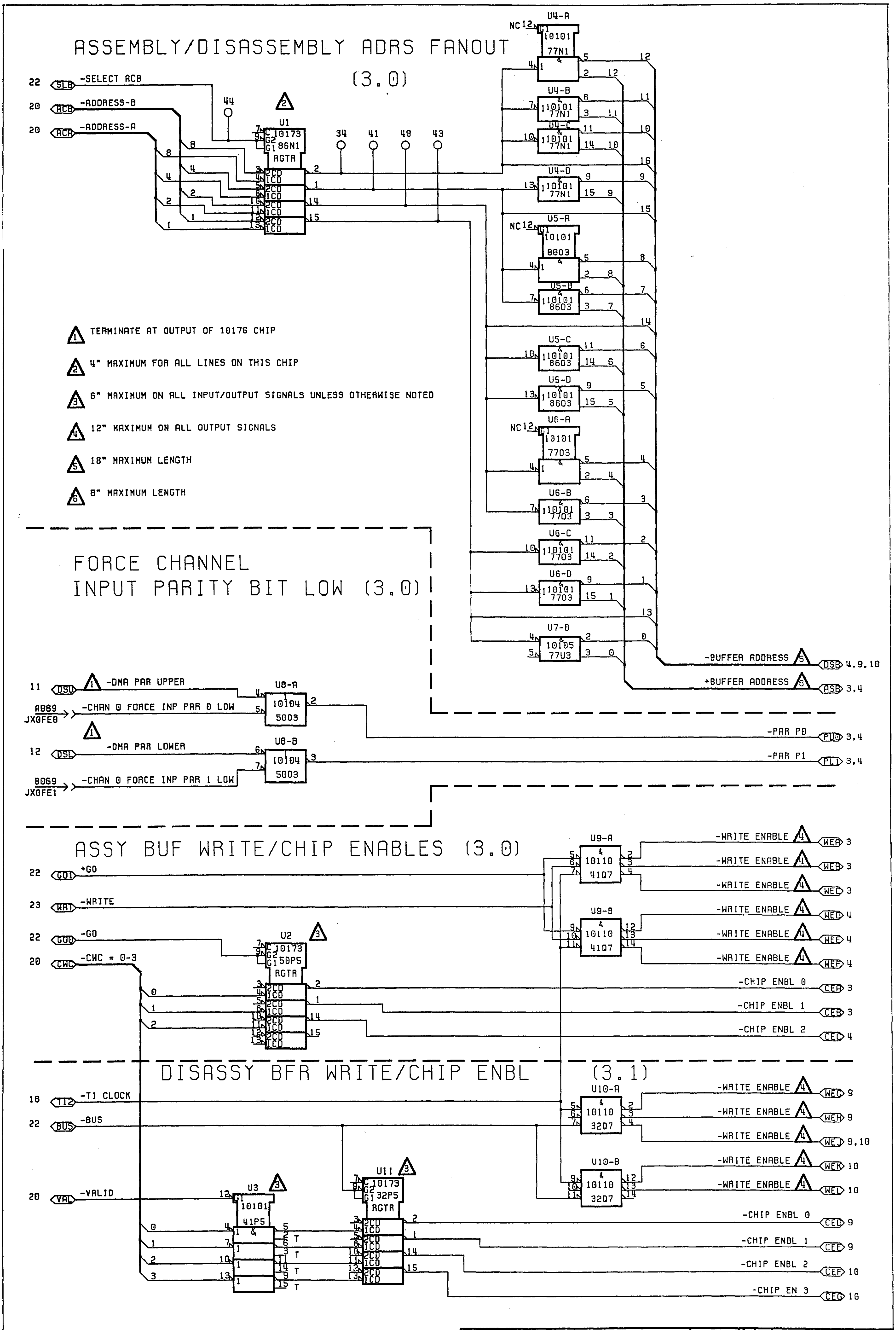
REVISION HISTORY B/M 41652700			
DATE	REV	DESCRIPTION OF CHANGE	INIT
12/02/85	A	CLASS A RELEASE OF LOGIC DIAGRAMS WITH	
		ECO 46883 INSTALLED.	LHJ
04/07/86	B	ECO #47444 ADDS LEVEL 3 REFERENCES	
		TO SHEETS 2 THRU 27.	LHJ
04/21/86	C	ECO #47732 SHEETS 20 AND 23.	
01/21/88	D	ECO #49505 DIAGRAM CORRECTIONS TO	
		SHEET 22.	DS

DWN	L H JOHNSON	12/02/85
CHKD	L H JOHNSON	02/04/86
ENG	J P STROMBECK	02/05/86
PUBS	D K BONDE	02/06/86
APP	J P STROMBECK	02/05/86

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

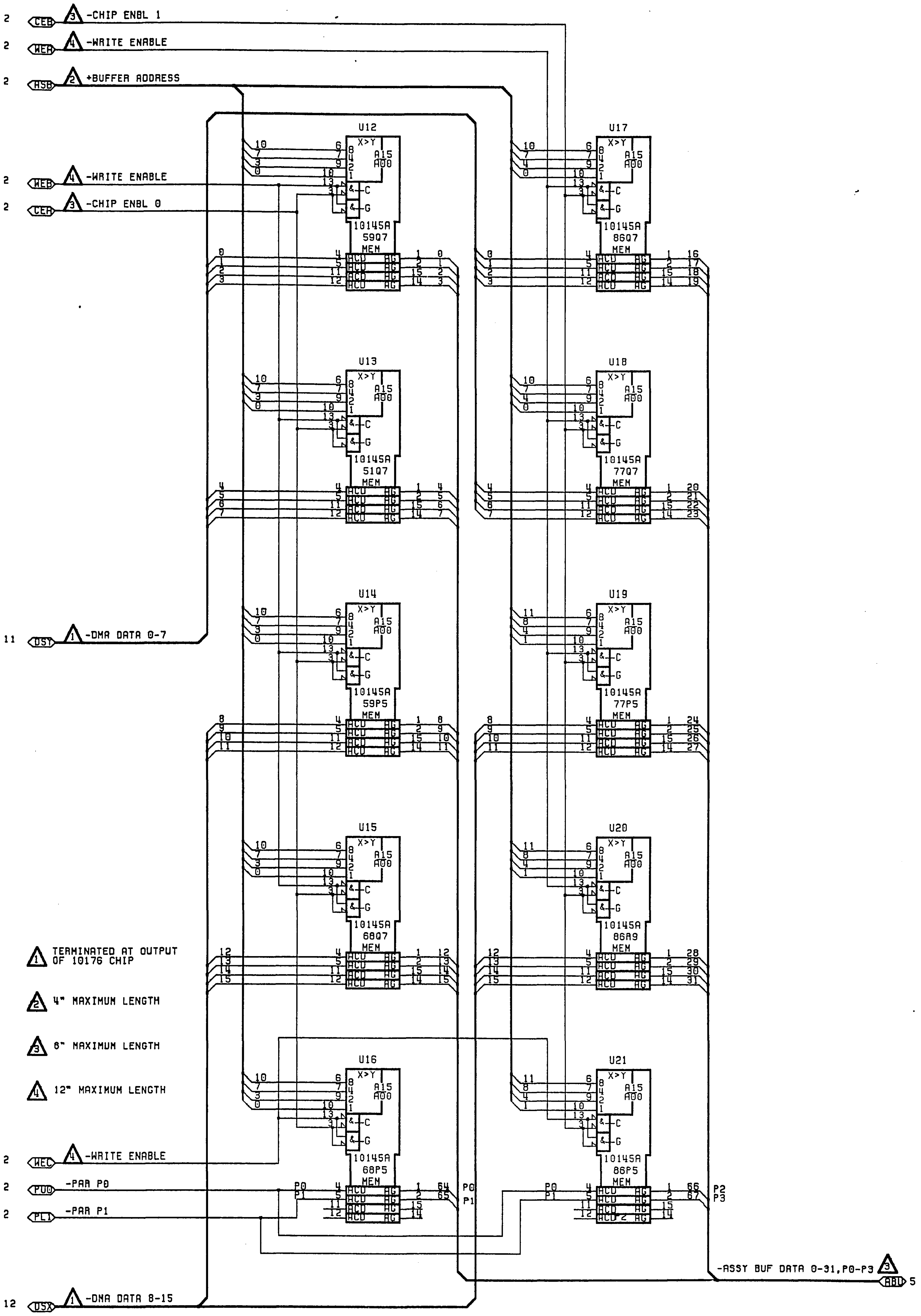
LOC: D10, D13, D16, D19, D22
C10, C13, C16, C19, C22

CONTROL DATA	REVISION HISTORY	B	DWG NO. 53575513	DATE 06/14/88	REV D
	TYPE 1JYH	N	SHEET NO. 1	60462210	PAGE JY-01

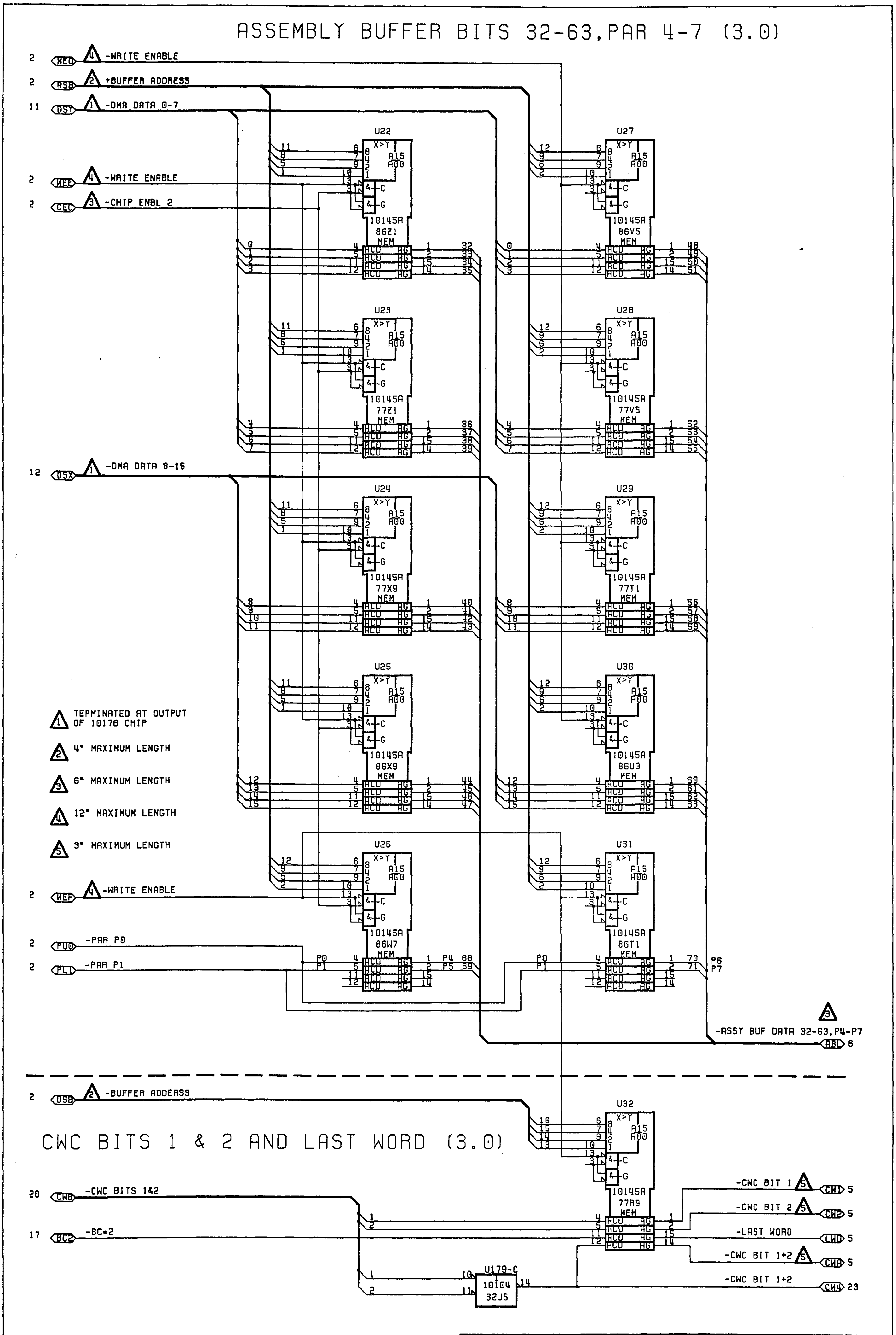


CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY/DISASSEMBLY ADDRESS. WRITE & CHIP ENABLE FANOUTS TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
	N	SHEET NO. 2	60462210	PAGE JY-02	

ASSEMBLY BUFFER BITS 0-31,PAR 0-3 (3.0)



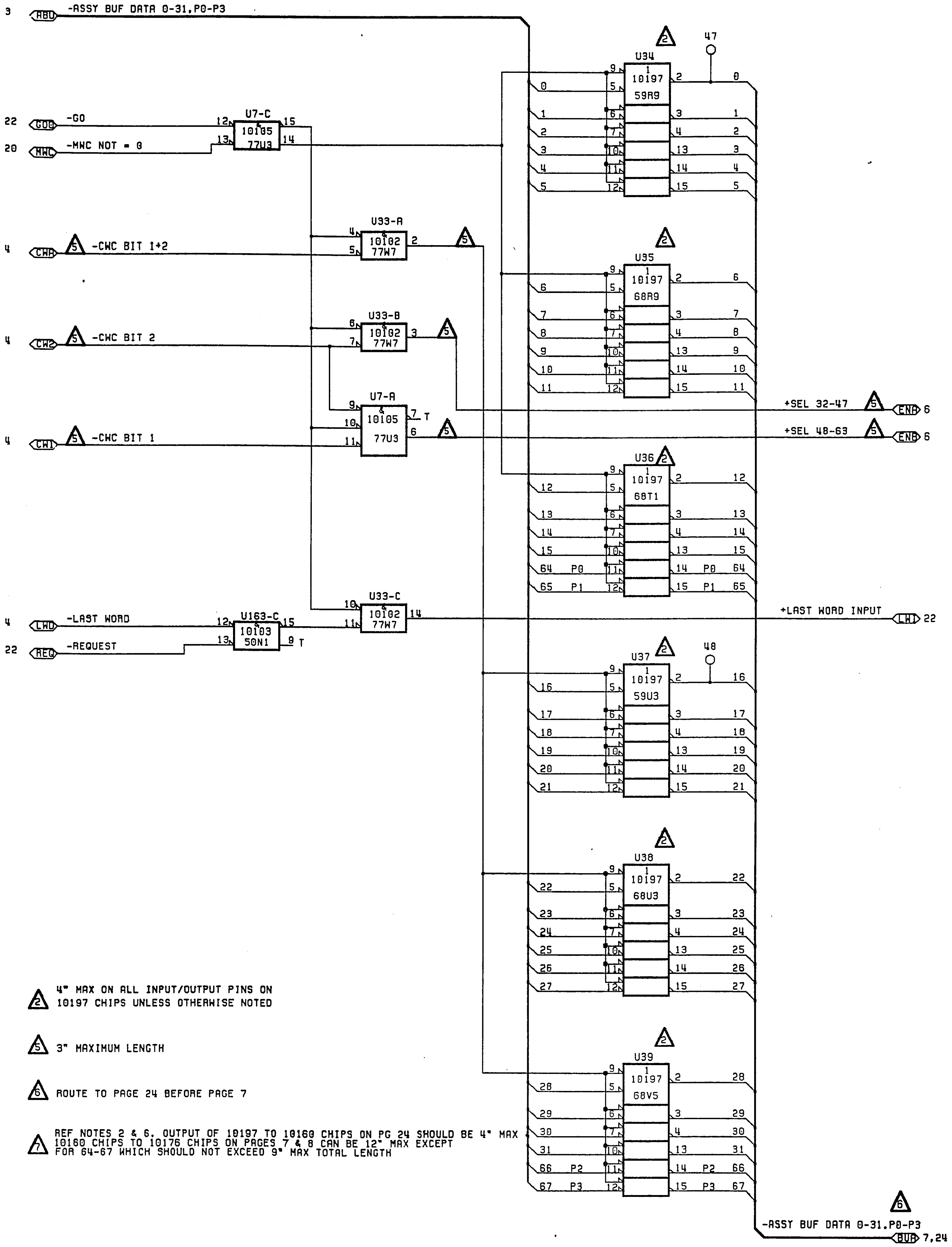
CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER BITS 0-31,P0-P3 TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 3	60442210	PAGE JY-03	



CONTROL DATA
CIO CHANNEL BOARD
ASSEMBLY BUFFER BITS 32-63,P4-P7
CWC BITS 1 & 2 AND LAST WORD
TYPE 1JYH

	DWG NO.	DATE	REV
B	53575513	04/07/86	A
SHEET NO. 4	60462210	PAGE JY-04	

SELECT 0-15,16-31 TO CM (3.0)



2 4" MAX ON ALL INPUT/OUTPUT PINS ON 10197 CHIPS UNLESS OTHERWISE NOTED

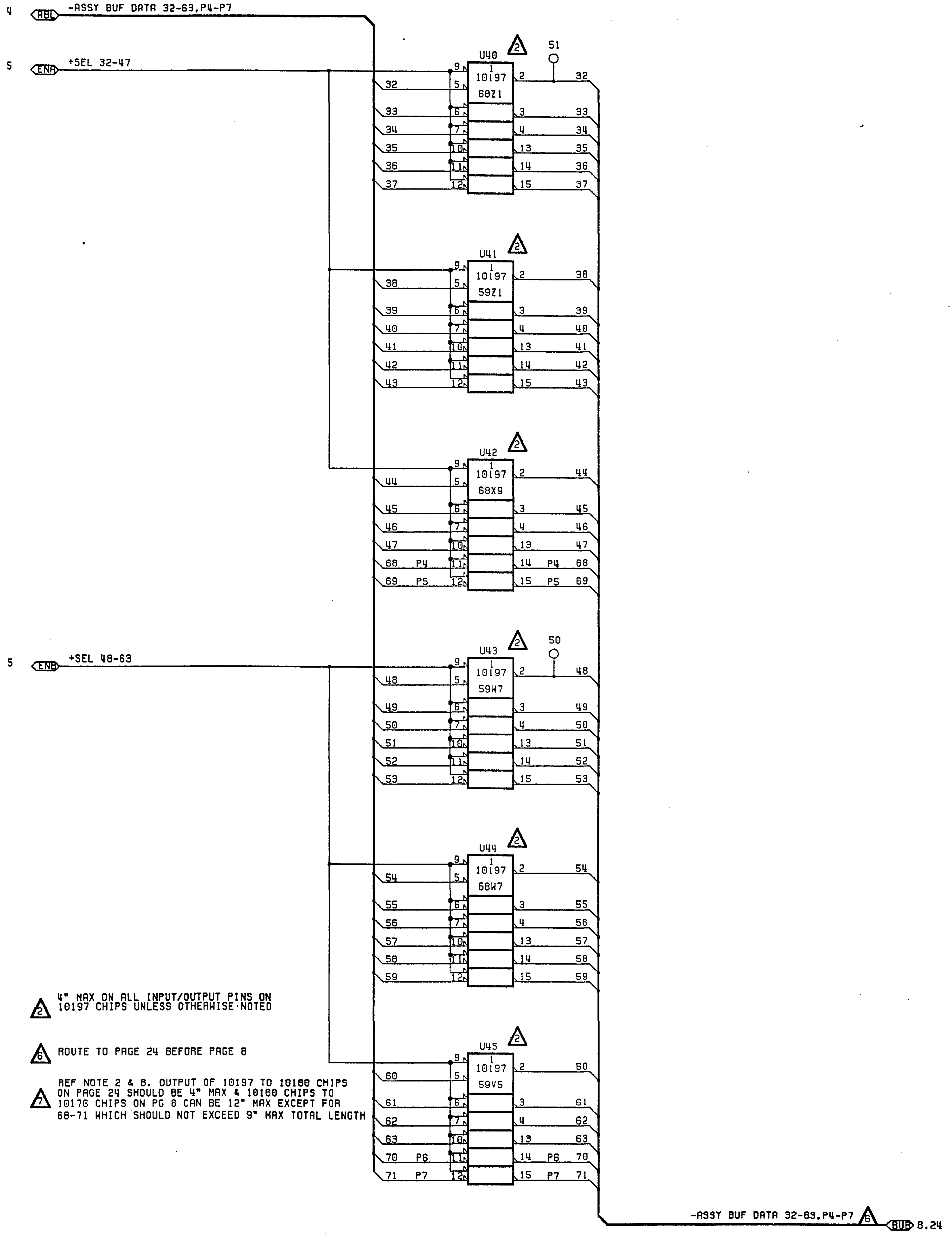
5 3" MAXIMUM LENGTH

6 ROUTE TO PAGE 24 BEFORE PAGE 7

7 REF NOTES 2 & 6. OUTPUT OF 10197 TO 10160 CHIPS ON PG 24 SHOULD BE 4" MAX 10160 CHIPS TO 10176 CHIPS ON PAGES 7 & 8 CAN BE 12" MAX EXCEPT FOR 64-67 WHICH SHOULD NOT EXCEED 9" MAX TOTAL LENGTH

CONTROL DATA	CIO CHANNEL BOARD SELECT 0-15,16-31 TO CM TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 5	60462210	PAGE JY-05	

SELECT 32-47,48-63 TO CM (3.0)



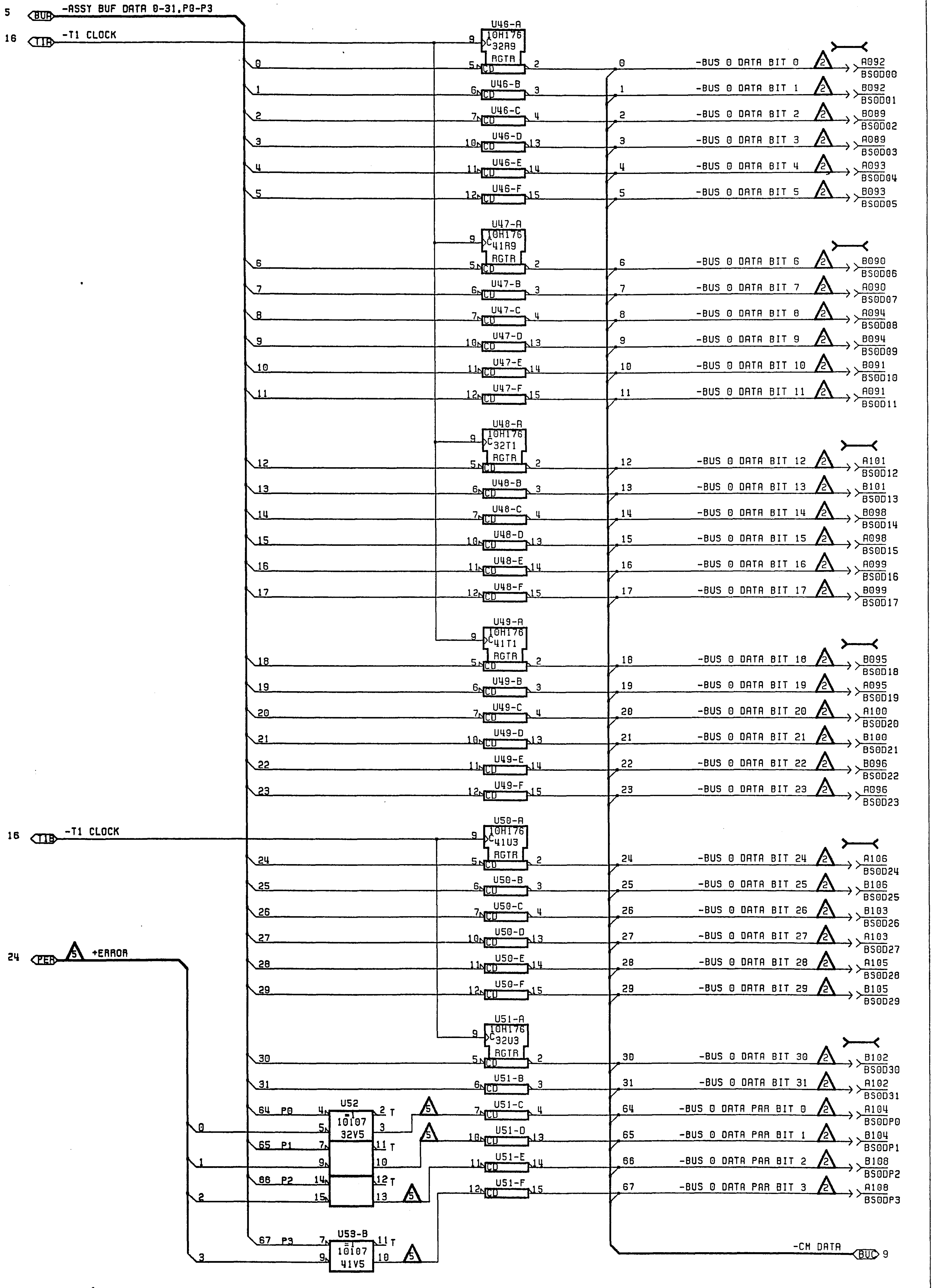
2. 4" MAX ON ALL INPUT/OUTPUT PINS ON 10197 CHIPS UNLESS OTHERWISE NOTED

6. ROUTE TO PAGE 24 BEFORE PAGE 8

7. REF NOTE 2 & 6. OUTPUT OF 10197 TO 10160 CHIPS ON PAGE 24 SHOULD BE 4" MAX & 10160 CHIPS TO 10176 CHIPS ON PG 8 CAN BE 12" MAX EXCEPT FOR 68-71 WHICH SHOULD NOT EXCEED 9" MAX TOTAL LENGTH

CONTROL DATA	CIO CHANNEL BOARD SELECT 32-47,48-63 TO CM TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		N	SHEET NO. 6	60462210	PAGE JY-06

ASSEMBLY BUFFER OUTPUT
REGISTER BITS 0-31,PAR 0-3 (3.1)



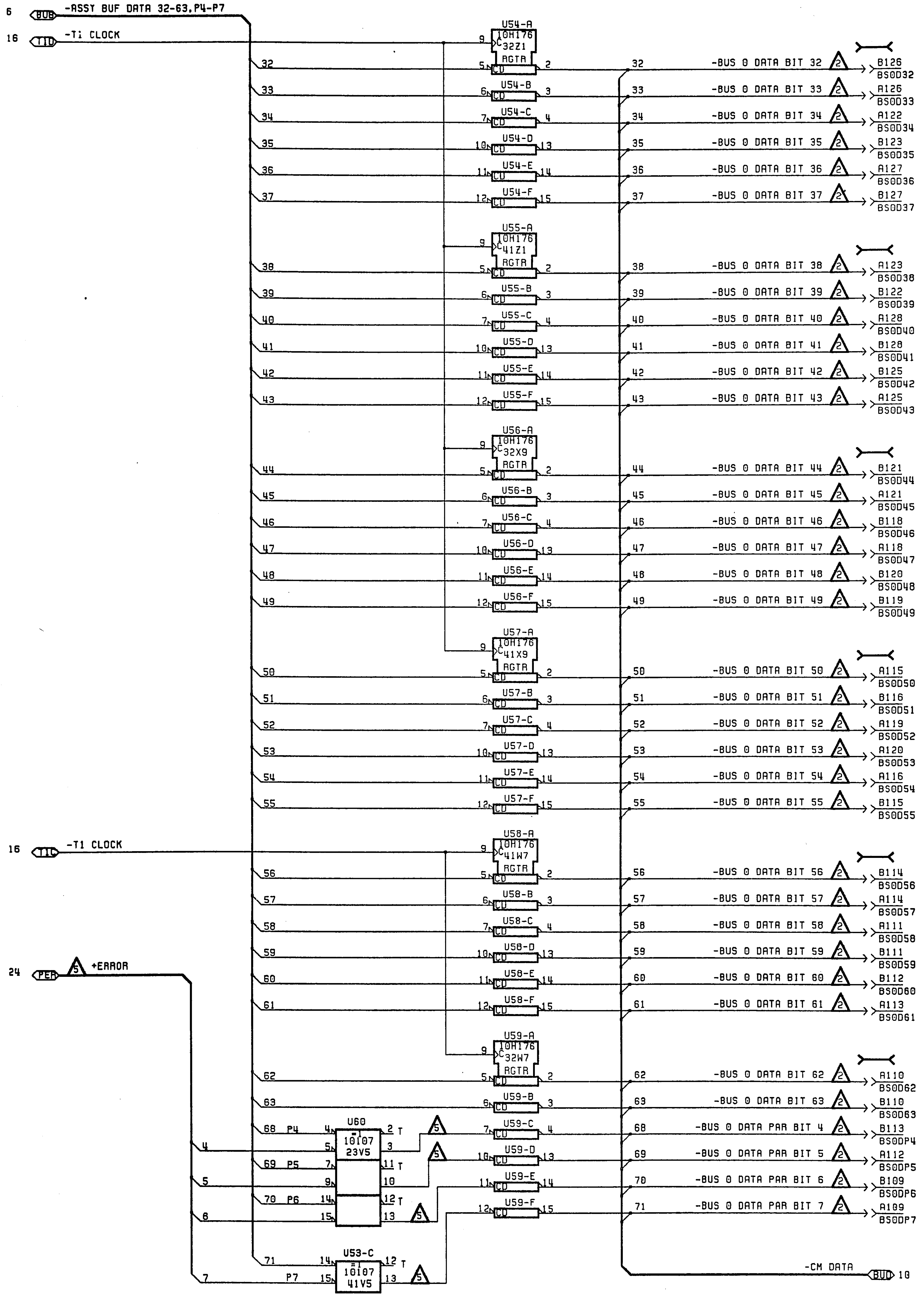
5 BUR -ASSY BUF DATA 0-31,P0-P3
16 T1B -T1 CLOCK
16 T1B -T1 CLOCK
24 PER 5 +ERROR
U46-A 10H176 32A9 RGTR
U46-B
U46-C
U46-D
U46-E
U46-F
U47-A 10H176 41A9 RGTR
U47-B
U47-C
U47-D
U47-E
U47-F
U48-A 10H176 32T1 RGTR
U48-B
U48-C
U48-D
U48-E
U48-F
U49-A 10H176 41T1 RGTR
U49-B
U49-C
U49-D
U49-E
U49-F
U50-A 10H176 41U3 RGTR
U50-B
U50-C
U50-D
U50-E
U50-F
U51-A 10H176 32U3 RGTR
U51-B
U51-C
U51-D
U51-E
U51-F
U52 =1 10107 32V5
U53-B =1 10107 41V5
64 P0
65 P1
66 P2
67 P3
-BUS 0 DATA BIT 0 A092 BS0D00
-BUS 0 DATA BIT 1 B092 BS0D01
-BUS 0 DATA BIT 2 B089 BS0D02
-BUS 0 DATA BIT 3 A089 BS0D03
-BUS 0 DATA BIT 4 A093 BS0D04
-BUS 0 DATA BIT 5 B093 BS0D05
-BUS 0 DATA BIT 6 B090 BS0D06
-BUS 0 DATA BIT 7 A090 BS0D07
-BUS 0 DATA BIT 8 A094 BS0D08
-BUS 0 DATA BIT 9 B094 BS0D09
-BUS 0 DATA BIT 10 B091 BS0D10
-BUS 0 DATA BIT 11 A091 BS0D11
-BUS 0 DATA BIT 12 A101 BS0D12
-BUS 0 DATA BIT 13 B101 BS0D13
-BUS 0 DATA BIT 14 B098 BS0D14
-BUS 0 DATA BIT 15 A098 BS0D15
-BUS 0 DATA BIT 16 A099 BS0D16
-BUS 0 DATA BIT 17 B099 BS0D17
-BUS 0 DATA BIT 18 B095 BS0D18
-BUS 0 DATA BIT 19 A095 BS0D19
-BUS 0 DATA BIT 20 A100 BS0D20
-BUS 0 DATA BIT 21 B100 BS0D21
-BUS 0 DATA BIT 22 B096 BS0D22
-BUS 0 DATA BIT 23 A096 BS0D23
-BUS 0 DATA BIT 24 A106 BS0D24
-BUS 0 DATA BIT 25 B106 BS0D25
-BUS 0 DATA BIT 26 B103 BS0D26
-BUS 0 DATA BIT 27 A103 BS0D27
-BUS 0 DATA BIT 28 A105 BS0D28
-BUS 0 DATA BIT 29 B105 BS0D29
-BUS 0 DATA BIT 30 B102 BS0D30
-BUS 0 DATA BIT 31 A102 BS0D31
-BUS 0 DATA PAR BIT 0 A104 BS0DP0
-BUS 0 DATA PAR BIT 1 B104 BS0DP1
-BUS 0 DATA PAR BIT 2 B108 BS0DP2
-BUS 0 DATA PAR BIT 3 A108 BS0DP3
-CM DATA BUC 9

2 4" MAXIMUM LENGTH & NOT TERMINATED

5 3" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER OUTPUT REGISTER BITS 0-31,P0-P3 TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		N	SHEET NO. 7	60462210	PAGE JY-07

ASSEMBLY BUFFER OUTPUT
REGISTER BITS 32-63,PAR 4-7 (3.1)

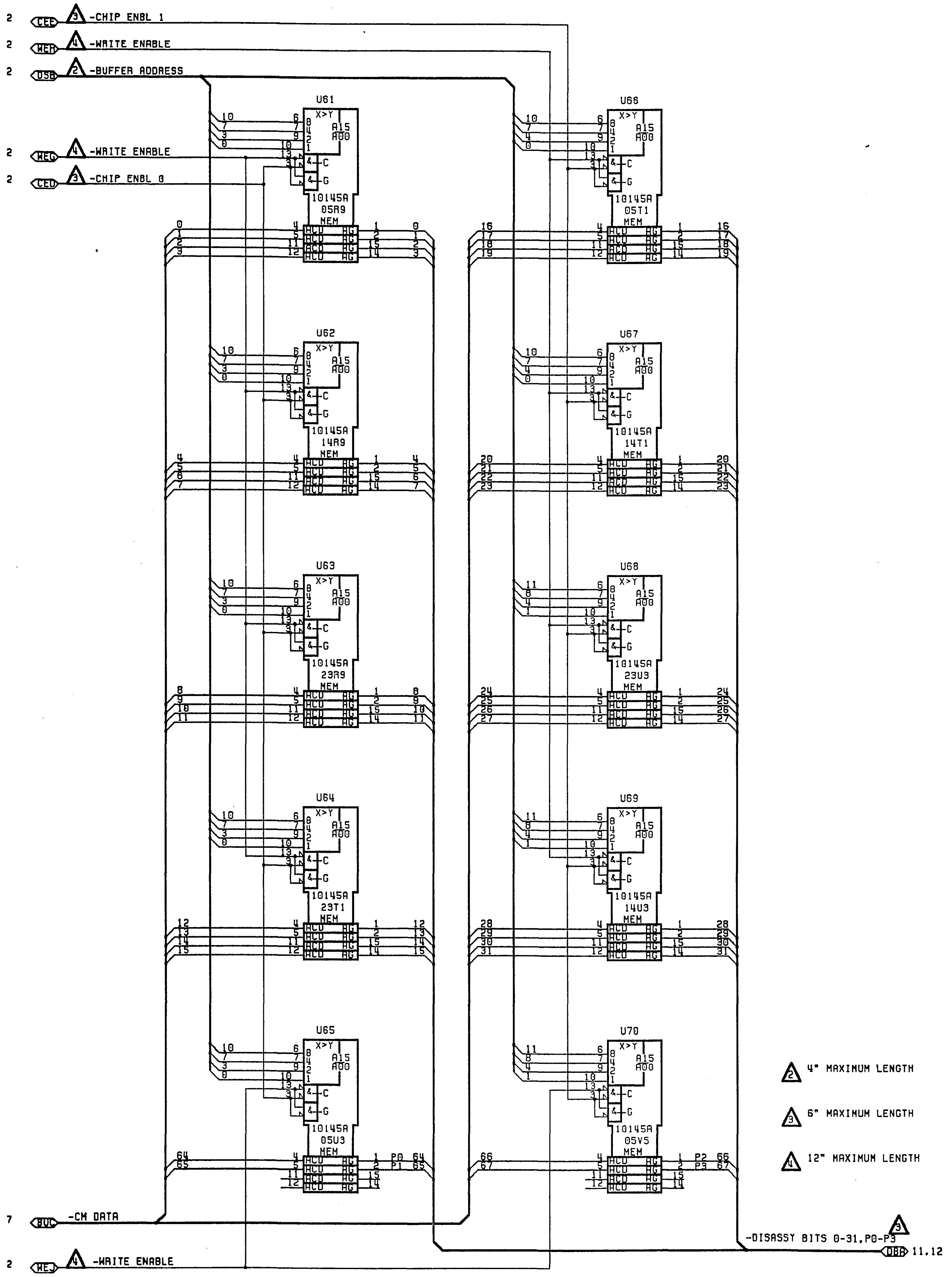

6 BUB -ASSY BUF DATA 32-63,P4-P7
16 T1D -T1 CLOCK
U54-A 10H176 32Z1 RGTR
U55-A 10H176 41Z1 RGTR
U56-A 10H176 32X9 RGTR
U57-A 10H176 41X9 RGTR
U58-A 10H176 41W7 RGTR
U59-A 10H176 32W7 RGTR
U60 =1 10107 23V5
U53-C =1 10107 41V5
24 PER +ERROR
-BUS 0 DATA BIT 32 B126 BS0D32
-BUS 0 DATA BIT 33 A126 BS0D33
-BUS 0 DATA BIT 34 A122 BS0D34
-BUS 0 DATA BIT 35 B123 BS0D35
-BUS 0 DATA BIT 36 A127 BS0D36
-BUS 0 DATA BIT 37 B127 BS0D37
-BUS 0 DATA BIT 38 A123 BS0D38
-BUS 0 DATA BIT 39 B122 BS0D39
-BUS 0 DATA BIT 40 A128 BS0D40
-BUS 0 DATA BIT 41 B128 BS0D41
-BUS 0 DATA BIT 42 B125 BS0D42
-BUS 0 DATA BIT 43 A125 BS0D43
-BUS 0 DATA BIT 44 B121 BS0D44
-BUS 0 DATA BIT 45 A121 BS0D45
-BUS 0 DATA BIT 46 B118 BS0D46
-BUS 0 DATA BIT 47 A118 BS0D47
-BUS 0 DATA BIT 48 B120 BS0D48
-BUS 0 DATA BIT 49 B119 BS0D49
-BUS 0 DATA BIT 50 A115 BS0D50
-BUS 0 DATA BIT 51 B116 BS0D51
-BUS 0 DATA BIT 52 A119 BS0D52
-BUS 0 DATA BIT 53 A120 BS0D53
-BUS 0 DATA BIT 54 A116 BS0D54
-BUS 0 DATA BIT 55 B115 BS0D55
-BUS 0 DATA BIT 56 B114 BS0D56
-BUS 0 DATA BIT 57 A114 BS0D57
-BUS 0 DATA BIT 58 A111 BS0D58
-BUS 0 DATA BIT 59 B111 BS0D59
-BUS 0 DATA BIT 60 B112 BS0D60
-BUS 0 DATA BIT 61 A113 BS0D61
-BUS 0 DATA BIT 62 A110 BS0D62
-BUS 0 DATA BIT 63 B110 BS0D63
-BUS 0 DATA PAR BIT 4 B113 BS0DP4
-BUS 0 DATA PAR BIT 5 A112 BS0DP5
-BUS 0 DATA PAR BIT 6 B109 BS0DP6
-BUS 0 DATA PAR BIT 7 A109 BS0DP7
68 P4
69 P5
70 P6
71 P7
-CM DATA BUD 10

△2 4" MAXIMUM LENGTH & NOT TERMINATED

△5 3" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER OUTPUT REGISTER BITS 32-63,P4-P7 TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 8	60462210	PAGE JY-08	

DISASSEMBLY BUFFER BITS 0-31,PAR 0-3 (3.1)

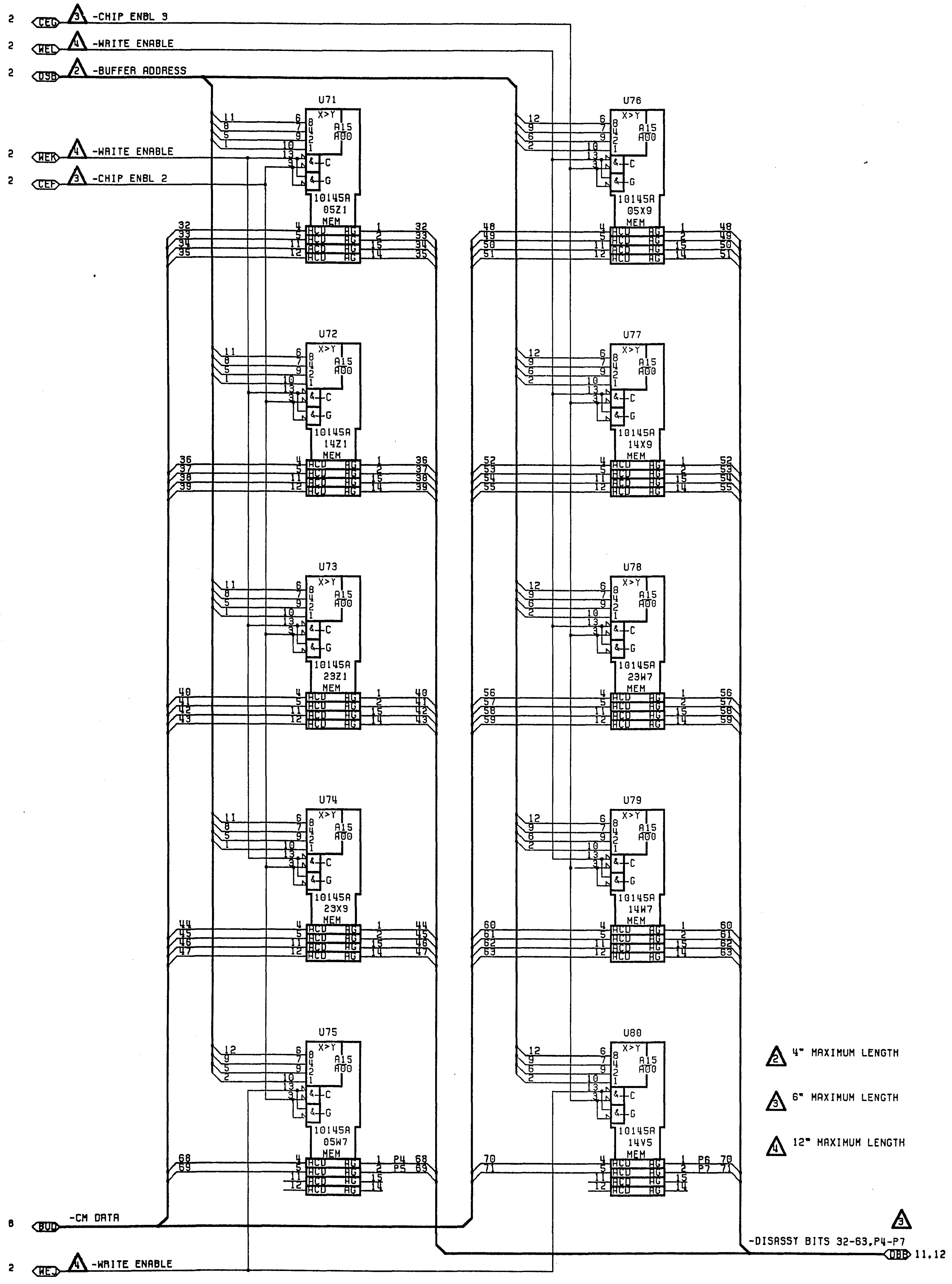


CONTROL DATA

CIO CHANNEL BOARD
DISASSEMBLY BITS 0-31,P0-P3
TYPE 1JYH

B
DWG NO. 53575513
DATE 04/07/86
REV A
N SHEET NO. 9
60462210
PAGE JT-09

DISASSEMBLY BUFFER BITS 32-63,PAR 4-7 (3.1)



CONTROL DATA

CIO CHANNEL BOARD

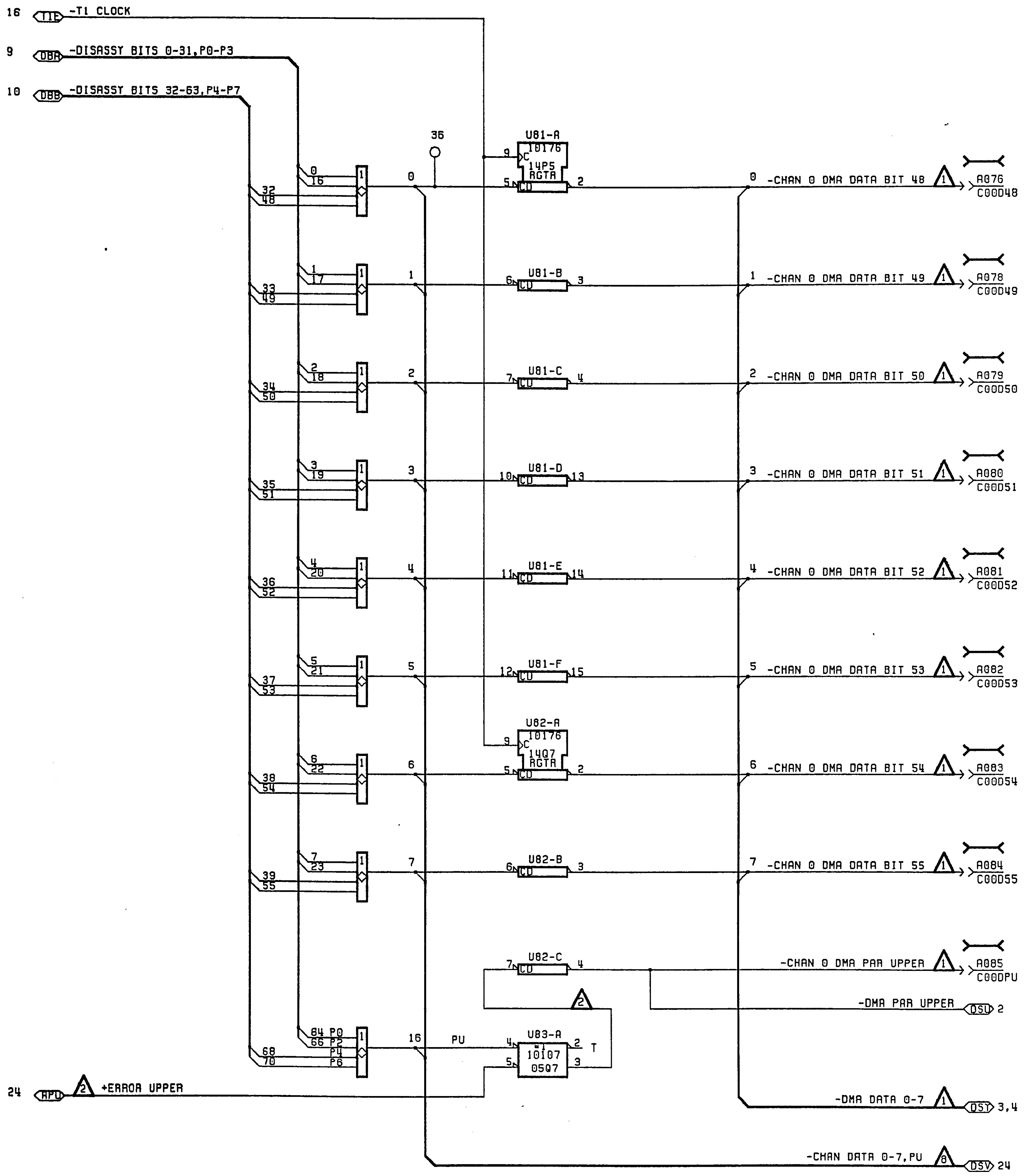
DISASSEMBLY BITS 32-63,P4-P7

TYPE 1JYH

	DWG NO.	DATE	REV
B	53575513	04/07/86	A
SHEET NO. 10	60462210	PAGE JT-10	

DISASSEMBLY BUFFER OUTPUT REGISTER BITS 0-7,PAR UPR

(3.1)



16 TIE -T1 CLOCK
9 DBA -DISASSY BITS 0-31,P0-P3
10 DBB -DISASSY BITS 32-63,P4-P7
36
U81-A 10176 14P5 RGTR
9 C
5 CD 2
0 16
32 48
0
U81-B 6 CD 3
1 17
33 49
1
U81-C 7 CD 4
2 18
34 50
2
U81-D 10 CD 13
3 19
35 51
3
U81-E 11 CD 14
4 20
36 52
4
U81-F 12 CD 15
5 21
37 53
5
U82-A 10176 14Q7 RGTR
9 C
5 CD 2
6 22
38 54
6
U82-B 6 CD 3
7 23
39 55
7
0 -CHAN 0 DMA DATA BIT 48 1 A076 C00D48
1 -CHAN 0 DMA DATA BIT 49 1 A078 C00D49
2 -CHAN 0 DMA DATA BIT 50 1 A079 C00D50
3 -CHAN 0 DMA DATA BIT 51 1 A080 C00D51
4 -CHAN 0 DMA DATA BIT 52 1 A081 C00D52
5 -CHAN 0 DMA DATA BIT 53 1 A082 C00D53
6 -CHAN 0 DMA DATA BIT 54 1 A083 C00D54
7 -CHAN 0 DMA DATA BIT 55 1 A084 C00D55
U82-C 7 CD 4
-CHAN 0 DMA PAR UPPER 1 A085 C00DPU
2
-DMA PAR UPPER DSU 2
64 P0
66 P2
68 P4
70 P6
16
PU
U83-A 4 =1 10107 0507 5 2 3
T
24 APU 2 +ERROR UPPER
-DMA DATA 0-7 1 DST 3,4
-CHAN DATA 0-7,PU 8 DSV 24

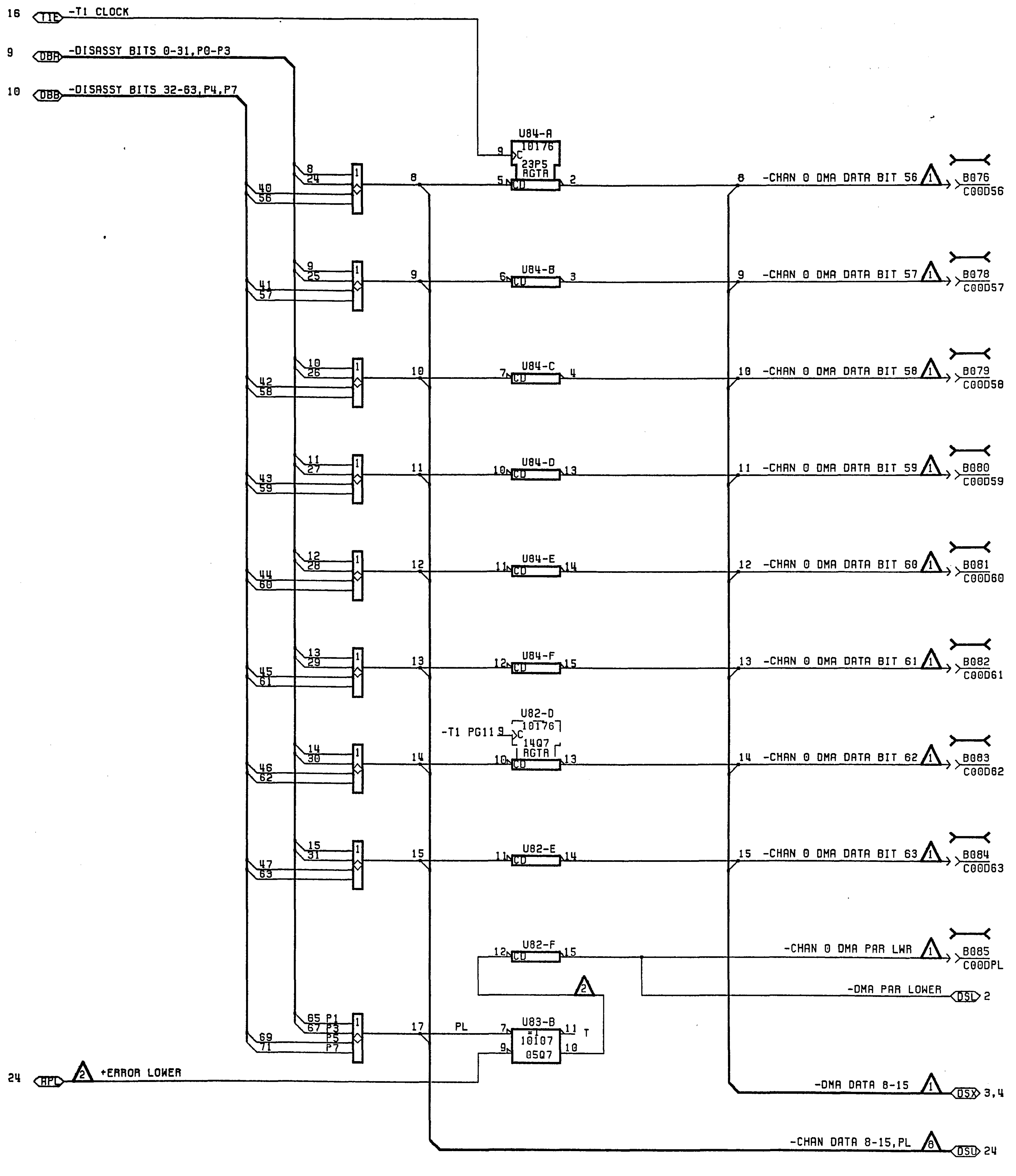
1 TERMINATE AT OUTPUT OF 10176 CHIP

2 4" MAXIMUM LENGTH

8 TERMINATE AT 10176/10107 CHIPS

CONTROL DATA
CIO CHANNEL BOARD
DISASSEMBLY BUFFER OUTPUT
REGISTER BITS 0-7.PU
TYPE 1JYH
B
DWG NO. 53575513
DATE 04/07/86
REV A
N SHEET NO. 11
60462210
PAGE JY-11

DISASSEMBLY BUFFER OUTPUT REGISTER BITS 8-15,PAR LWR
(3.1)



16 T1E -T1 CLOCK
9 DBA -DISASSY BITS 0-31,P0-P3
10 DBB -DISASSY BITS 32-63,P4,P7
U84-A 10176 23P5 AGTA
8 -CHAN 0 DMA DATA BIT 56 B076 C00D56
U84-B
9 -CHAN 0 DMA DATA BIT 57 B078 C00D57
U84-C
10 -CHAN 0 DMA DATA BIT 58 B079 C00D58
U84-D
11 -CHAN 0 DMA DATA BIT 59 B080 C00D59
U84-E
12 -CHAN 0 DMA DATA BIT 60 B081 C00D60
U84-F
13 -CHAN 0 DMA DATA BIT 61 B082 C00D61
U82-D 10176 1407 AGTA
-T1 PG11
14 -CHAN 0 DMA DATA BIT 62 B083 C00D62
U82-E
15 -CHAN 0 DMA DATA BIT 63 B084 C00D63
U82-F
-CHAN 0 DMA PAR LWR B085 C00DPL
-DMA PAR LOWER DSL 2
U83-B 10107 05Q7
PL
T
24 APL +ERROR LOWER
-DMA DATA 8-15 DSX 3,4
-CHAN DATA 8-15,PL DSU 24
65 P1 67 P3 69 P5 71 P7

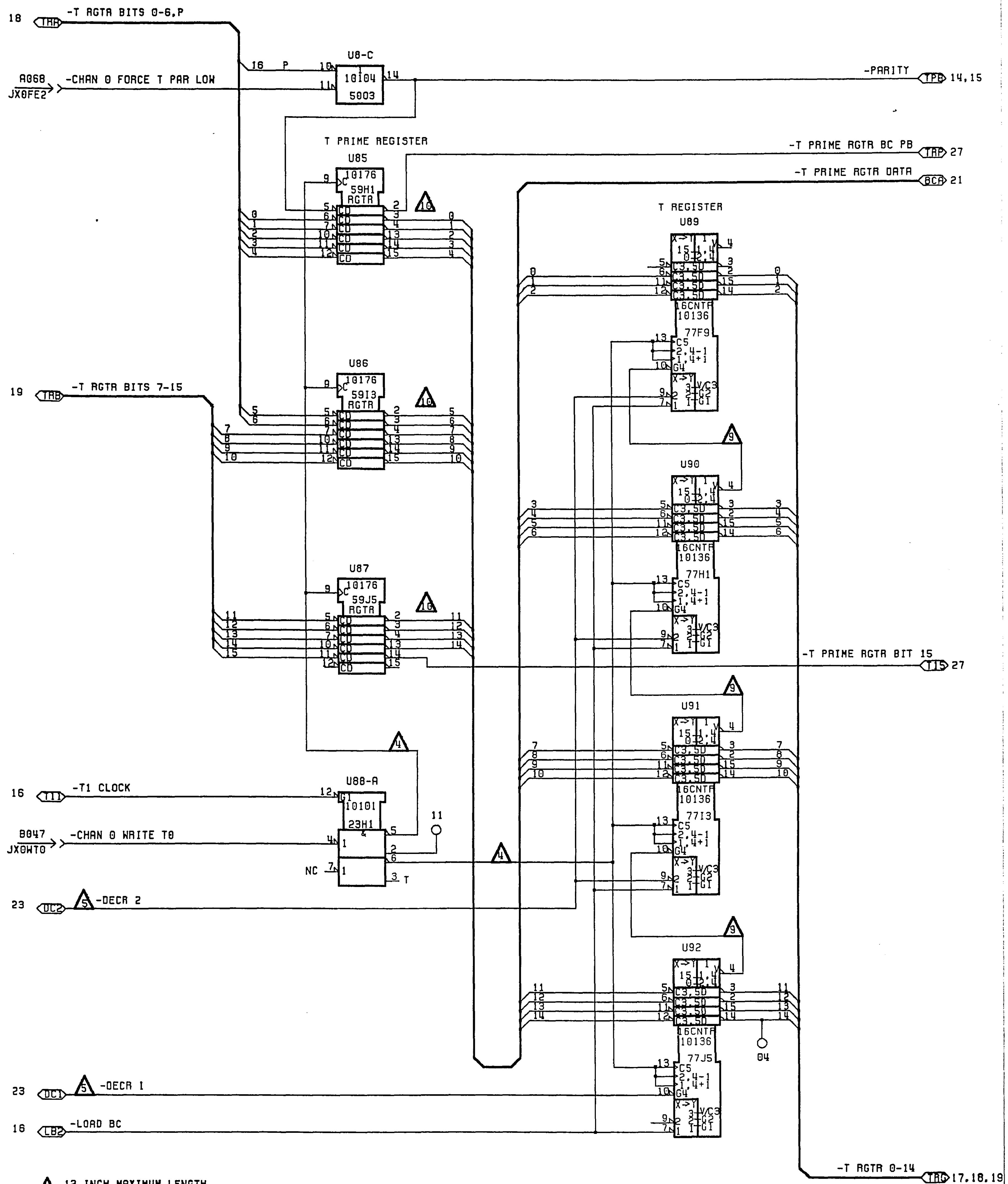
△1 TERMINATE AT OUTPUT OF 10176 CHIP

△2 4" MAXIMUM LENGTH

△8 TERMINATE AT 10176/10107 CHIPS

CONTROL DATA	CIO CHANNEL BOARD DISASSEMBLY BUFFER OUTPUT REGISTER BITS 8-15,PL TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		N	SHEET NO. 12	60462210	PAGE JY-12

T REGISTER BITS 0-15, PAR
BYTE COUNT 0-15 (3.2)



4 12 INCH MAXIMUM LENGTH

5 3 INCH MAXIMUM LENGTH

9 2 INCH MAXIMUM LENGTH

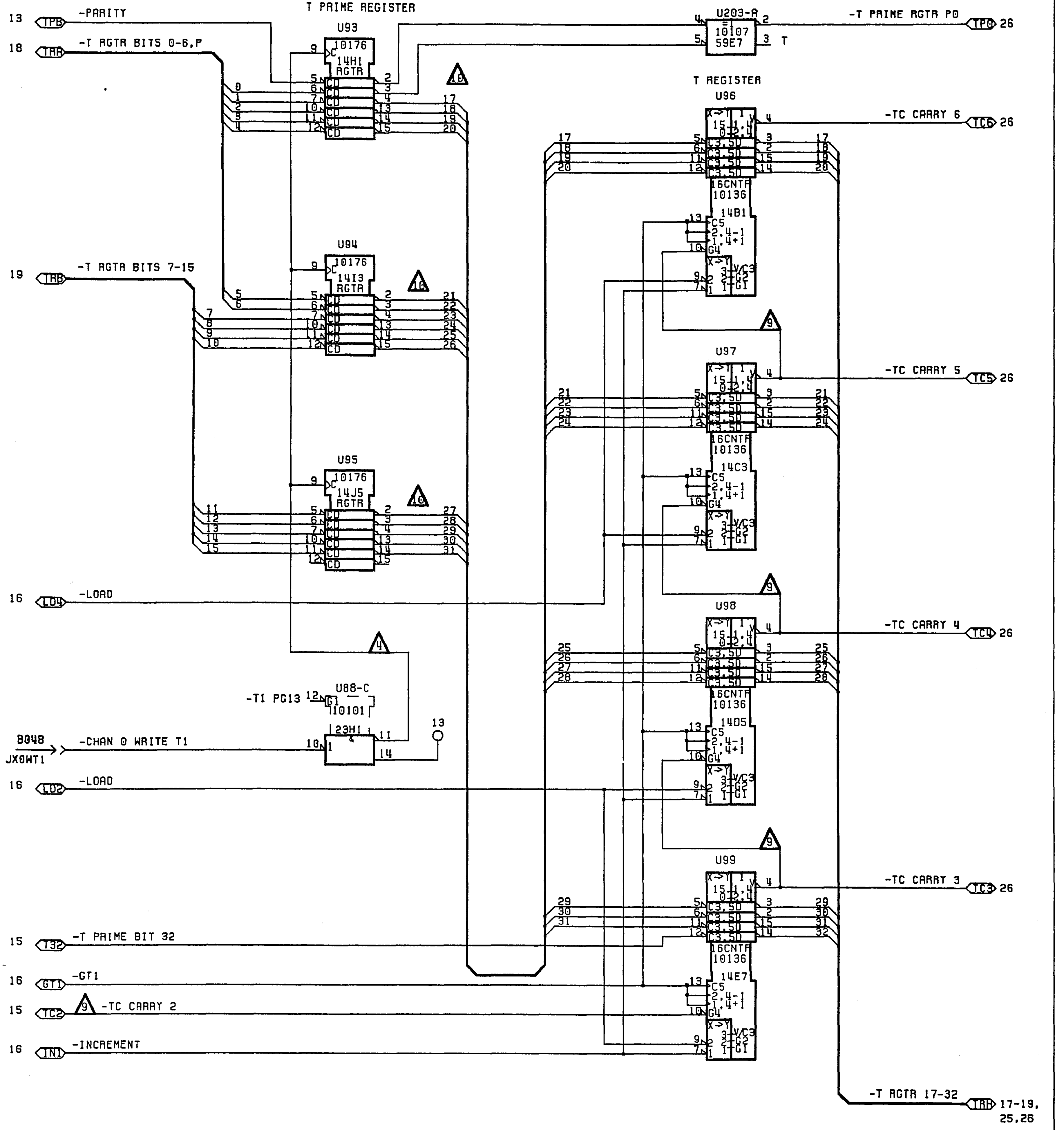
10 9 INCH MINIMUM LENGTHS
(EXCLUDING PIN2 ON U85 $ PIN 14 ON U87)

CONTROL DATA

CIO CHANNEL BOARD
T REGISTER BITS 0-15, PB
BYTE COUNT 0-15
TYPE 1JYH

	DWG NO.	DATE	REV
B	53575513	04/07/86	A
SHEET NO. 13	60462210	PAGE JY-13	

T REGISTER BITS 17-32, PAR 0
RMA 36-51 (3.2)



4 12 INCH MAXIMUM LENGTH

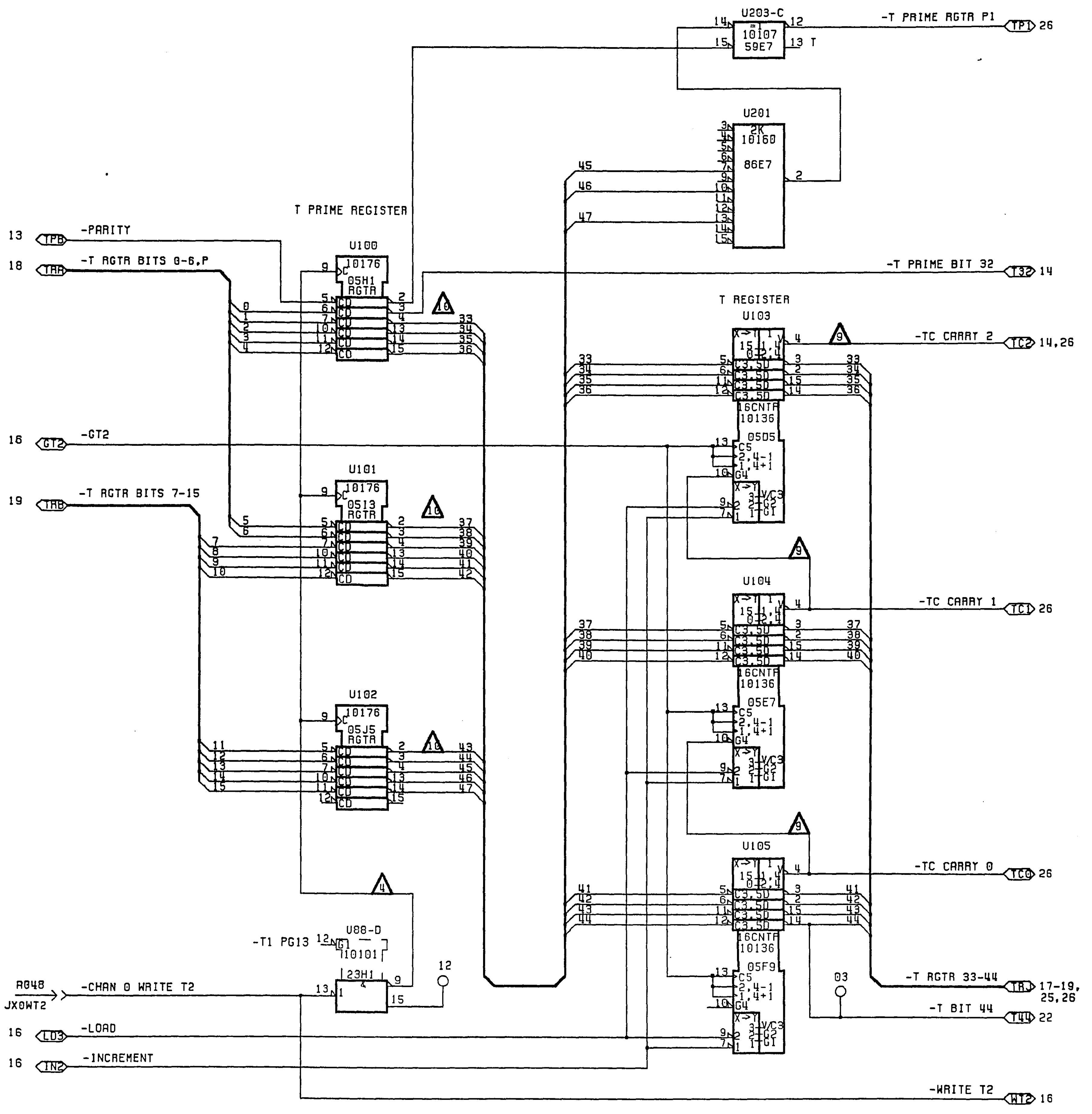
9 2 INCH MAXIMUM LENGTH

10 9 INCH MINUMUM LENGTHS (EXCLUDING PINS 2 & 3 ON U93)

CONTROL DATA | CIO CHANNEL BOARD
T REGISTER BITS 17-32, P0
RMA 36-51
TYPE 1JYH | B | DWG NO. 53575513 | DATE 04/07/86 | REV A
N | SHEET NO. 14 | 60462210 | PAGE JY-14

T REGISTER BITS 33-44, PAR 1

RMA 52-63 (3.2)



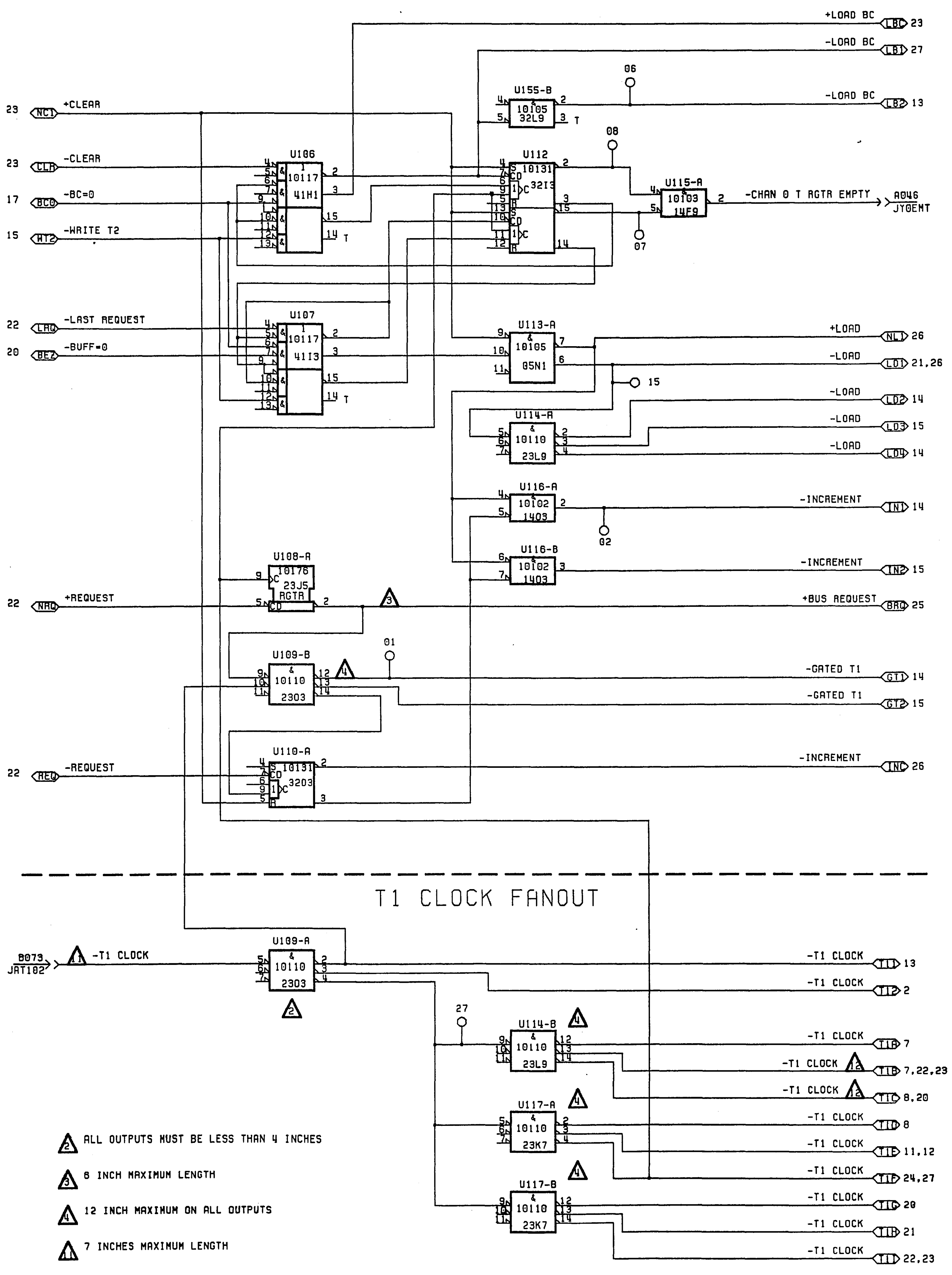
△4 12 INCH MAXIMUM LENGTH

△9 2 INCH MAXIMUM LENGTH

△10 9 INCH MINIMUM LENGTHS (EXCLUDING PINS 2 & 3 OF U100 AND PINS 4, 13, & 14 OF U102)

CONTROL DATA	CIO CHANNEL BOARD T REGISTER BITS 33-44, P1 RMA 52-63 TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 15	60462210	PAGE JY-15	

T REGISTER CONTROL (3.2)



△2 ALL OUTPUTS MUST BE LESS THAN 4 INCHES

△3 8 INCH MAXIMUM LENGTH

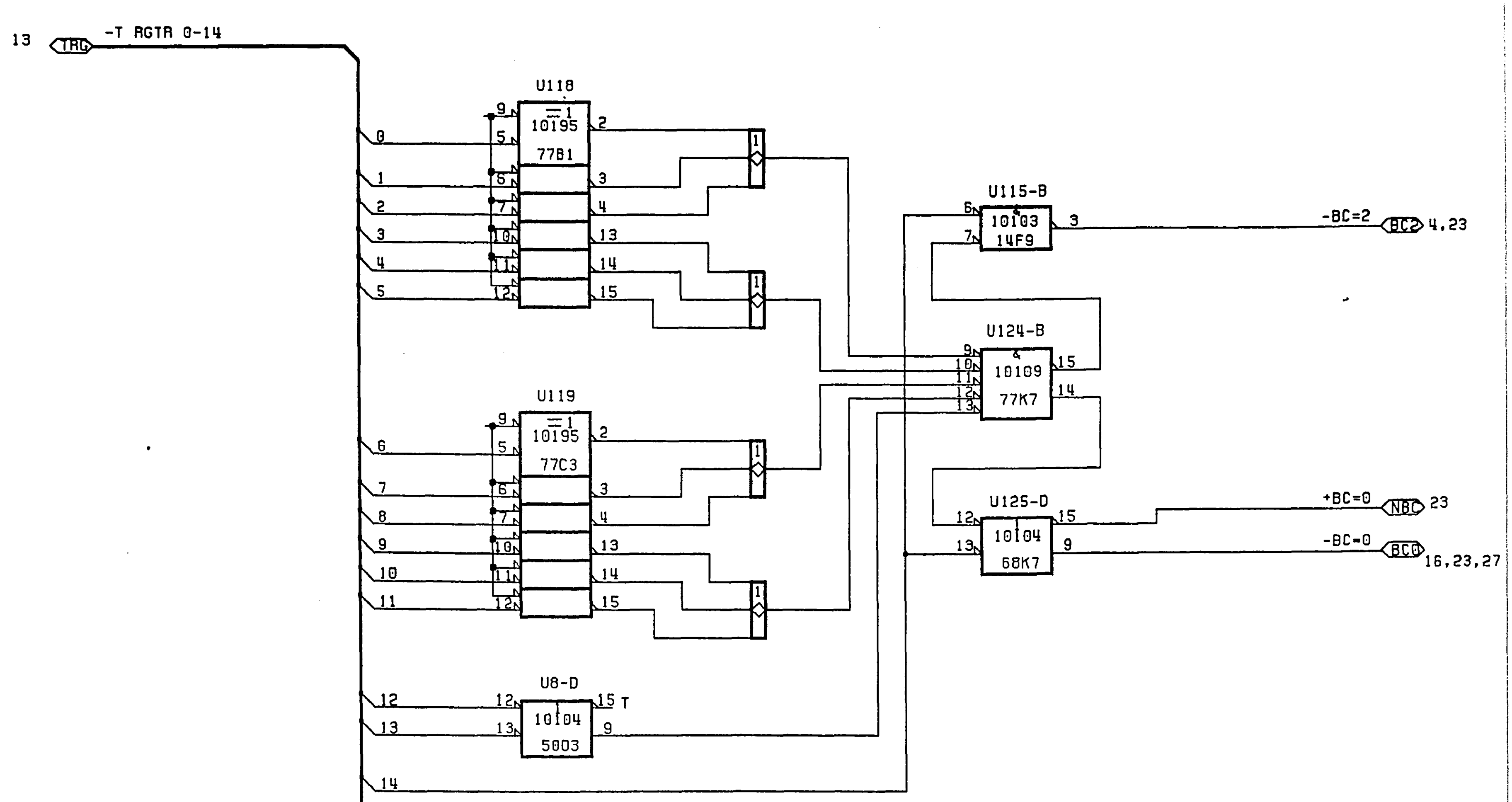
△4 12 INCH MAXIMUM ON ALL OUTPUTS

△11 7 INCHES MAXIMUM LENGTH

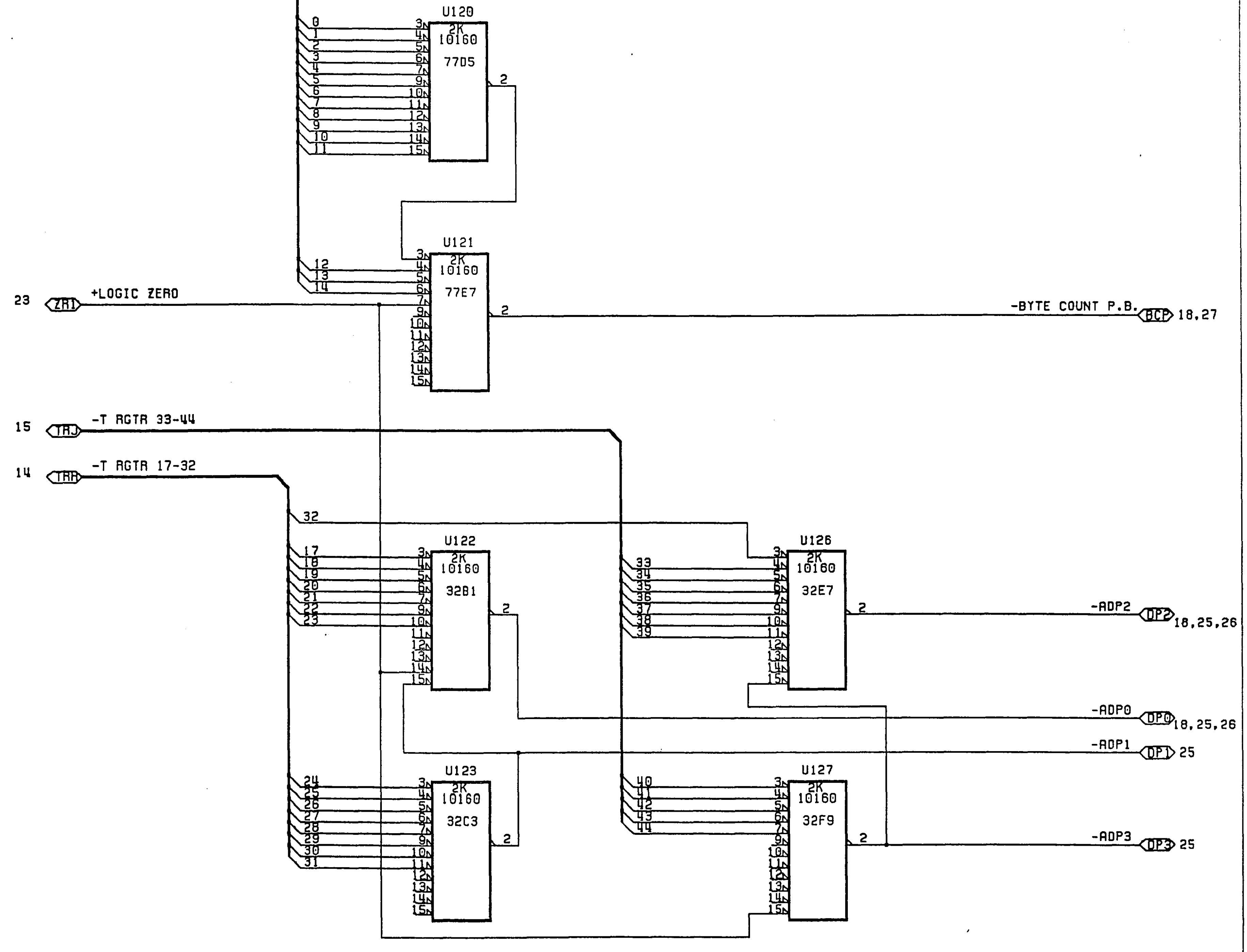
△12 GO TO PAGES 20 & 22 FIRST

CONTROL DATA	CIO CHANNEL BOARD T REGISTER CONTROL T1 CLOCK FANOUT TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
			SHEET NO. 16	60462210	PAGE JY-16

BYTE COUNT = 2 OR 0 TEST (3.3)

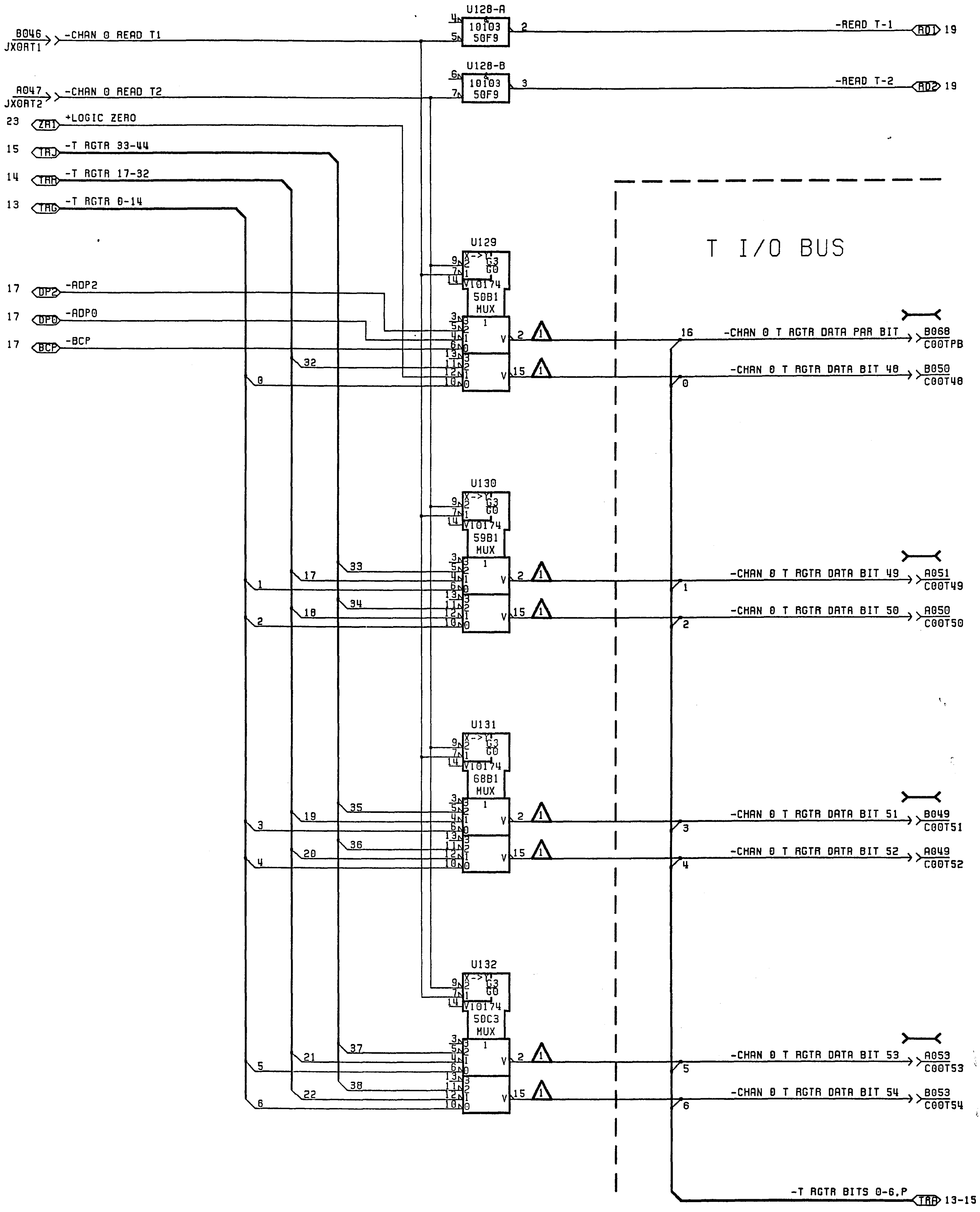


T REGISTER PARITY GENERATOR (3.3)



CONTROL DATA	CIO CHANNEL BOARD BYTE COUNT = 2 OR 0 TEST T REGISTER PARITY GENERATOR TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 17	60462210	PAGE JY-17	

T REGISTER MUX BITS 0-6,PAR (3.2)



B046
JX0RT1
-CHAN 0 READ T1
A047
JX0RT2
-CHAN 0 READ T2
23 ZR1 +LOGIC ZERO
15 TRJ -T RGTR 33-44
14 TRR -T RGTR 17-32
13 TRG -T RGTR 0-14
17 DP2 -ADP2
17 DP0 -ADP0
17 BCP -BCP
U128-A
10103
50F9
U128-B
10103
50F9
-READ T-1 RD1 19
-READ T-2 RD2 19
U129
10174
50B1
MUX
U130
10174
59B1
MUX
U131
10174
68B1
MUX
U132
10174
50C3
MUX
T I/O BUS
16 -CHAN 0 T RGTR DATA PAR BIT B068 C00TPB
0 -CHAN 0 T RGTR DATA BIT 48 B050 C00T48
1 -CHAN 0 T RGTR DATA BIT 49 A051 C00T49
2 -CHAN 0 T RGTR DATA BIT 50 A050 C00T50
3 -CHAN 0 T RGTR DATA BIT 51 B049 C00T51
4 -CHAN 0 T RGTR DATA BIT 52 A049 C00T52
5 -CHAN 0 T RGTR DATA BIT 53 A053 C00T53
6 -CHAN 0 T RGTR DATA BIT 54 B053 C00T54
-T RGTR BITS 0-6,P TRR 13-15
32
17
18
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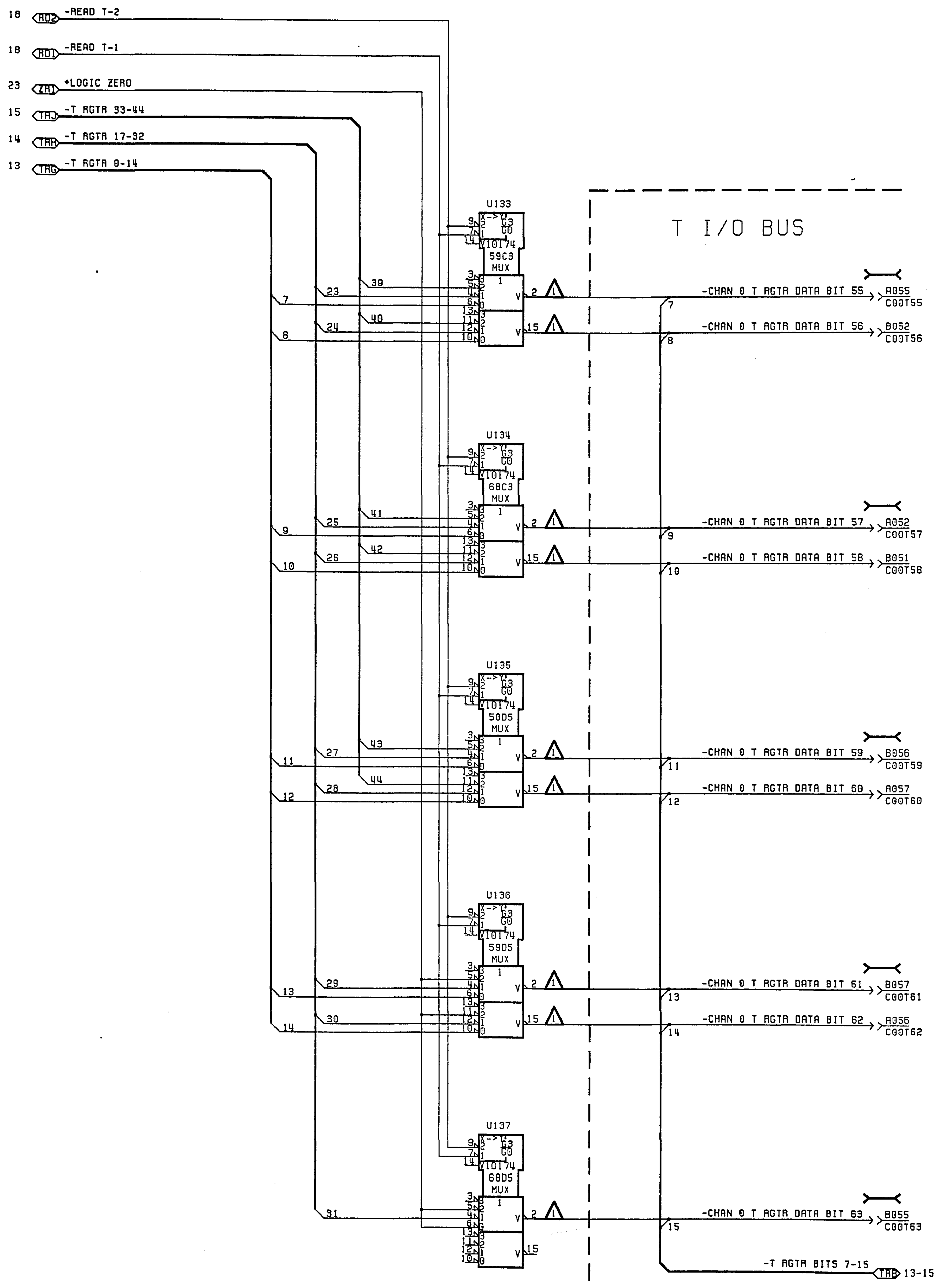
33
34
35
36
37
38

△1 TERMINATE AT FARTHEST POINT FROM CONNECTOR PIN

CONTROL DATA	CIO CHANNEL BOARD T REGISTER MUX BITS 0-6,PB T I/O BUS TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 18	60462210	PAGE JY-18	

T REGISTER MUX BITS 7-15 (3.2)


18 RD2 -READ T-2
18 RD1 -READ T-1
23 ZR1 +LOGIC ZERO
15 TRJ -T RGTR 33-44
14 TRH -T RGTR 17-32
13 TRG -T RGTR 0-14
T I/O BUS
U133 10174 59C3 MUX
U134 10174 68C3 MUX
U135 10174 50D5 MUX
U136 10174 59D5 MUX
U137 10174 68D5 MUX
-CHAN 0 T RGTR DATA BIT 55 A055 C00T55
-CHAN 0 T RGTR DATA BIT 56 B052 C00T56
-CHAN 0 T RGTR DATA BIT 57 A052 C00T57
-CHAN 0 T RGTR DATA BIT 58 B051 C00T58
-CHAN 0 T RGTR DATA BIT 59 B056 C00T59
-CHAN 0 T RGTR DATA BIT 60 A057 C00T60
-CHAN 0 T RGTR DATA BIT 61 B057 C00T61
-CHAN 0 T RGTR DATA BIT 62 A056 C00T62
-CHAN 0 T RGTR DATA BIT 63 B055 C00T63
-T RGTR BITS 7-15 TRB 13-15

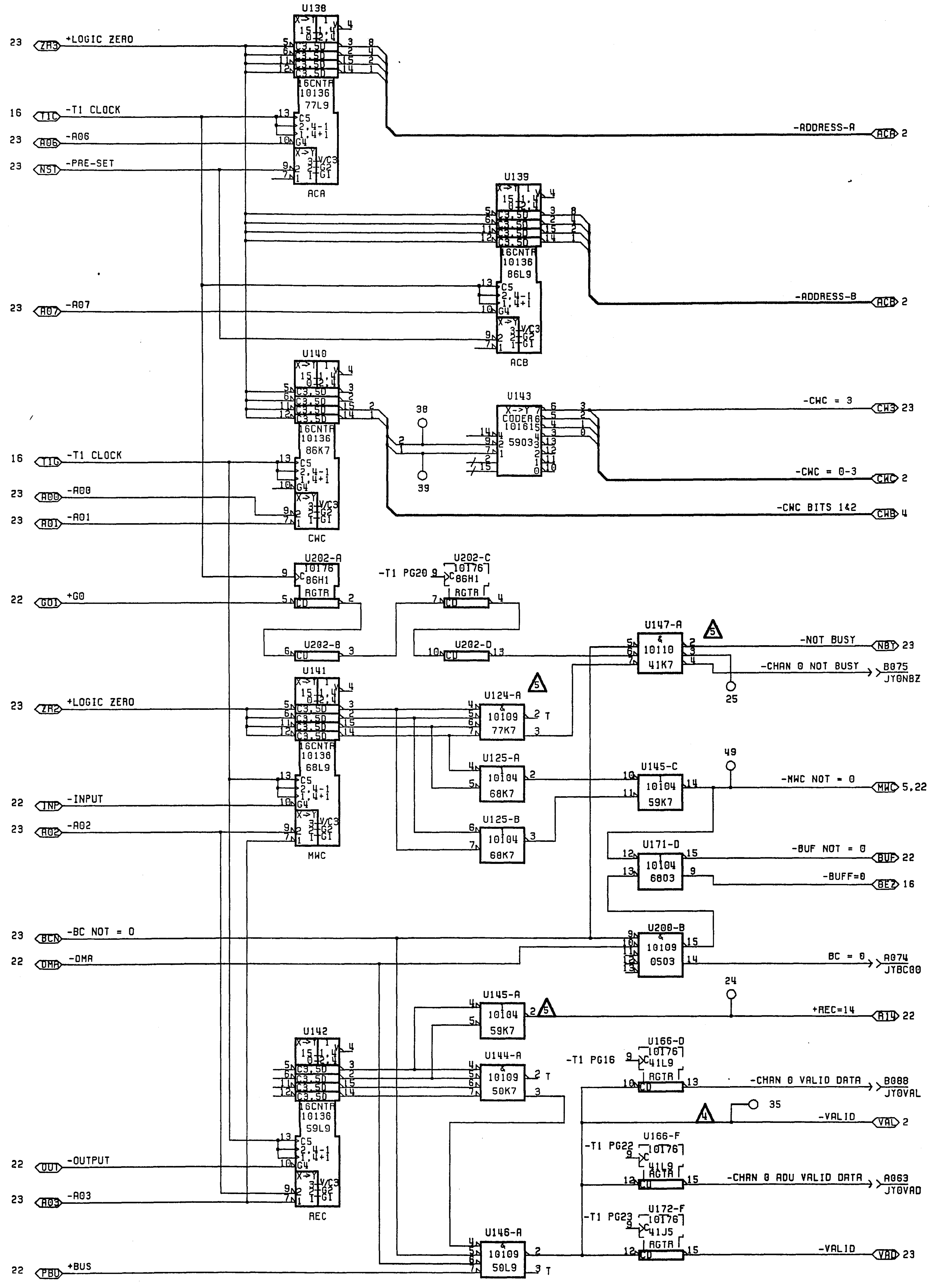
1 TERMINATE AT FARTHEST POINT FROM CONNECTOR PIN

CONTROL DATA

CIO CHANNEL BOARD
T REGISTER MUX BITS 7-15
T I/O BUS
TYPE 1JYH

B	DWG NO. 53575513	DATE 04/07/86	REV A
SHEET NO. 19	60462210	PAGE JY-19	

COUNTERS (3.4)

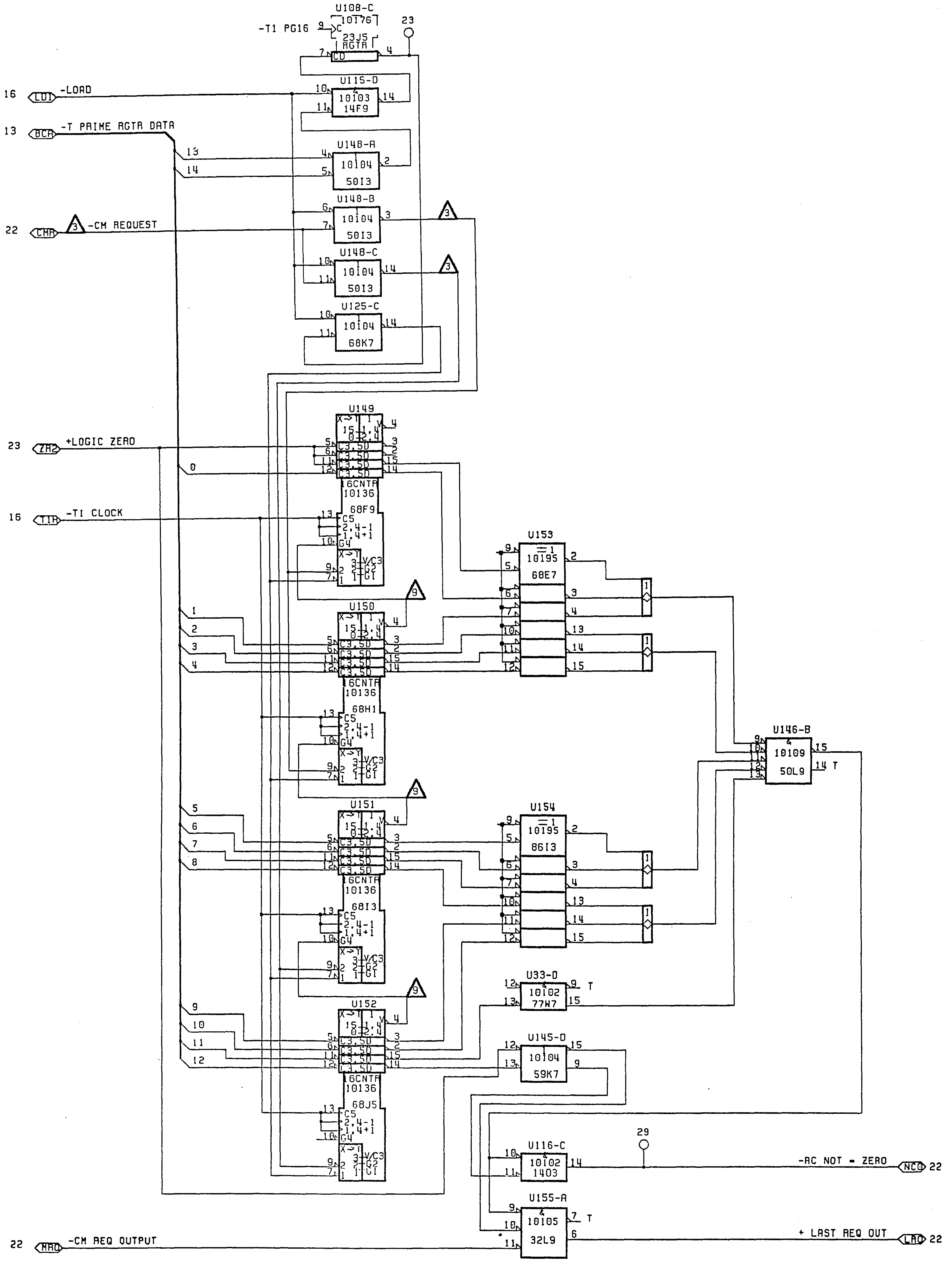


4 12 INCH MAXIMUM

5 3 INCH MAXIMUM LENGTH ON ALL INPUT/OUTPUT PINS UNLESS OTHERWISE INDICATED

CONTROL DATA	CIO CHANNEL BOARD COUNTERS TYPE 1JYH	B	DWG NO. 53575513	DATE 04/21/86	REV A
		SHEET NO. 20	60462210	PAGE JY-20	

REQUEST COUNTER (3.5)

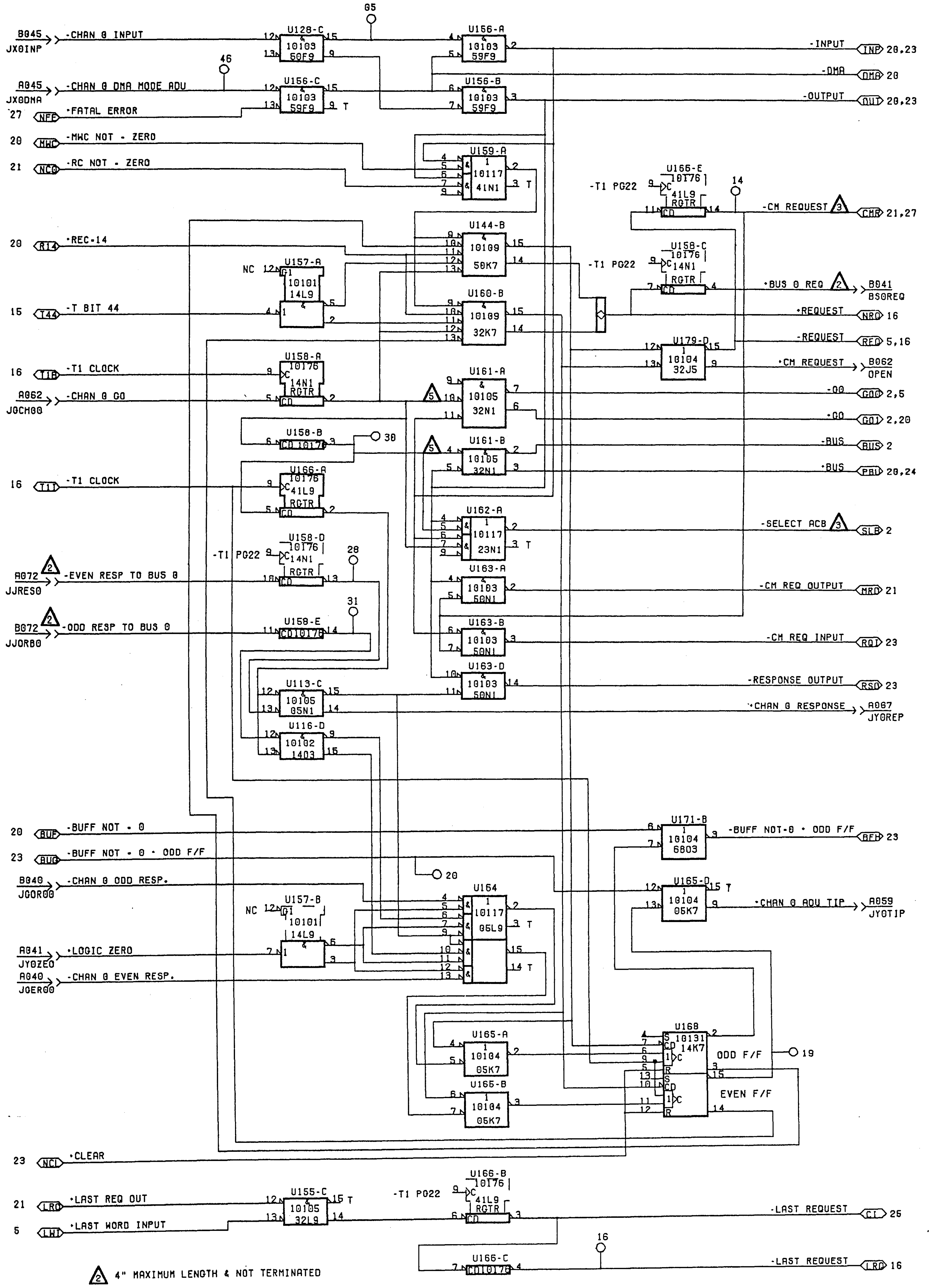


△3 6 INCH MAXIMUM LENGTH

△9 2 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD REQUEST COUNTER	B	DWG NO. 53575513	DATE 04/07/86	REV A
	TYPE 1JYH	N	SHEET NO. 21	60462210	PAGE JY-21

CHANNEL GO/CM REQUEST/CM RESPONSE (3.5)



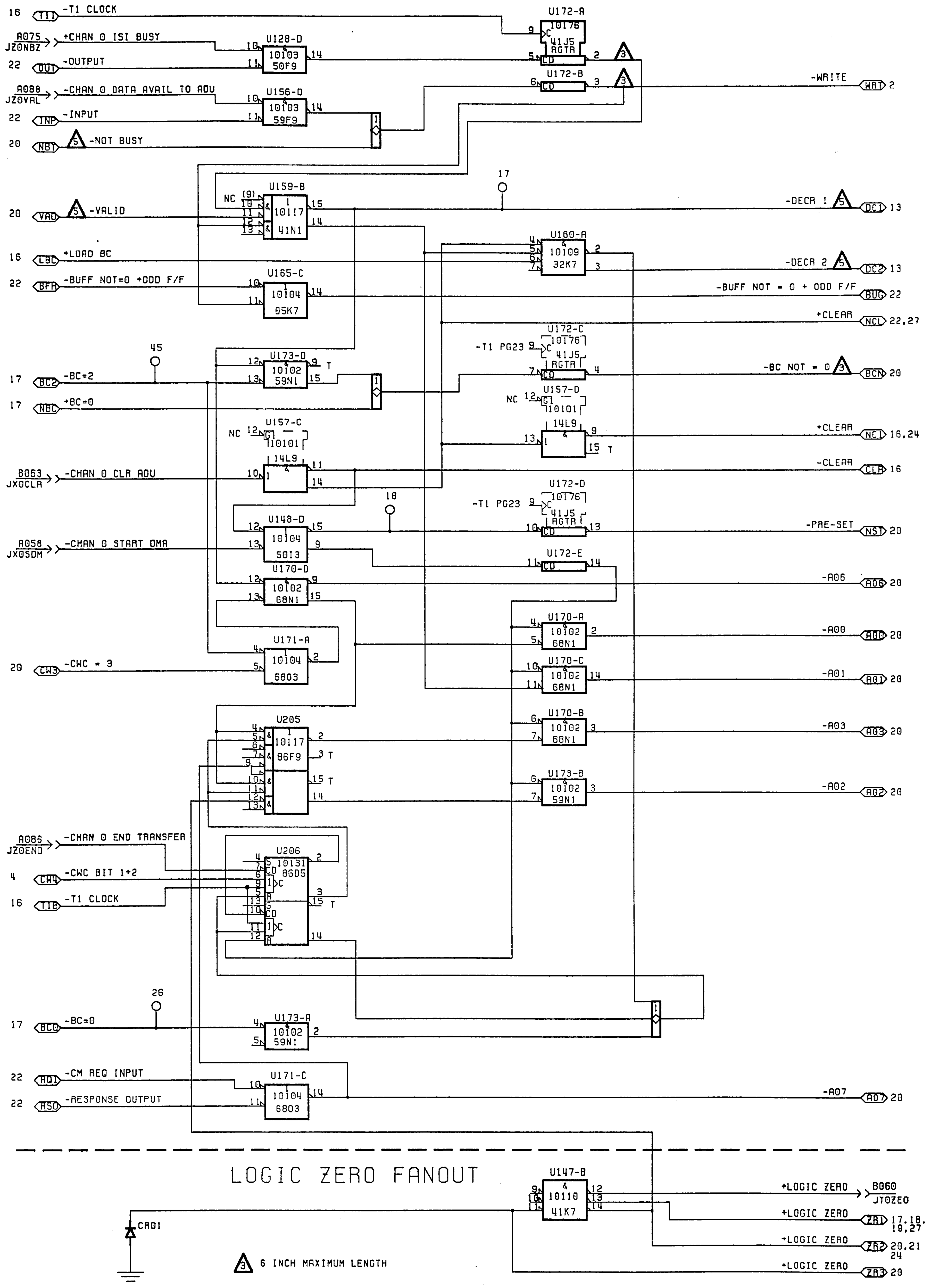
△2 4" MAXIMUM LENGTH & NOT TERMINATED

△3 6 INCH MAXIMUM LENGTH

△5 3 INCH MAXIMUM LENGTH TO 10117 & 9 INCH MAX TOTAL LENGTH

CONTROL DATA	CIO CHANNEL BOARD CHANNEL GO / CM REQUEST / CM RESPONSE TYPE 1JYH	B	DWG NO. 53575513	DATE 06/14/88	REV D
		N	SHEET NO. 22	60462210	PAGE JY-22

COUNTER CONTROL (3.4)



LOGIC ZERO FANOUT

3 6 INCH MAXIMUM LENGTH

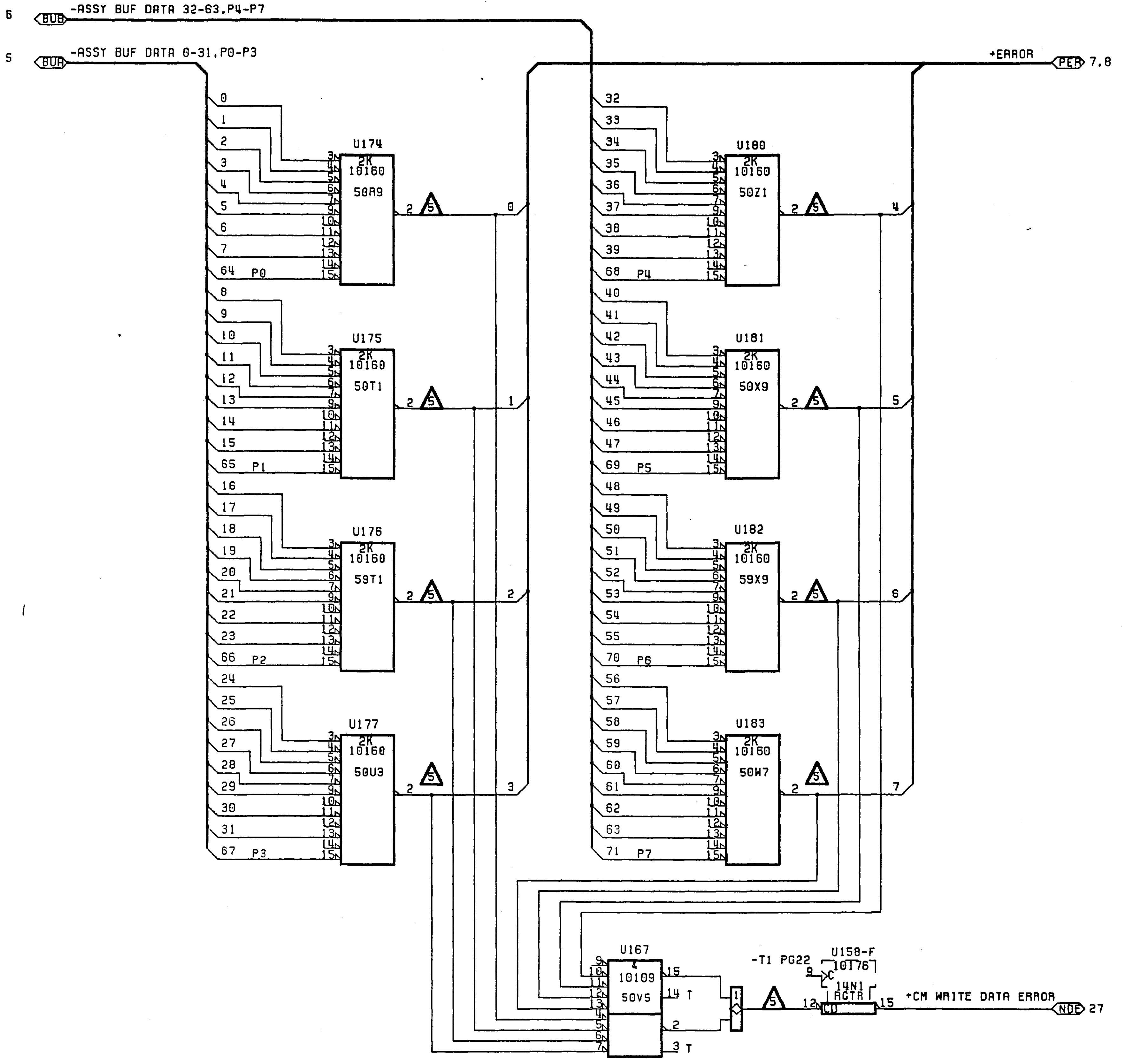
5 3 INCH MAXIMUM LENGTH

CONTROL DATA

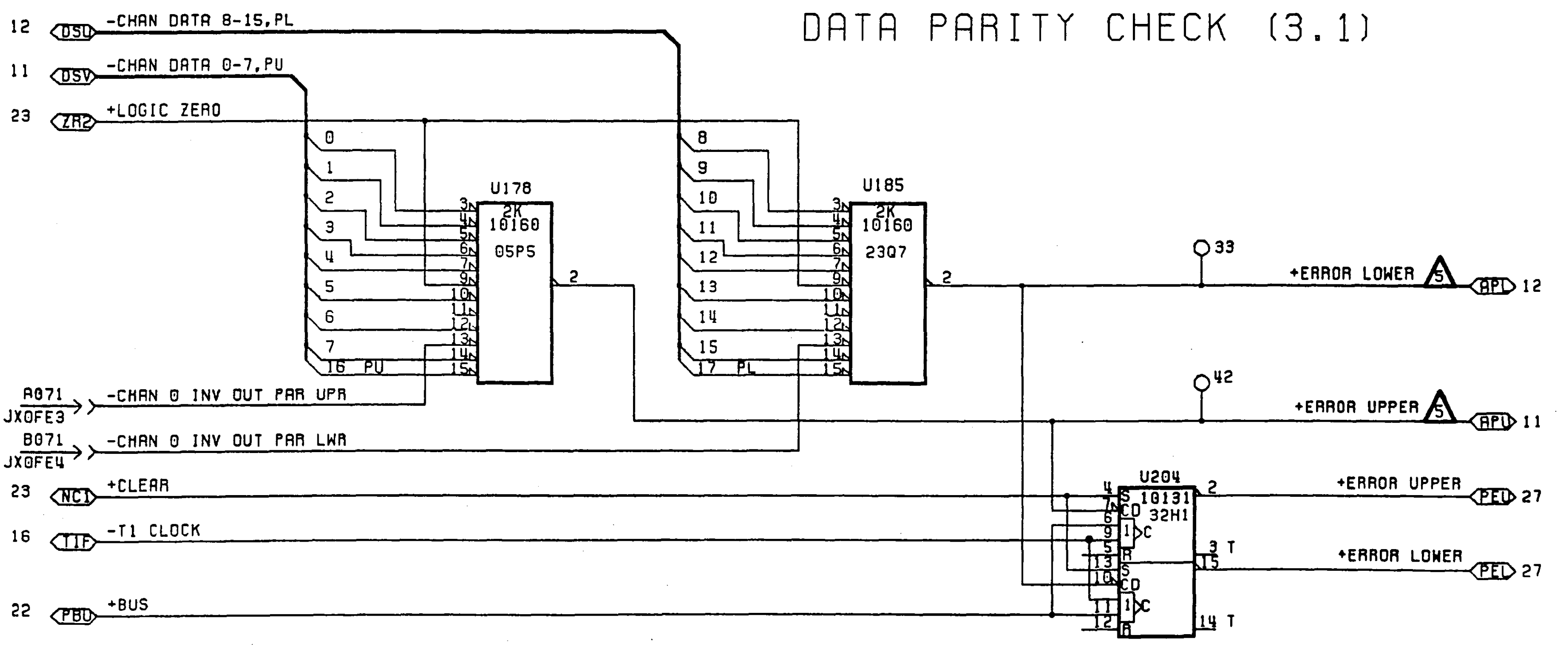
CIO CHANNEL BOARD
COUNTER CONTROL &
LOGIC ZERO FANOUT
TYPE 1JYH

B	DWG NO. 53575513	DATE 04/21/86	REV A
SHEET NO. 23	60462210	PAGE JT-23	

DATA PARITY CHECK (3.0)



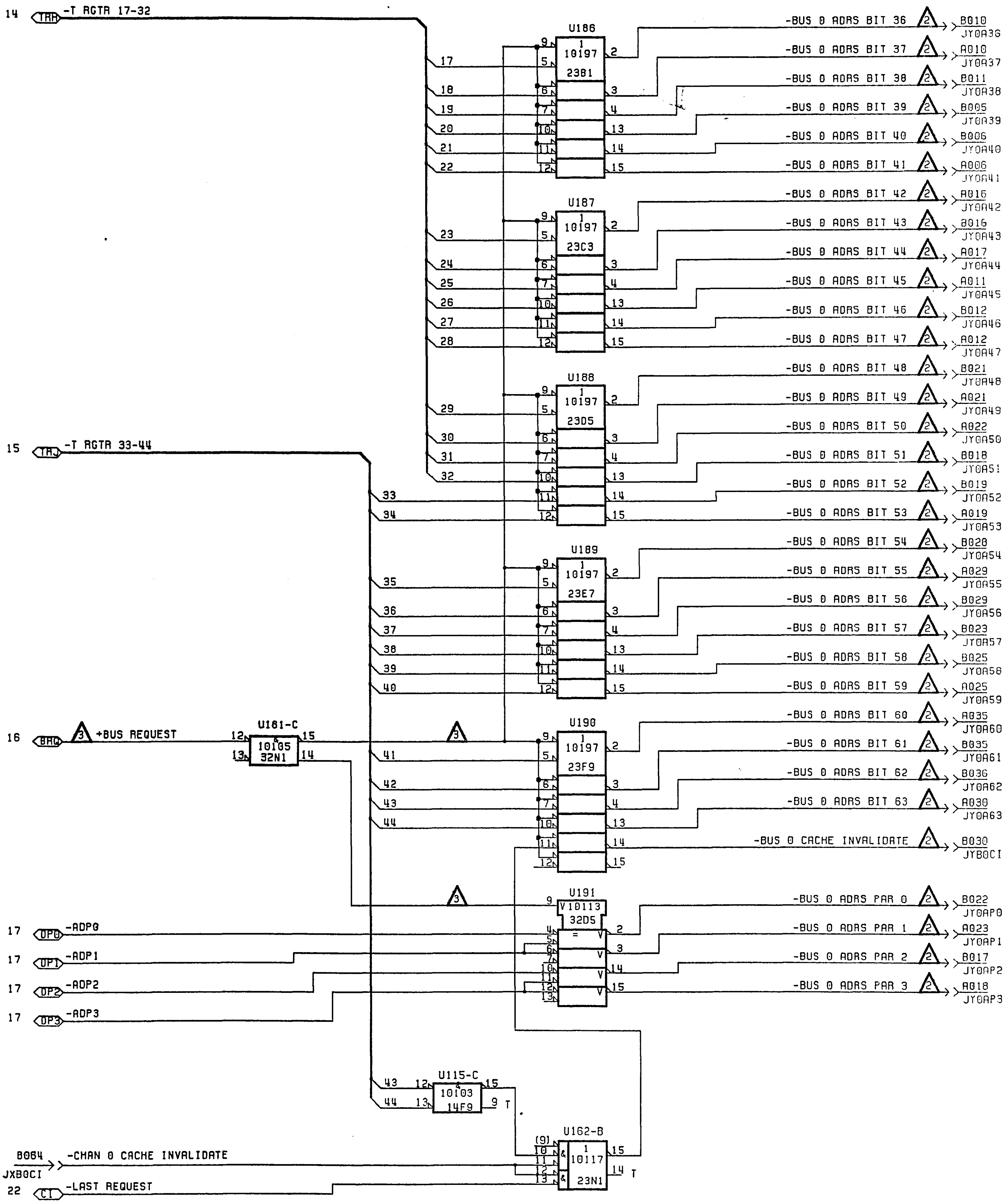
DATA PARITY CHECK (3.1)



⚠5 3 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD DATA PARITY CHECK TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 24	60462210	PAGE JY-24	

CM ADDRESS TO CMI (3.3)


14 TRA -T RGTR 17-32
15 TRJ -T RGTR 33-44
16 BRQ +BUS REQUEST
17 DP0 -ADP0
17 DP1 -ADP1
17 DP2 -ADP2
17 DP3 -ADP3
B064 JXB0CI -CHAN 0 CACHE INVALIDATE
22 CI -LAST REQUEST
U186 10197 23B1
U187 10197 23C3
U188 10197 23D5
U189 10197 23E7
U190 10197 23F9
U191 10113 32D5
U161-C 10105 32N1
U115-C 10103 14F9
U162-B 10117 23N1
-BUS 0 ADRS BIT 36 B010 JY0A36
-BUS 0 ADRS BIT 37 A010 JY0A37
-BUS 0 ADRS BIT 38 B011 JY0A38
-BUS 0 ADRS BIT 39 B005 JY0A39
-BUS 0 ADRS BIT 40 B006 JY0A40
-BUS 0 ADRS BIT 41 A006 JY0A41
-BUS 0 ADRS BIT 42 A016 JY0A42
-BUS 0 ADRS BIT 43 B016 JY0A43
-BUS 0 ADRS BIT 44 A017 JY0A44
-BUS 0 ADRS BIT 45 A011 JY0A45
-BUS 0 ADRS BIT 46 B012 JY0A46
-BUS 0 ADRS BIT 47 A012 JY0A47
-BUS 0 ADRS BIT 48 B021 JY0A48
-BUS 0 ADRS BIT 49 A021 JY0A49
-BUS 0 ADRS BIT 50 A022 JY0A50
-BUS 0 ADRS BIT 51 B018 JY0A51
-BUS 0 ADRS BIT 52 B019 JY0A52
-BUS 0 ADRS BIT 53 A019 JY0A53
-BUS 0 ADRS BIT 54 B028 JY0A54
-BUS 0 ADRS BIT 55 A029 JY0A55
-BUS 0 ADRS BIT 56 B029 JY0A56
-BUS 0 ADRS BIT 57 B023 JY0A57
-BUS 0 ADRS BIT 58 B025 JY0A58
-BUS 0 ADRS BIT 59 A025 JY0A59
-BUS 0 ADRS BIT 60 A035 JY0A60
-BUS 0 ADRS BIT 61 B035 JY0A61
-BUS 0 ADRS BIT 62 B036 JY0A62
-BUS 0 ADRS BIT 63 A030 JY0A63
-BUS 0 CACHE INVALIDATE B030 JYB0CI
-BUS 0 ADRS PAR 0 B022 JY0AP0
-BUS 0 ADRS PAR 1 A023 JY0AP1
-BUS 0 ADRS PAR 2 B017 JY0AP2
-BUS 0 ADRS PAR 3 A018 JY0AP3

2: 4" MAXIMUM LENGTH & NOT TERMINATED

3: 6" MAXIMUM LENGTH

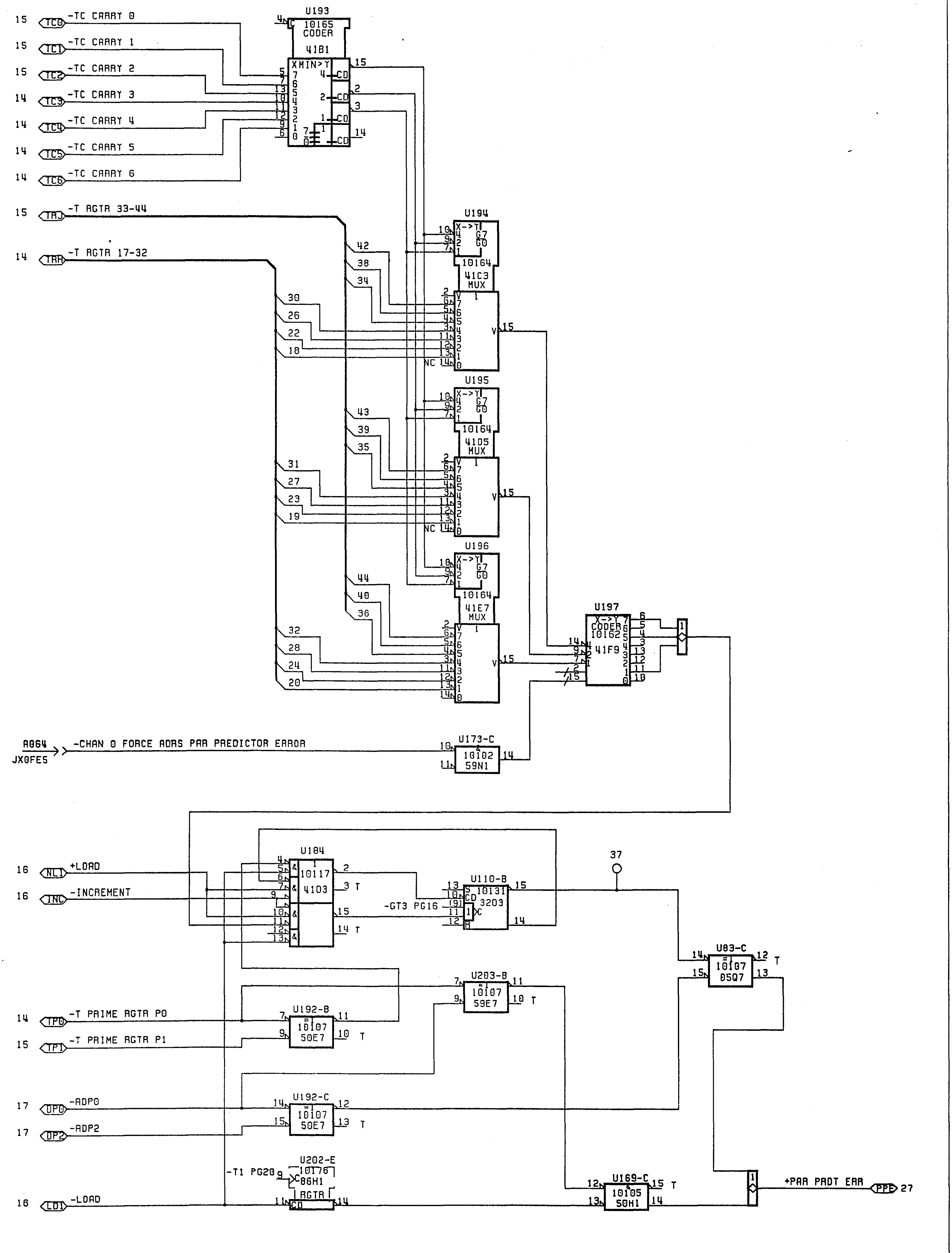
CONTROL DATA

CIO CHANNEL BOARD
CM ADDRESS TO CMI
TYPE 1JYH

B

DWG NO. 53575513
DATE 04/07/86
REV A
SHEET NO. 25
60462210
PAGE JY-25

RMA PARITY PREDICTION (3.6)



CONTROL DATA

CIO CHANNEL BOARD
RMA PARITY PREDICTION
TYPE 1JYH

B

DWG NO. 53575513

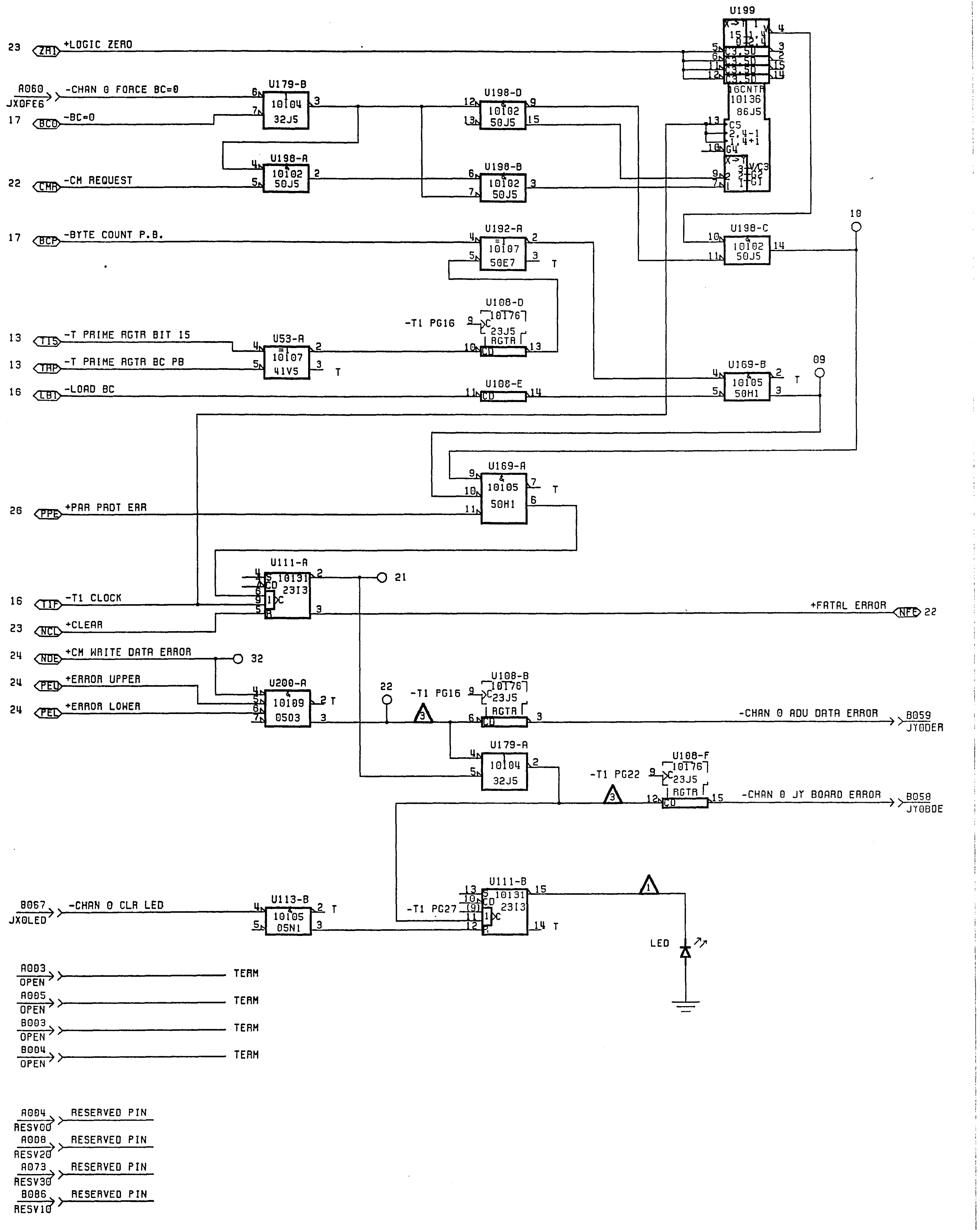
DATE 04/07/86

REV A

SHEET NO. 26 60462210

PAGE JY-26

ERROR FANIN (3.6)



△1 THIS LINE MUST BE TERMINATED

△3 6 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ERROR FANIN TYPE 1JYH	B	DWG NO. 53575513	DATE 04/07/86	REV A
		SHEET NO. 27	60462210	PAGE JY-27	

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	16	-GATED T1 CLOCK	27	16	-T1 CLOCK
02	16	-INCREMENT RMA	28	22	-RESPONSE
03	15	-RMA BIT 44	29	21	-REQ CNT NOT ZERO
04	13	-BC BIT 14	30	22	-CHANNEL GO
05	22	-INPUT	31	22	-ODD RESPONSE FLAG
06	16	-LOAD BYTE COUNT	32	27	+CM WRITE DATA ERROR
07	16	-RMA T PRIME EMPTY	33	24	+OUTPUT LOWER ERROR
08	16	-BC T PRIME EMPTY	34	02	-BUFFER ADRS BIT 3
09	27	+BYTE COUNT ERROR	35	20	-VALID OUTPUT DATA
10	27	+CM REQUEST ERROR	36	11	-OUTPUT DATA BIT 0
11	13	+WR T REG BITS 0-15	37	26	-PAR PREDICTOR F/F
12	15	+WR T REG BITS 32-47	38	20	-CWC BIT 1
13	14	+WR T REG BITS 16-31	39	20	-CWC BIT 0
14	22	-CM REQUEST	40	02	-BUFFER ADRS BIT 1
15	16	+LOAD RMA	41	02	-BUFFER ADRS BIT 2
16	22	-LAST CM REQUEST	42	24	+OUTPUT UPPER ERROR
17	23	-DECREMENT BYTE CNT	43	02	-BUFFER ADRS BIT 0
18	23	-CLEAR	44	02	-SELECT ADDRESS B
19	22	-EVEN REQUEST OUT	45	23	-BYTE COUNT EQUAL 2
20	22	-BUFF FULL/ODD REQ	46	22	-DMA MODE
21	27	-FATAL ERROR	47	05	-DATA BIT 0 TO CM
22	27	-DATA ERROR	48	05	-DATA BIT 16 TO CM
23	21	-INCREMENT REQ CNTR	49	20	-MWC NOT EQUAL ZERO
24	20	+RESPONSE CNT = 14	50	06	-DATA BIT 48 TO CM
25	20	+BUSY	51	06	-DATA BIT 32 TO CM
26	23	-BYTE COUNT = ZERO			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117,A037,A038,B037,B038,B128
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070
TERM	A003,B003,B004,A005
UNUSED	A004,A008,B008,A009,B009,A013,B013,A015,B015,A020,B020,A026,B026,A027,B027,A028,A031,B031,A032,B032,A033,B033,A036,A037,B037,A038,B038,A039,B039,A074,B074

CONTROL DATA	CIO CHANNEL BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JYH	B	DWG NO. 53575513	DATE 12/02/85	REV A
	N	SHEET NO. 28	60462210	PAGE JY-28	

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1JYH CIO CHANNEL BOARD

REVISION HISTORY B/M 41652701			
DATE	REV	DESCRIPTION OF CHANGE	INIT
03/14/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	
01/21/88	B	ECO #49505 DIAGRAM CORRECTIONS TO	
		SHEET 22.	DS
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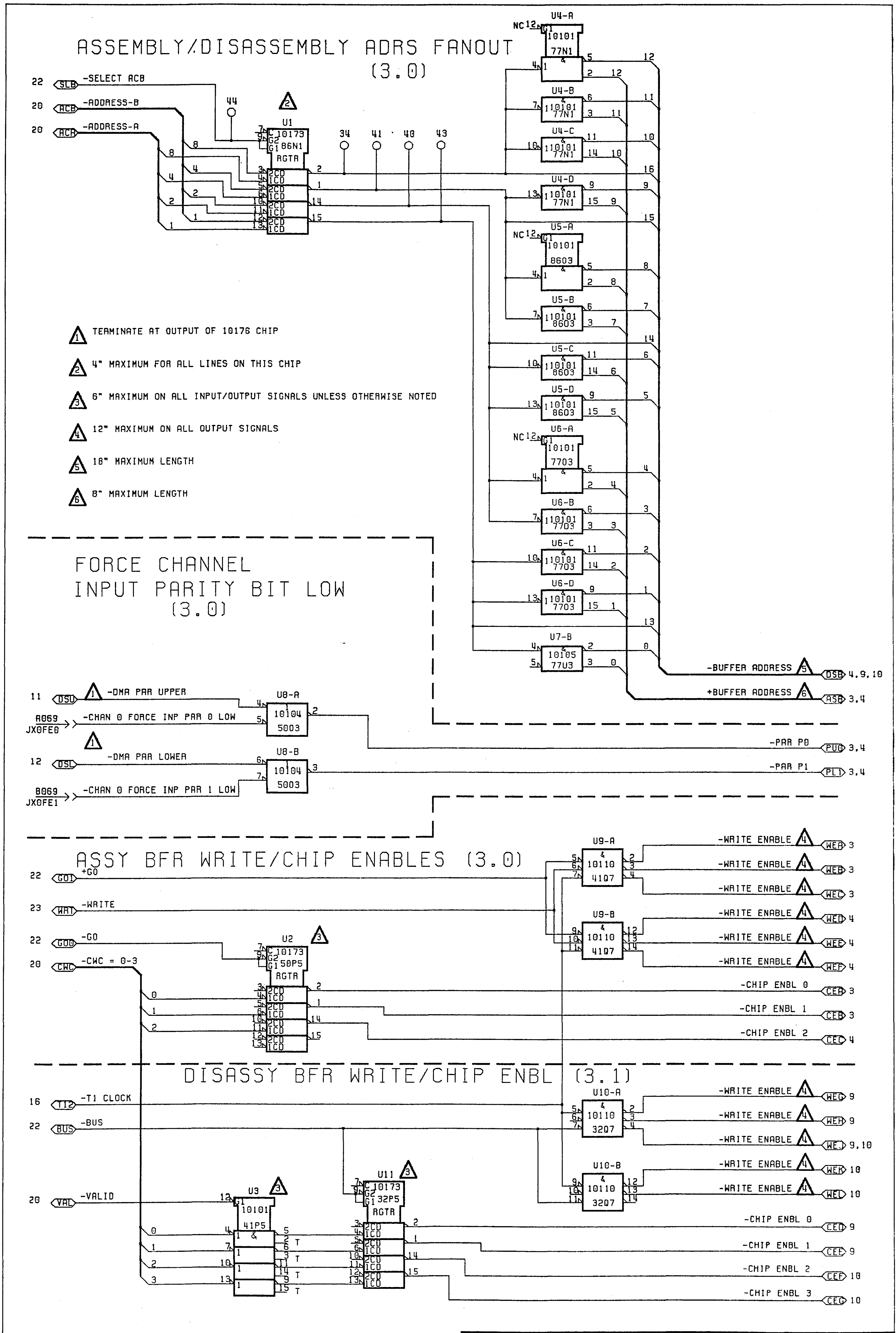
DWN	L H JOHNSON	03/14/86
CHKD		
ENG		
PUBS		
APP		

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED
LOC: D10,D13,D16,D19,D22
C10,C13,C16,C19,C22

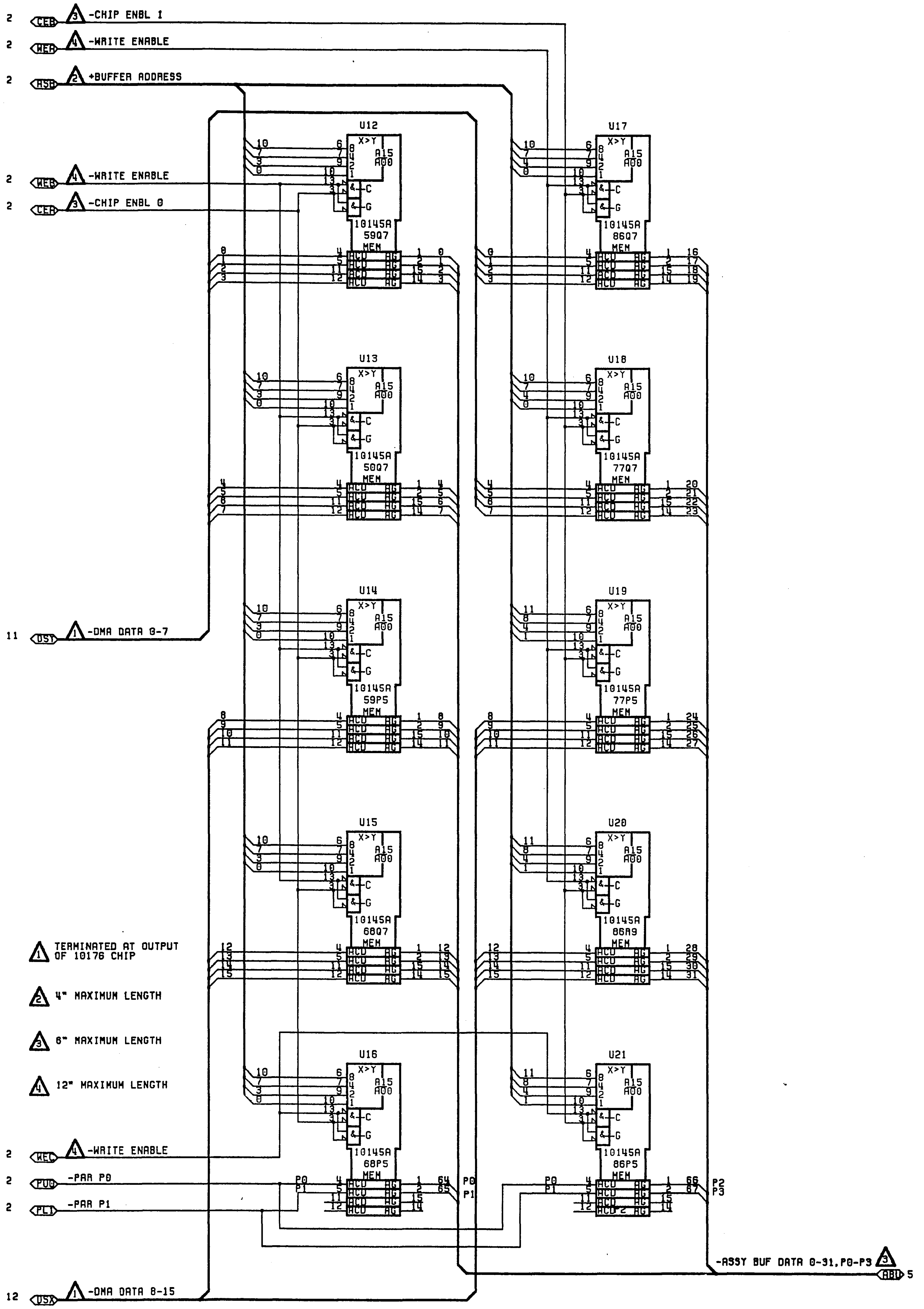
CONTROL DATA	REVISION HISTORY	B	DWG NO. 22105622	DATE 06/14/88	REV B
	TYPE 1JYH		SHEET NO. 1	60462210	PAGE JY-01



1. TERMINATE AT OUTPUT OF 10176 CHIP
2. 4" MAXIMUM FOR ALL LINES ON THIS CHIP
3. 6" MAXIMUM ON ALL INPUT/OUTPUT SIGNALS UNLESS OTHERWISE NOTED
4. 12" MAXIMUM ON ALL OUTPUT SIGNALS
5. 18" MAXIMUM LENGTH
6. 8" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY/DISASSEMBLY ADDRESS, WRITE & CHIP ENABLE FANOUTS TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 2	60462210	PAGE JY-02	

ASSEMBLY BUFFER BITS 0-31,PAR 0-3 (3.0)



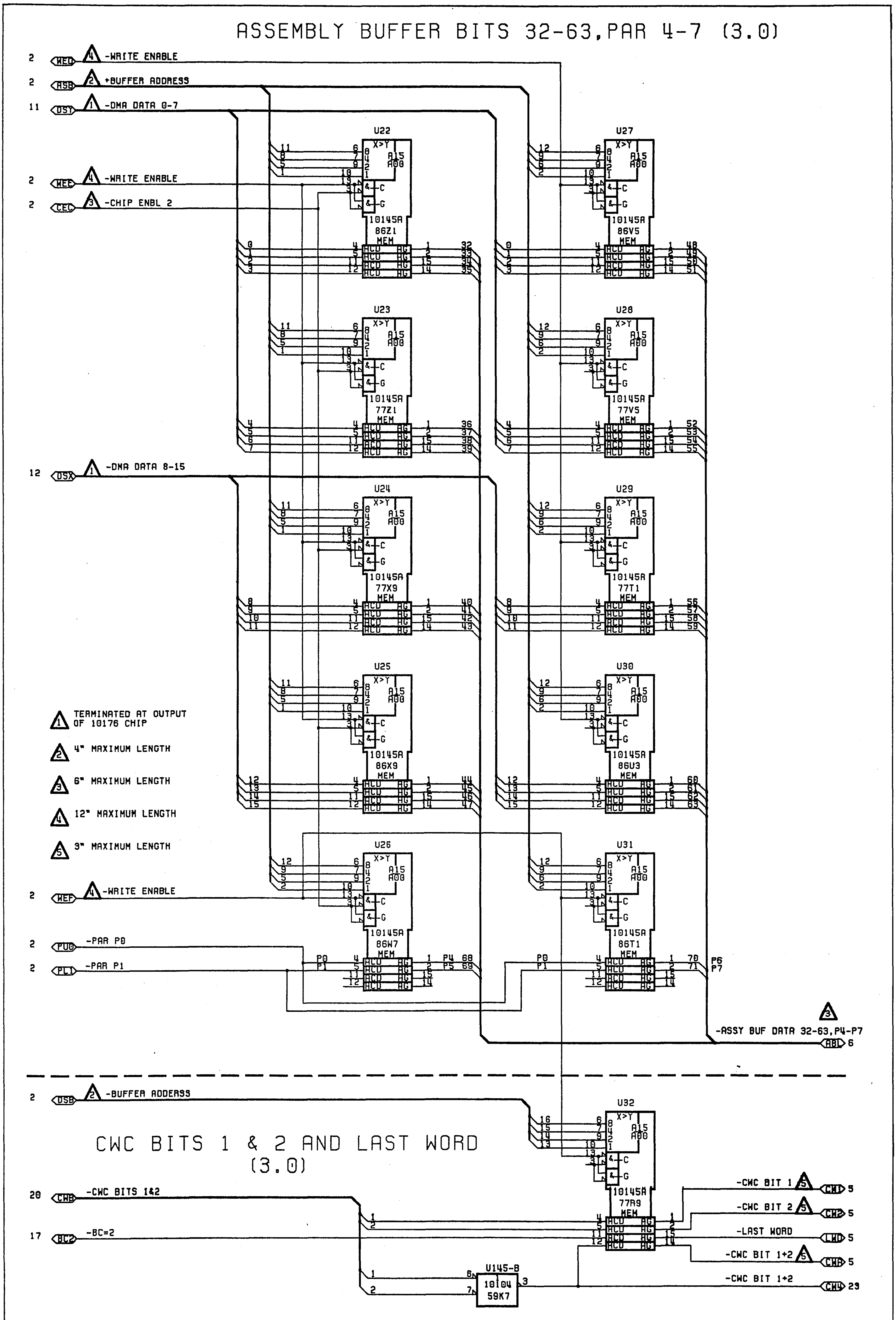
1 TERMINATED AT OUTPUT OF 10176 CHIP

2 4" MAXIMUM LENGTH

3 8" MAXIMUM LENGTH

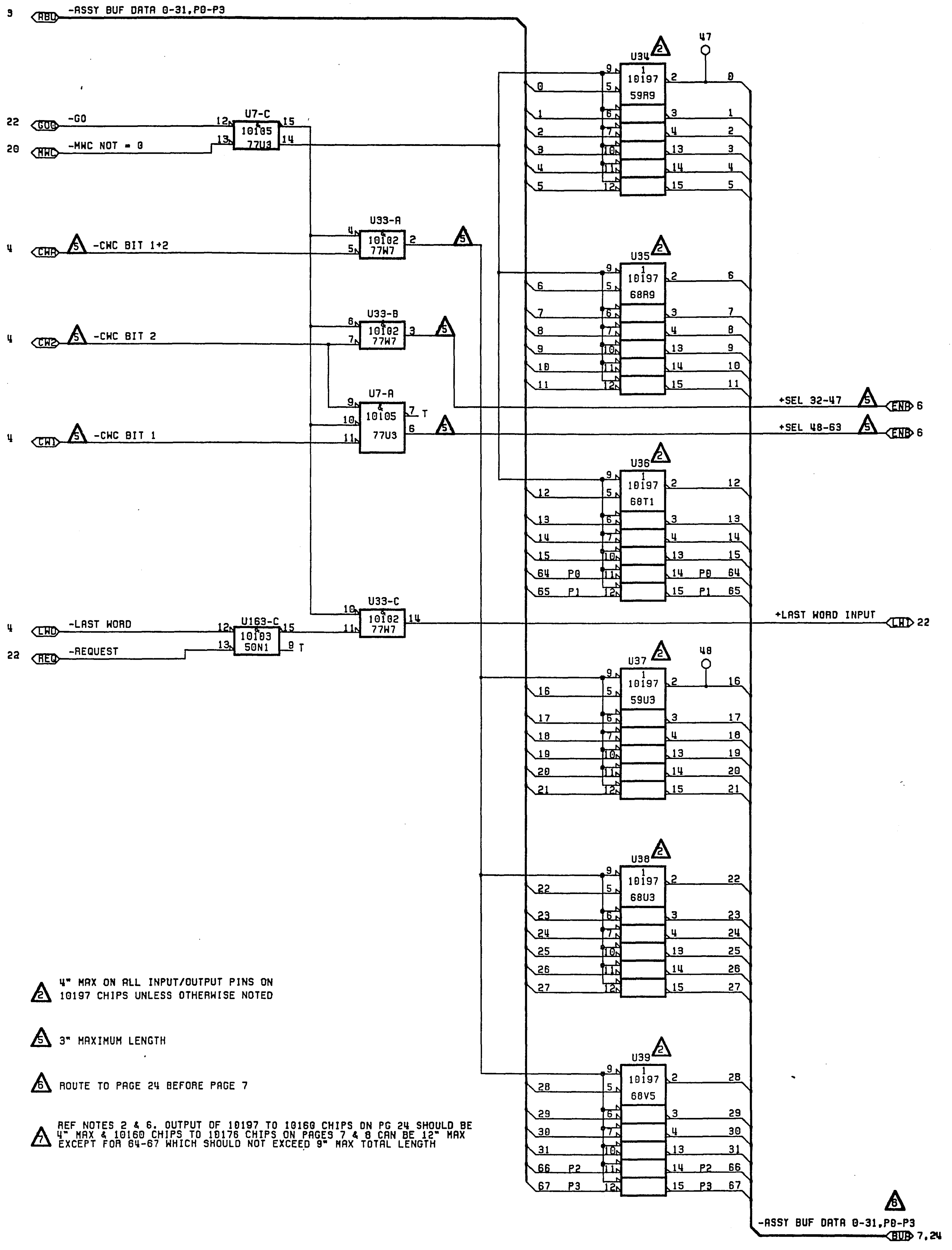
4 12" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER BITS 0-31,P0-P3	B	DWG NO. 22105622	DATE 03/14/86	REV A
	TYPE 1JYH	SHEET NO. 3	60442210	PAGE JY-03	



CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER BITS 32-63,P4-P7 CWC BITS 1 & 2 AND LAST WORD TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 4	60462210	PAGE JY-04	

SELECT 0-15,16-31 TO CM (3.0)



2 4" MAX ON ALL INPUT/OUTPUT PINS ON 10197 CHIPS UNLESS OTHERWISE NOTED

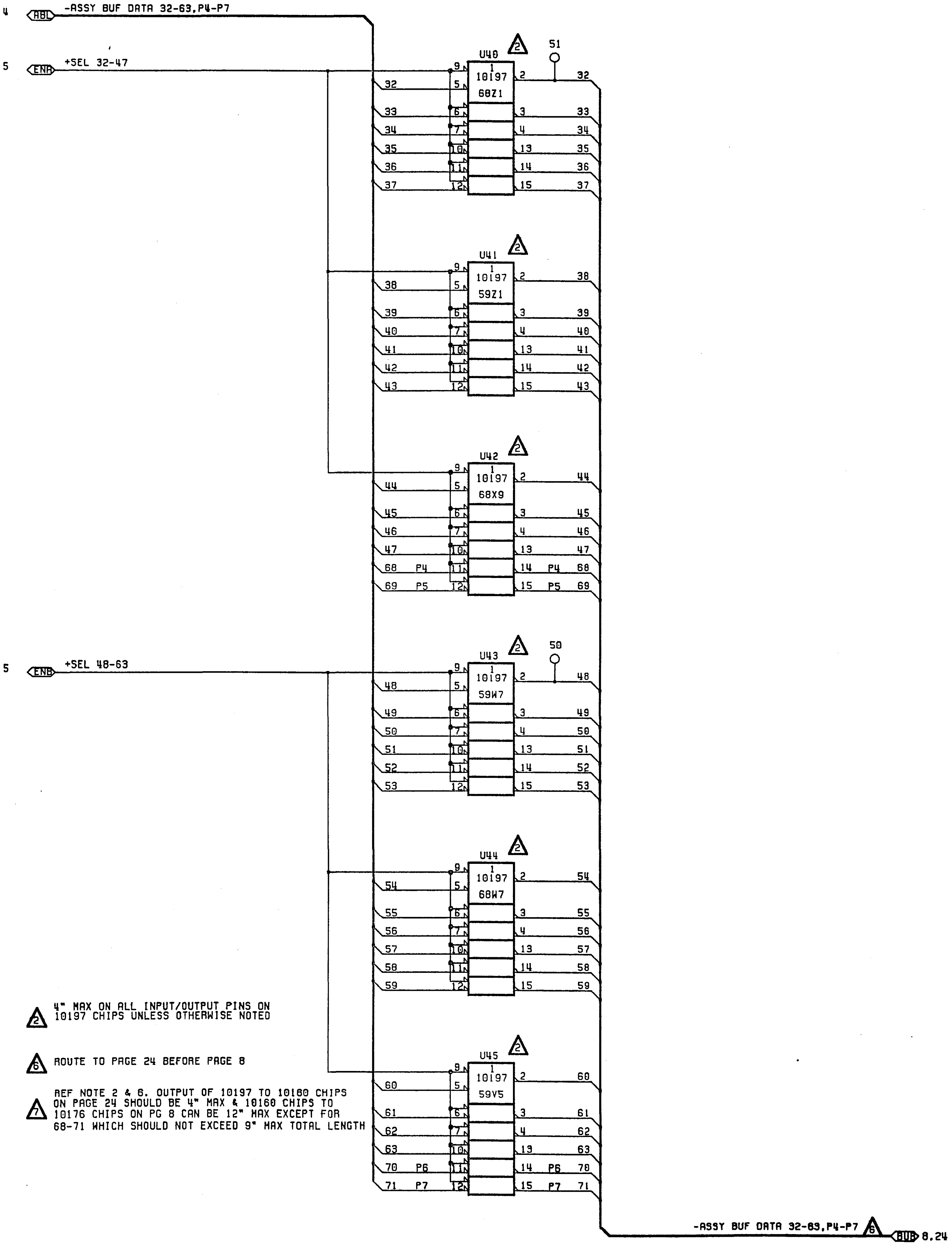
5 3" MAXIMUM LENGTH

6 ROUTE TO PAGE 24 BEFORE PAGE 7

7 REF NOTES 2 & 6. OUTPUT OF 10197 TO 10160 CHIPS ON PG 24 SHOULD BE 4" MAX & 10160 CHIPS TO 10176 CHIPS ON PAGES 7 & 8 CAN BE 12" MAX EXCEPT FOR 64-67 WHICH SHOULD NOT EXCEED 9" MAX TOTAL LENGTH

CONTROL DATA
CIO CHANNEL BOARD
SELECT 0-15,16-31 TO CM
TYPE 1JYH
B
DWG NO. 22105622
DATE 03/14/86
REV A
SHEET NO. 5
60462210
PAGE JY-05

SELECT 32-47,48-63 TO CM (3.0)



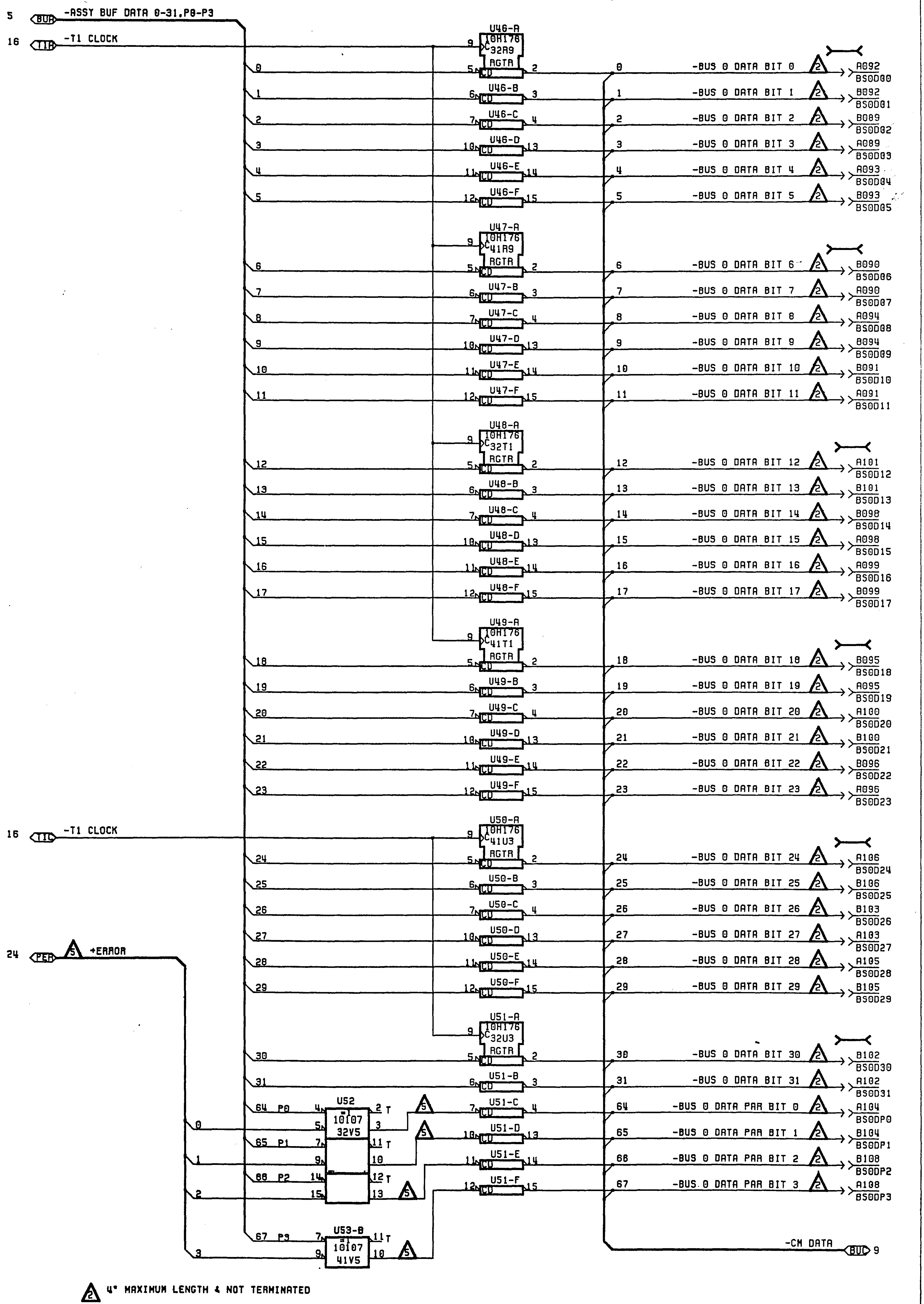
2 — 4" MAX ON ALL INPUT/OUTPUT PINS ON 10197 CHIPS UNLESS OTHERWISE NOTED

6 — ROUTE TO PAGE 24 BEFORE PAGE 8

7 — REF NOTE 2 & 6. OUTPUT OF 10197 TO 10160 CHIPS ON PAGE 24 SHOULD BE 4" MAX & 10160 CHIPS TO 10176 CHIPS ON PG 8 CAN BE 12" MAX EXCEPT FOR 68-71 WHICH SHOULD NOT EXCEED 9" MAX TOTAL LENGTH

CONTROL DATA	CIO CHANNEL BOARD SELECT 32-47,48-63 TO CM	B	DWG NO. 22105622	DATE 03/14/86	REV A
	TYPE 1JYH	SHEET NO. 6	60462210	PAGE JY-06	

ASSEMBLY BUFFER OUTPUT
REGISTER BITS 0-31, PAR 0-3 (3.1)



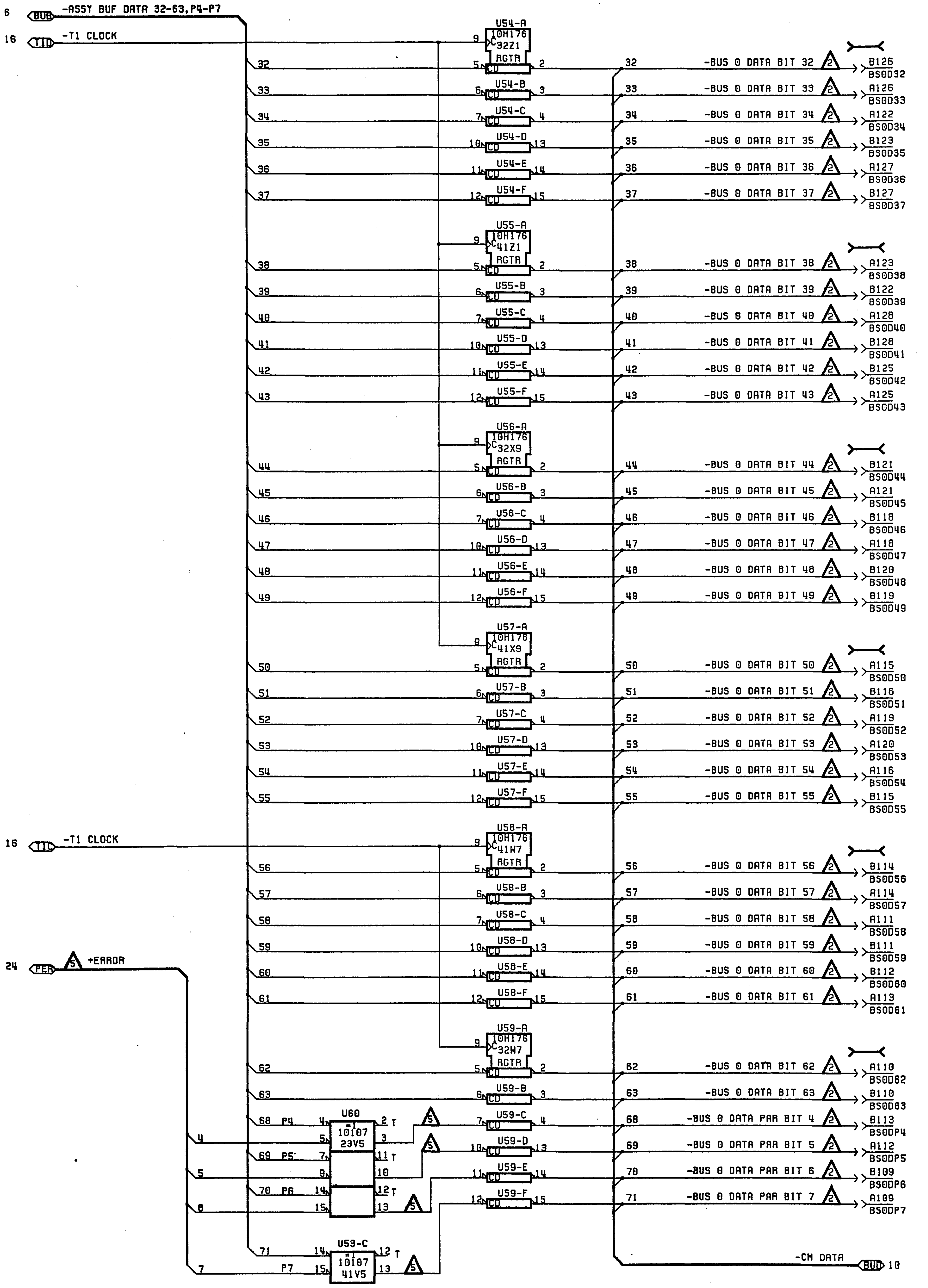
5 BUF -ASSY BUF DATA 0-31,P0-P3
16 TIB -T1 CLOCK
16 TIC -T1 CLOCK
24 PER 5 +ERROR
U46-A 10H176 32A9 AGTR
U46-B
U46-C
U46-D
U46-E
U46-F
U47-A 10H176 41A9 AGTR
U47-B
U47-C
U47-D
U47-E
U47-F
U48-A 10H176 32T1 AGTR
U48-B
U48-C
U48-D
U48-E
U48-F
U49-A 10H176 41T1 AGTR
U49-B
U49-C
U49-D
U49-E
U49-F
U50-A 10H176 41U3 AGTR
U50-B
U50-C
U50-D
U50-E
U50-F
U51-A 10H176 32U3 AGTR
U51-B
U51-C
U51-D
U51-E
U51-F
U52 10107 32V5
U53-B 10107 41V5
C
CD
64 P0
65 P1
66 P2
67 P3
-BUS 0 DATA BIT 0 2 A092 BS0D00
-BUS 0 DATA BIT 1 2 B092 BS0D01
-BUS 0 DATA BIT 2 2 B089 BS0D02
-BUS 0 DATA BIT 3 2 A089 BS0D03
-BUS 0 DATA BIT 4 2 A093 BS0D04
-BUS 0 DATA BIT 5 2 B093 BS0D05
-BUS 0 DATA BIT 6 2 B090 BS0D06
-BUS 0 DATA BIT 7 2 A090 BS0D07
-BUS 0 DATA BIT 8 2 A094 BS0D08
-BUS 0 DATA BIT 9 2 B094 BS0D09
-BUS 0 DATA BIT 10 2 B091 BS0D10
-BUS 0 DATA BIT 11 2 A091 BS0D11
-BUS 0 DATA BIT 12 2 A101 BS0D12
-BUS 0 DATA BIT 13 2 B101 BS0D13
-BUS 0 DATA BIT 14 2 B098 BS0D14
-BUS 0 DATA BIT 15 2 A098 BS0D15
-BUS 0 DATA BIT 16 2 A099 BS0D16
-BUS 0 DATA BIT 17 2 B099 BS0D17
-BUS 0 DATA BIT 18 2 B095 BS0D18
-BUS 0 DATA BIT 19 2 A095 BS0D19
-BUS 0 DATA BIT 20 2 A100 BS0D20
-BUS 0 DATA BIT 21 2 B100 BS0D21
-BUS 0 DATA BIT 22 2 B096 BS0D22
-BUS 0 DATA BIT 23 2 A096 BS0D23
-BUS 0 DATA BIT 24 2 A106 BS0D24
-BUS 0 DATA BIT 25 2 B106 BS0D25
-BUS 0 DATA BIT 26 2 B103 BS0D26
-BUS 0 DATA BIT 27 2 A103 BS0D27
-BUS 0 DATA BIT 28 2 A105 BS0D28
-BUS 0 DATA BIT 29 2 B105 BS0D29
-BUS 0 DATA BIT 30 2 B102 BS0D30
-BUS 0 DATA BIT 31 2 A102 BS0D31
-BUS 0 DATA PAR BIT 0 2 A104 BS0DP0
-BUS 0 DATA PAR BIT 1 2 B104 BS0DP1
-BUS 0 DATA PAR BIT 2 2 B108 BS0DP2
-BUS 0 DATA PAR BIT 3 2 A108 BS0DP3
-CM DATA BUD 9

2 4" MAXIMUM LENGTH & NOT TERMINATED

5 3" MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER OUTPUT REGISTER BITS 0-31,P0-P3 TYPE JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 7	60462210	PAGE JY-07	

ASSEMBLY BUFFER OUTPUT
REGISTER BITS 32-63, PAR 4-7 (3.1)

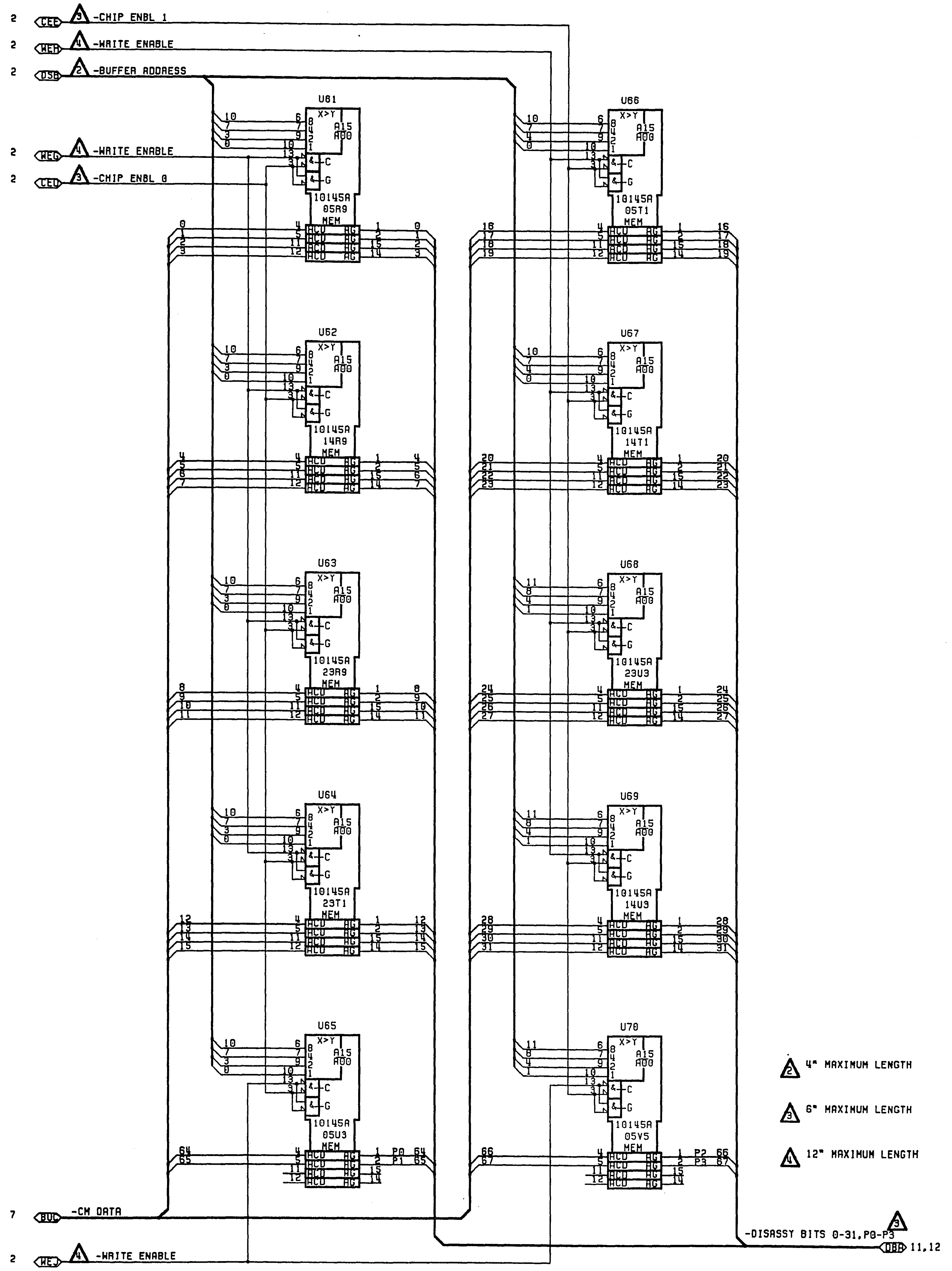

6 BUB -ASSY BUF DATA 32-63,P4-P7
16 T1D -T1 CLOCK
U54-A 10H176 32Z1 AGTR C CD 9 5 2
U54-B 6 3
U54-C 7 4
U54-D 10 13
U54-E 11 14
U54-F 12 15
32 -BUS 0 DATA BIT 32 2 B126 BS0D32
33 -BUS 0 DATA BIT 33 2 A126 BS0D33
34 -BUS 0 DATA BIT 34 2 A122 BS0D34
35 -BUS 0 DATA BIT 35 2 B123 BS0D35
36 -BUS 0 DATA BIT 36 2 A127 BS0D36
37 -BUS 0 DATA BIT 37 2 B127 BS0D37
U55-A 10H176 41Z1 AGTR
U55-B
U55-C
U55-D
U55-E
U55-F
38 -BUS 0 DATA BIT 38 2 A123 BS0D38
39 -BUS 0 DATA BIT 39 2 B122 BS0D39
40 -BUS 0 DATA BIT 40 2 A128 BS0D40
41 -BUS 0 DATA BIT 41 2 B128 BS0D41
42 -BUS 0 DATA BIT 42 2 B125 BS0D42
43 -BUS 0 DATA BIT 43 2 A125 BS0D43
U56-A 10H176 32X9 AGTR
U56-B
U56-C
U56-D
U56-E
U56-F
44 -BUS 0 DATA BIT 44 2 B121 BS0D44
45 -BUS 0 DATA BIT 45 2 A121 BS0D45
46 -BUS 0 DATA BIT 46 2 B118 BS0D46
47 -BUS 0 DATA BIT 47 2 A118 BS0D47
48 -BUS 0 DATA BIT 48 2 B120 BS0D48
49 -BUS 0 DATA BIT 49 2 B119 BS0D49
U57-A 10H176 41X9 AGTR
U57-B
U57-C
U57-D
U57-E
U57-F
50 -BUS 0 DATA BIT 50 2 A115 BS0D50
51 -BUS 0 DATA BIT 51 2 B116 BS0D51
52 -BUS 0 DATA BIT 52 2 A119 BS0D52
53 -BUS 0 DATA BIT 53 2 A120 BS0D53
54 -BUS 0 DATA BIT 54 2 A116 BS0D54
55 -BUS 0 DATA BIT 55 2 B115 BS0D55
16 T1C -T1 CLOCK
U58-A 10H176 41W7 AGTR
U58-B
U58-C
U58-D
U58-E
U58-F
56 -BUS 0 DATA BIT 56 2 B114 BS0D56
57 -BUS 0 DATA BIT 57 2 A114 BS0D57
58 -BUS 0 DATA BIT 58 2 A111 BS0D58
59 -BUS 0 DATA BIT 59 2 B111 BS0D59
60 -BUS 0 DATA BIT 60 2 B112 BS0D60
61 -BUS 0 DATA BIT 61 2 A113 BS0D61
24 PER 5 +ERROR
U59-A 10H176 32W7 AGTR
U59-B
U59-C
U59-D
U59-E
U59-F
62 -BUS 0 DATA BIT 62 2 A110 BS0D62
63 -BUS 0 DATA BIT 63 2 B110 BS0D63
68 -BUS 0 DATA PAR BIT 4 2 B113 BS0DP4
69 -BUS 0 DATA PAR BIT 5 2 A112 BS0DP5
70 -BUS 0 DATA PAR BIT 6 2 B109 BS0DP6
71 -BUS 0 DATA PAR BIT 7 2 A109 BS0DP7
68 P4
69 P5
70 P6
U60 =1 10107 23V5 T 5
U53-C =1 10107 41V5 T 5
71 P7
4 5 6 7
-CM DATA BUD 10

2 4" MAXIMUM LENGTH & NOT TERMINATED

5 3" MAXIMUM LENGTH

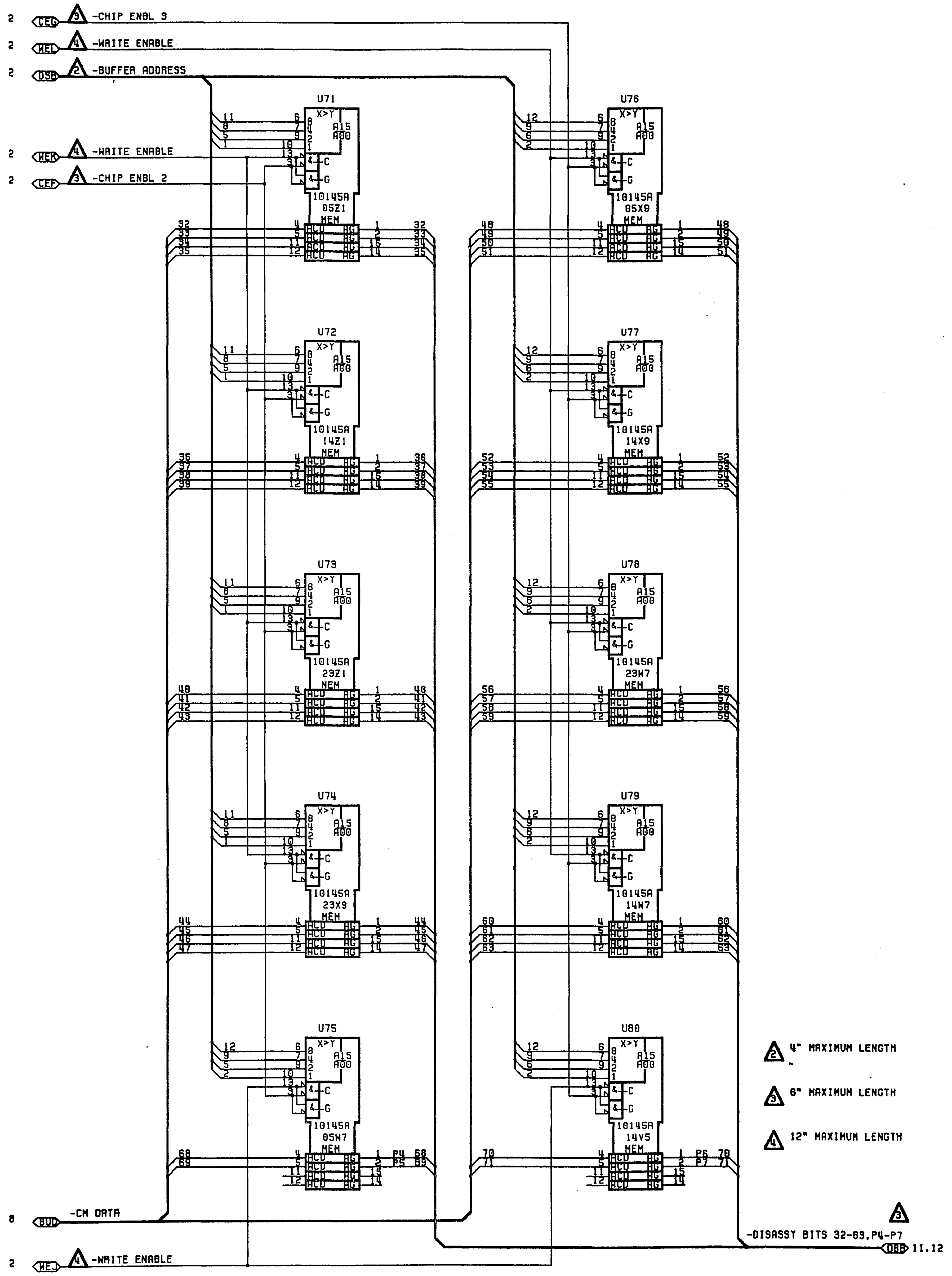
CONTROL DATA	CIO CHANNEL BOARD ASSEMBLY BUFFER OUTPUT REGISTER BITS 32-63, P4-P7 TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 8	60462210	PAGE JY-08	

DISASSEMBLY BUFFER BITS 0-31,PAR 0-3 (3.1)



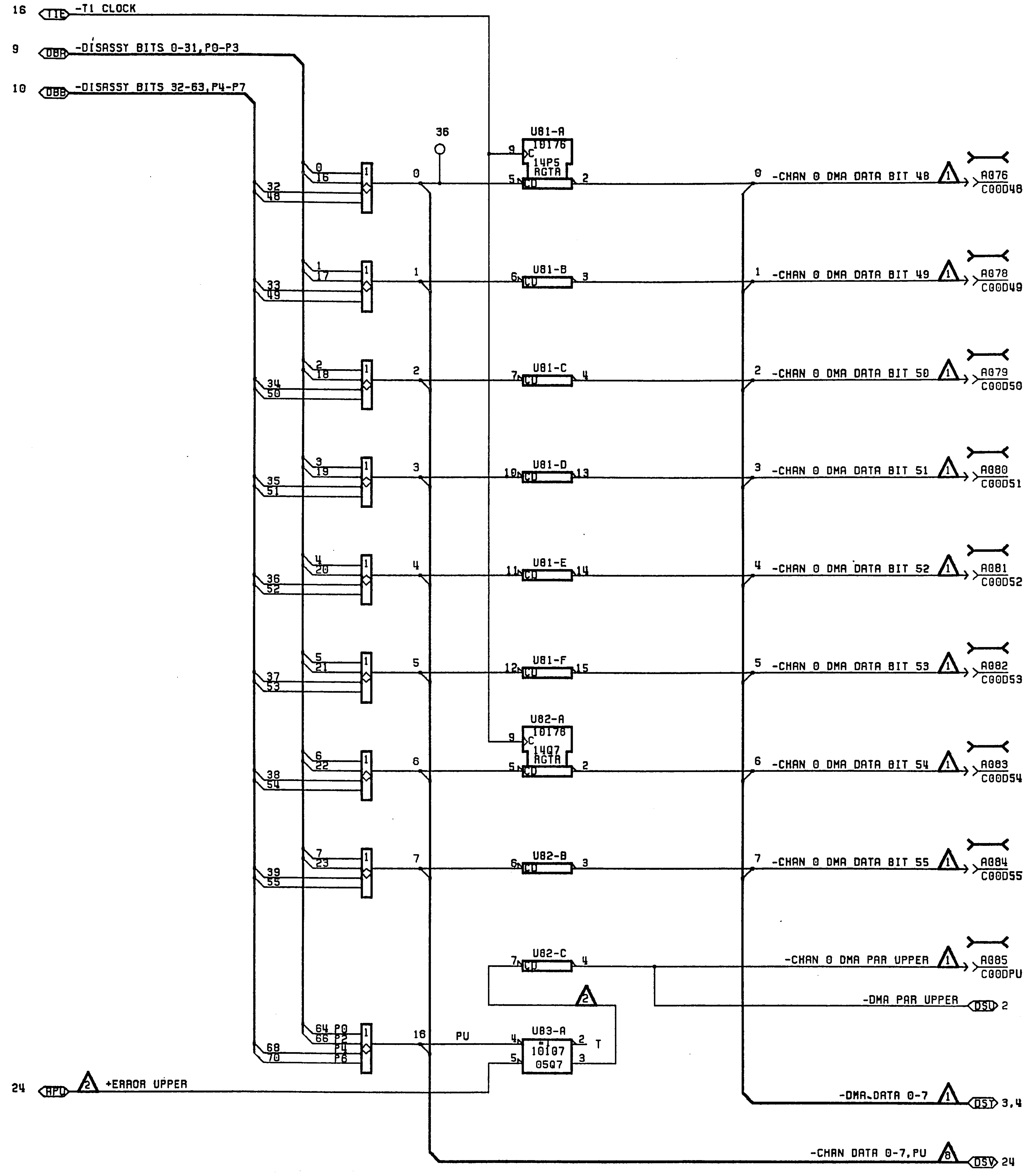
CONTROL DATA	CIO CHANNEL BOARD DISASSEMBLY BITS 0-31,P0-P3 TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 9	60462210	PAGE JT-09	

DISASSEMBLY BUFFER BITS 32-63,PAR 4-7 (3.1)



CONTROL DATA	CIO CHANNEL BOARD DISASSEMBLY BITS 32-63,P4-P7 TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
			SHEET NO. 10	60462210	PAGE JY-10

DISASSEMBLY BUFFER OUTPUT REGISTER BITS 0-7,PAR UPR (3.1)


16 -T1 CLOCK
9 -DISASSY BITS 0-31,P0-P3
10 -DISASSY BITS 32-63,P4-P7
36
U01-A 10176 14P5 RGTR
U01-B
U01-C
U01-D
U01-E
U01-F
U02-A 10176 14Q7 RGTR
U02-B
U02-C
U03-A 10107 05Q7
0 -CHAN 0 DMA DATA BIT 48 A076 C00D48
1 -CHAN 0 DMA DATA BIT 49 A078 C00D49
2 -CHAN 0 DMA DATA BIT 50 A079 C00D50
3 -CHAN 0 DMA DATA BIT 51 A080 C00D51
4 -CHAN 0 DMA DATA BIT 52 A081 C00D52
5 -CHAN 0 DMA DATA BIT 53 A082 C00D53
6 -CHAN 0 DMA DATA BIT 54 A083 C00D54
7 -CHAN 0 DMA DATA BIT 55 A084 C00D55
-CHAN 0 DMA PAR UPPER A085 C00DPU
-DMA PAR UPPER DSU 2
-DMA DATA 0-7 DSI 3,4
-CHAN DATA 0-7,PU DSV 24
24 APU +ERROR UPPER
PU
T

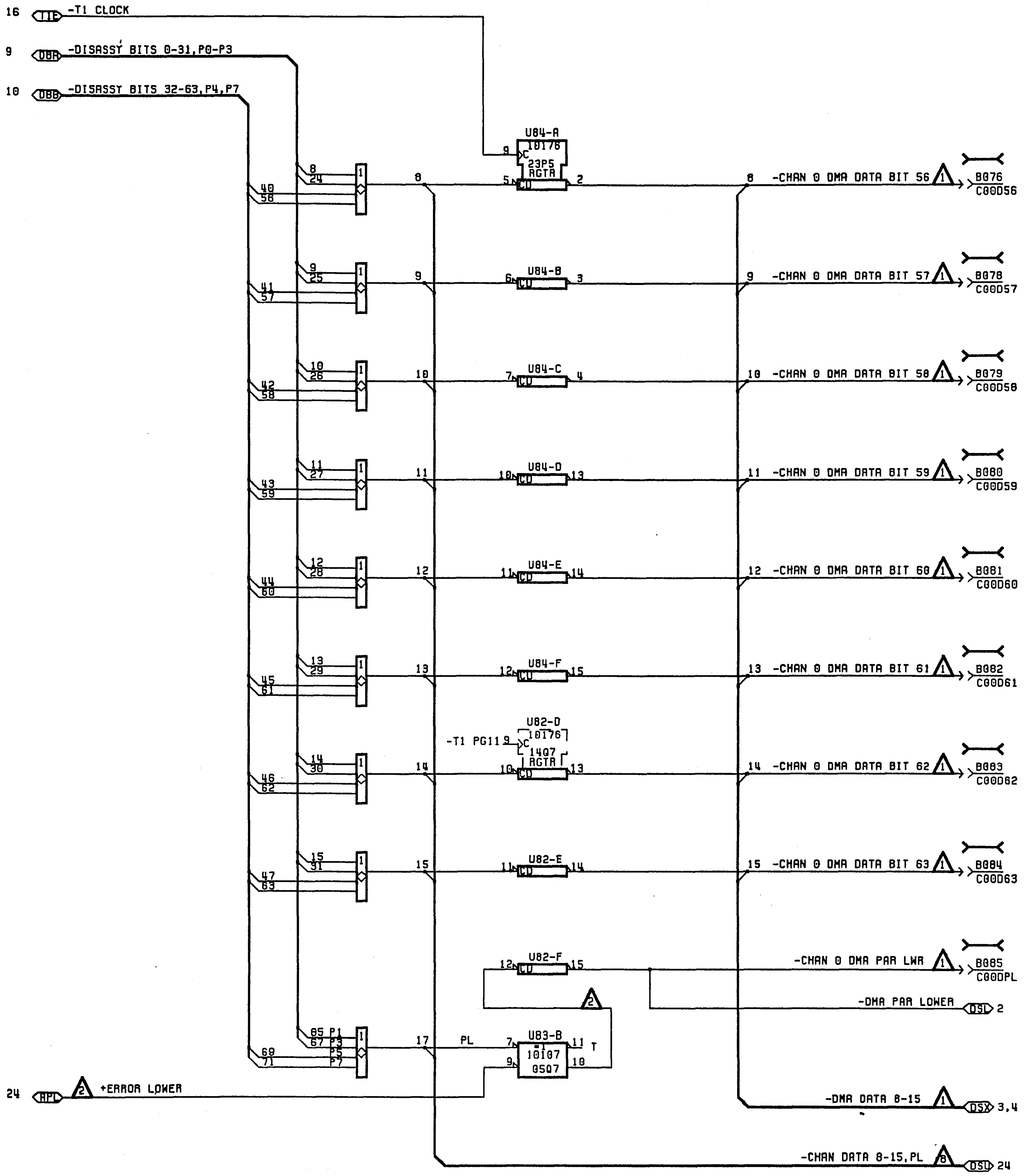
△1 TERMINATE AT OUTPUT OF 10176 CHIP

△2 4" MAXIMUM LENGTH

△8 TERMINATE AT 10176/10107 CHIPS

CONTROL DATA	CIO CHANNEL BOARD DISASSEMBLY BUFFER OUTPUT REGISTER BITS 0-7,PU TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
	N	SHEET NO. 11	60462210	PAGE JY-11	

DISASSEMBLY BUFFER OUTPUT REGISTER BITS 8-15,PAR LWR
(3.1)



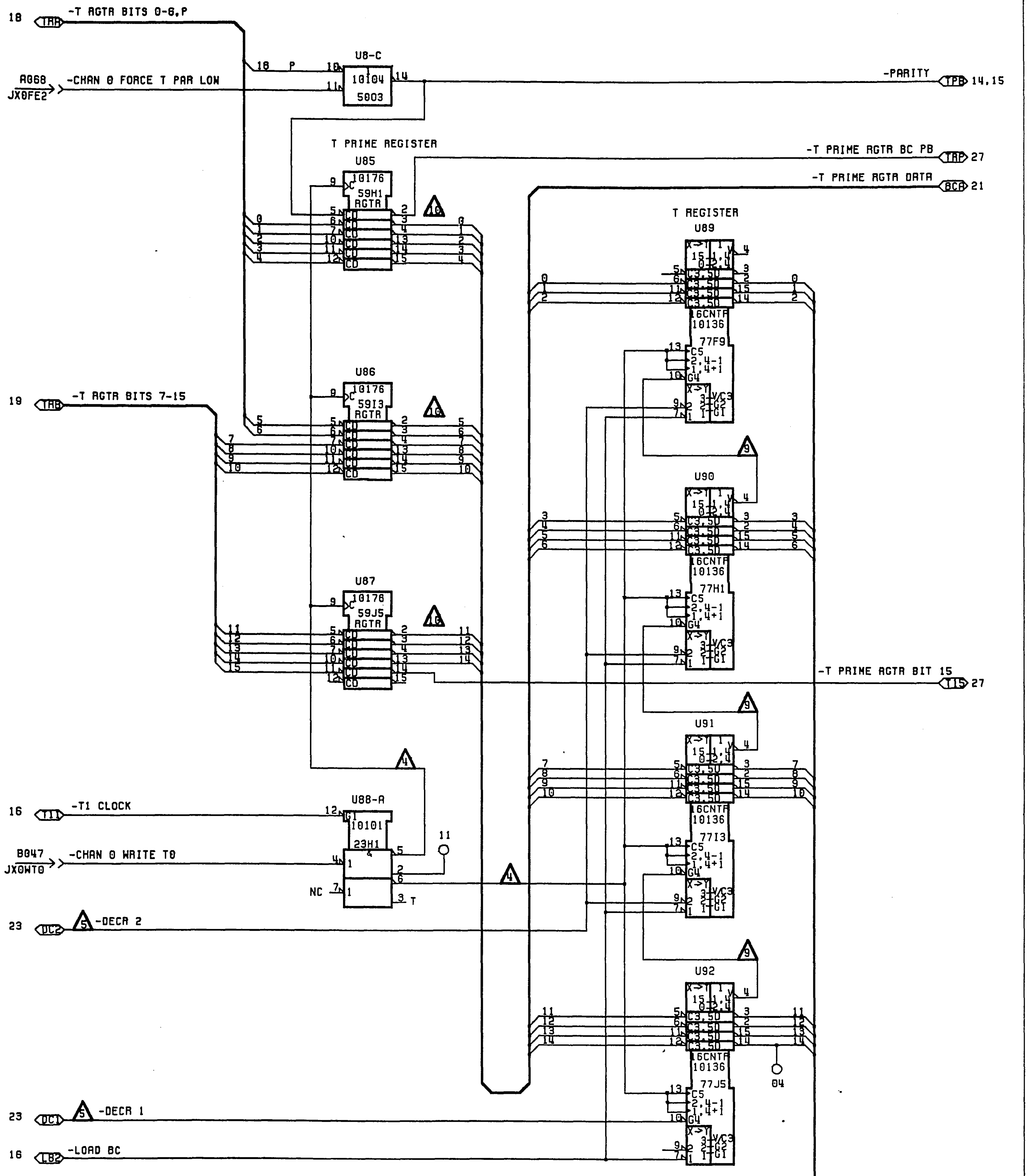
1 TERMINATE AT OUTPUT OF 10176 CHIP

2 4" MAXIMUM LENGTH

8 TERMINATE AT 10176/10107 CHIPS

CONTROL DATA	CIO CHANNEL BOARD DISASSEMBLY BUFFER OUTPUT REGISTER BITS 8-15,PL TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		N SHEET NO. 12	60462210	PAGE JY-12	

T REGISTER BITS 0-15, PAR
BYTE COUNT 0-15 (3.2)



4 12 INCH MAXIMUM LENGTH

5 3 INCH MAXIMUM LENGTH

9 2 INCH MAXIMUM LENGTH

10 9 INCH MINIMUM LENGTHS
(EXCLUDING PIN2 ON U85 $ PIN 14 ON U87)

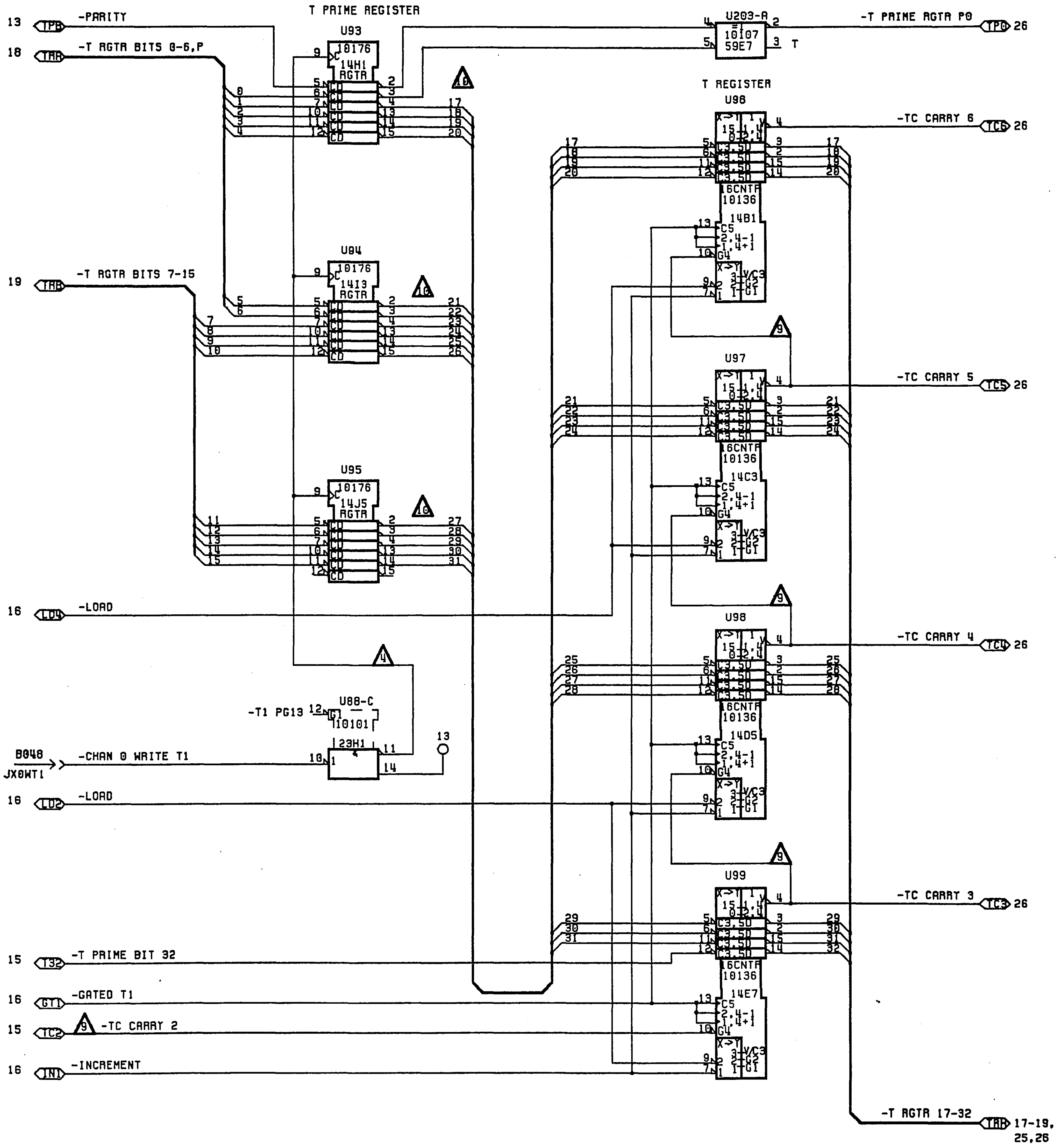
CONTROL DATA

CIO CHANNEL BOARD
T REGISTER BITS 0-15, PB
BYTE COUNT 0-15
TYPE 1JYH

B	DWG NO.	DATE	REV
	22105622	03/14/86	A
SHEET NO.	13	60462210	PAGE JY-13

T REGISTER BITS 17-32, PAR 0

RMA 36-51 (3.2)



4 — 12 INCH MAXIMUM LENGTH

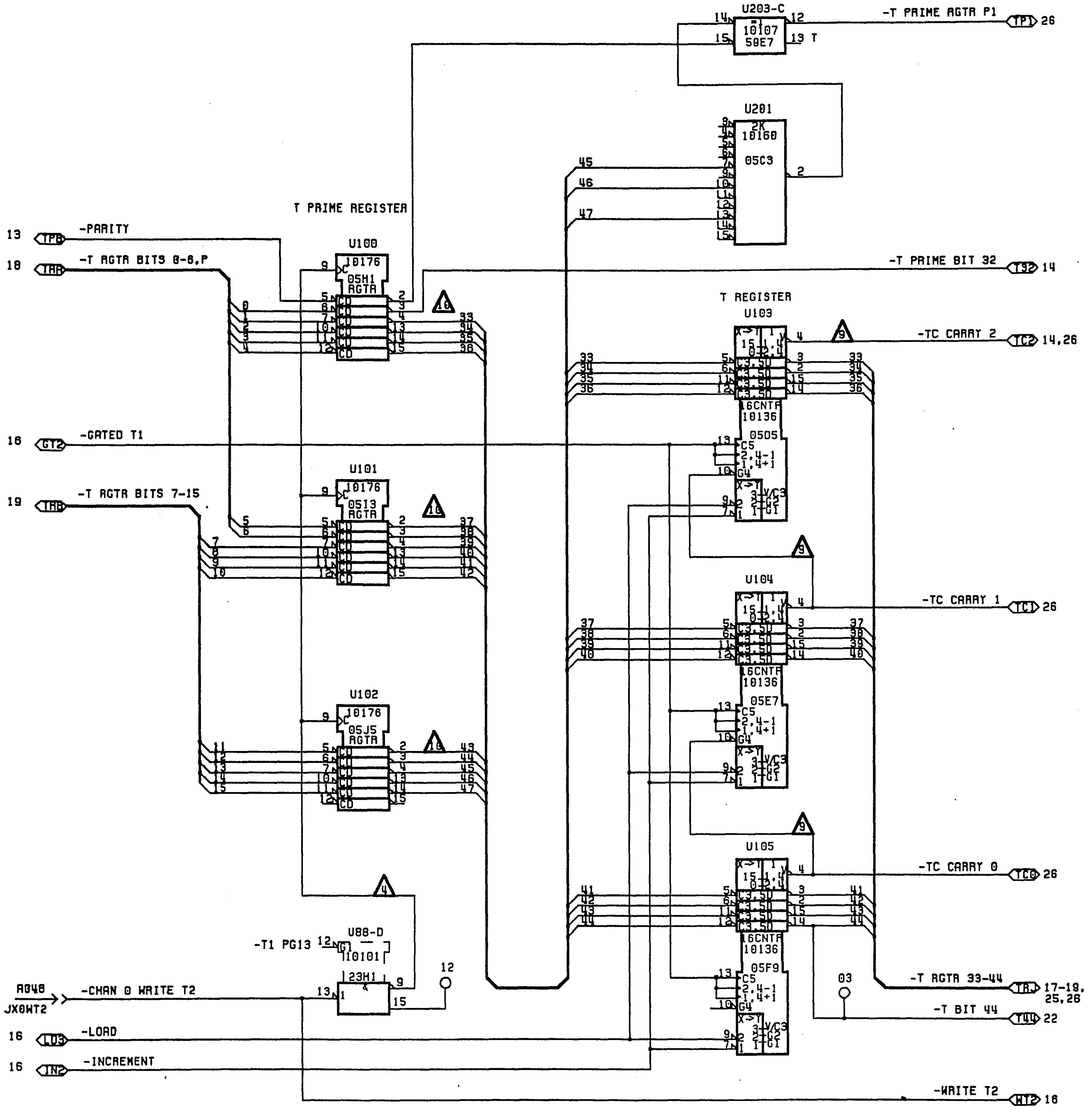
9 — 2 INCH MAXIMUM LENGTH

10 — 9 INCH MINUMUM LENGTHS (EXCLUDING PINS 2 & 3 ON U93)

CONTROL DATA	CIO CHANNEL BOARD T REGISTER BITS 17-32, P0 RMA 36-51 TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
			SHEET NO. 14	60462210	PAGE JY-14

T REGISTER BITS 33-44, PAR 1

RMA 52-63 (3.2)



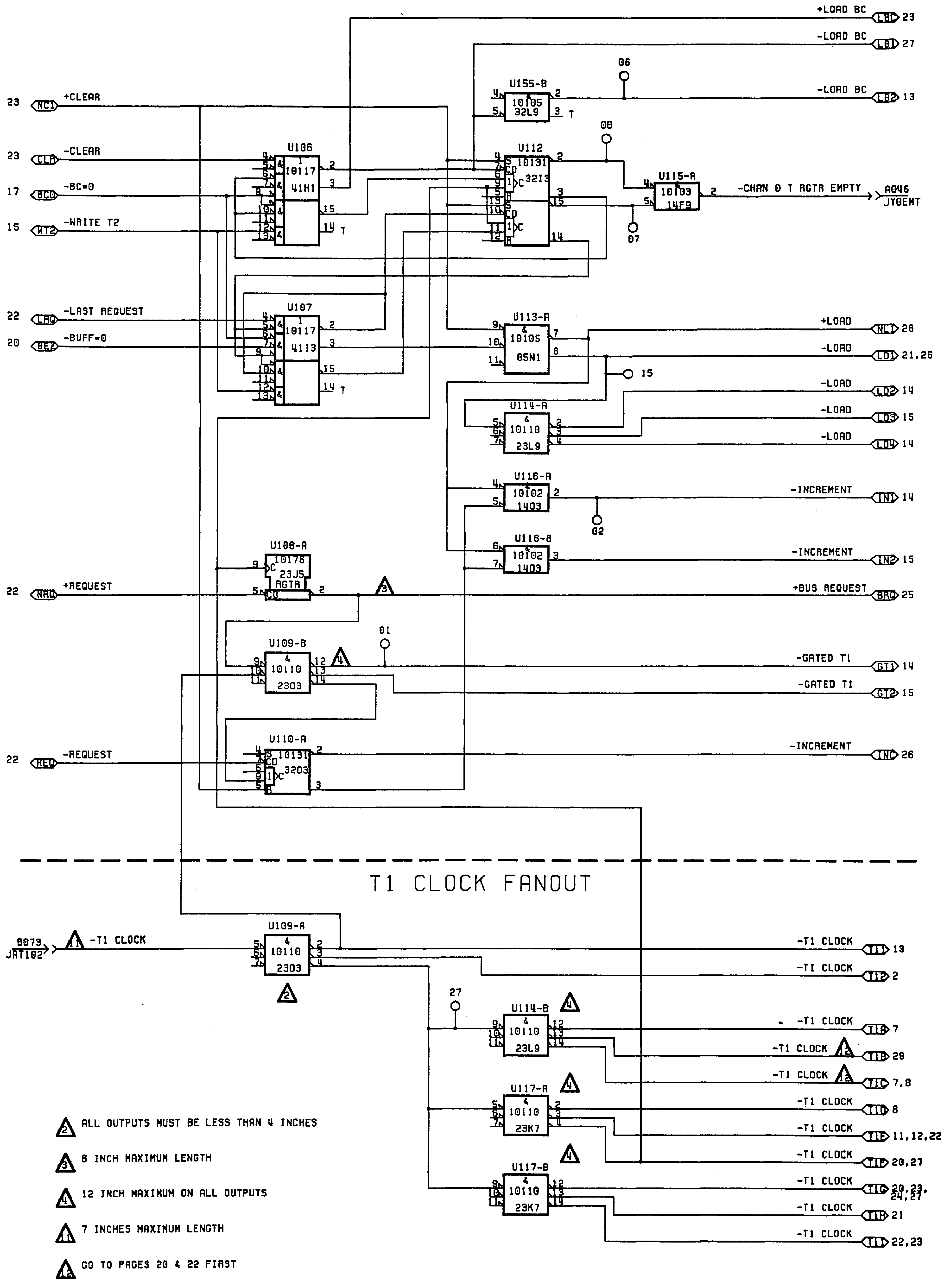
4 12 INCH MAXIMUM LENGTH

5 2 INCH MAXIMUM LENGTH

10 9 INCH MINIMUM LENGTHS (EXCLUDING PINS 2 & 3 OF U100 AND PINS 4, 13, & 14 OF U102)

CONTROL DATA	CIO CHANNEL BOARD T REGISTER BITS 33-44, P1 RMA 52-63 TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 15	60462210	PAGE JY-15	

T REGISTER CONTROL (3.2)



T1 CLOCK FANOUT

△2 ALL OUTPUTS MUST BE LESS THAN 4 INCHES

△3 8 INCH MAXIMUM LENGTH

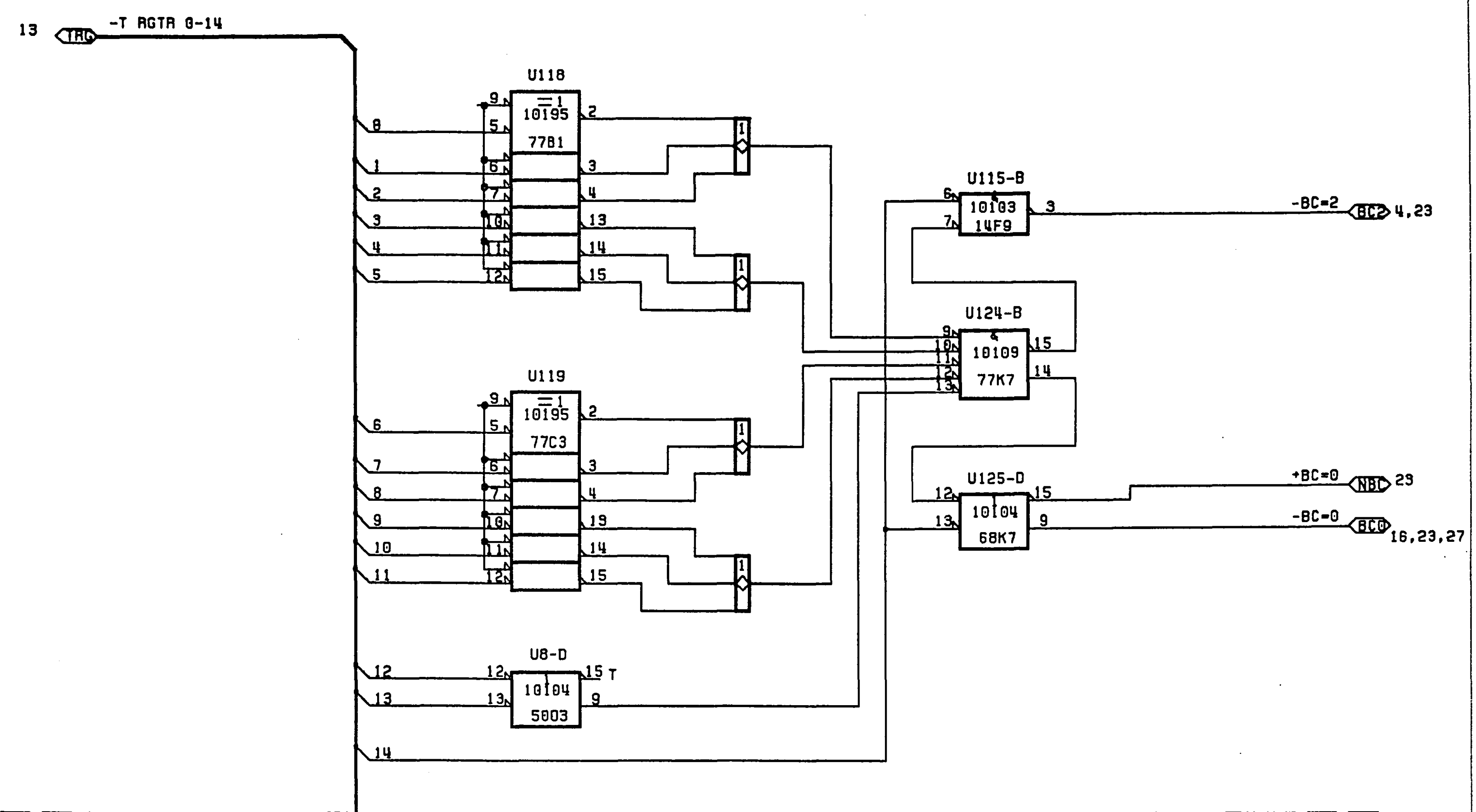
△4 12 INCH MAXIMUM ON ALL OUTPUTS

△11 7 INCHES MAXIMUM LENGTH

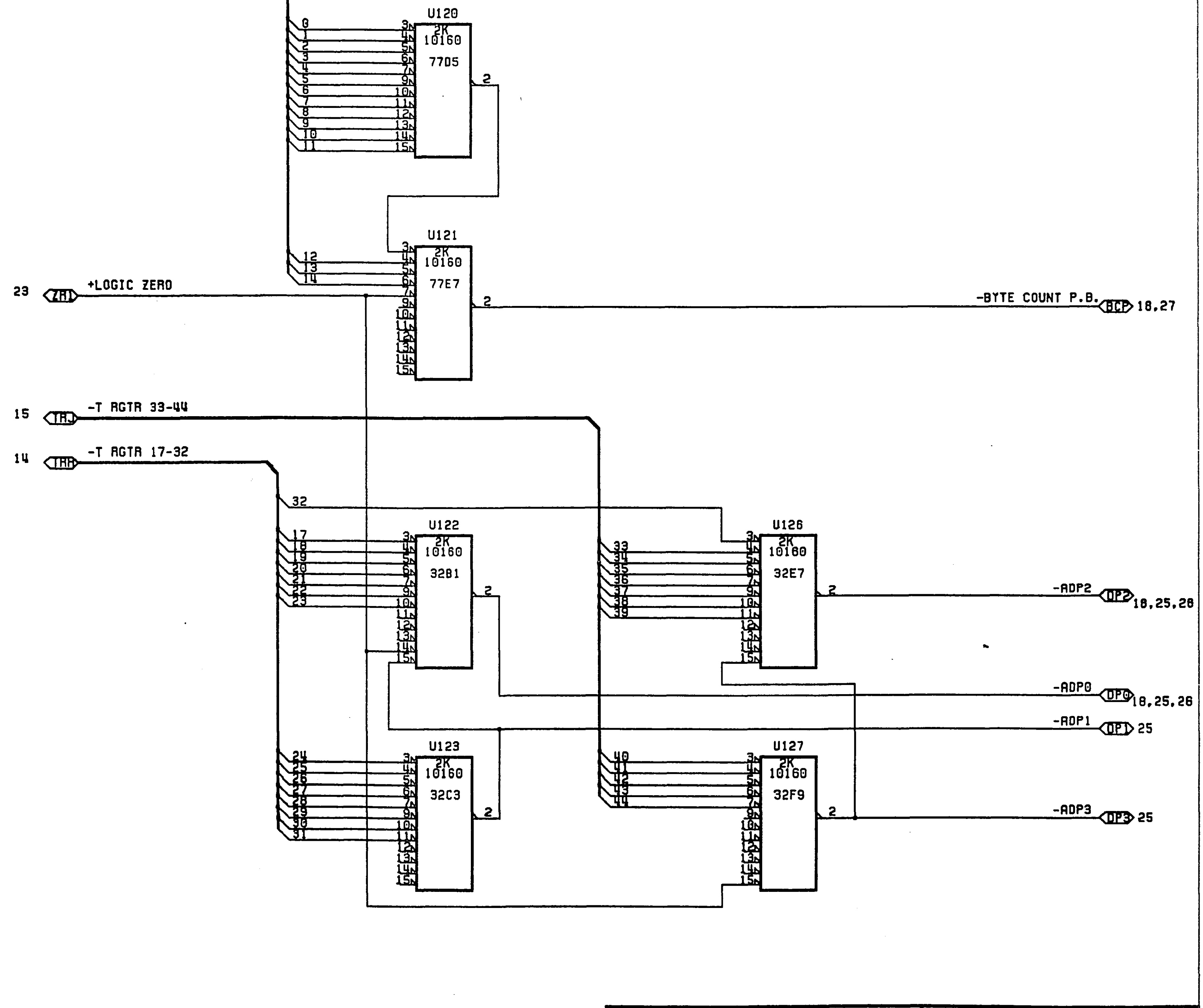
△12 GO TO PAGES 20 & 22 FIRST

CONTROL DATA	CIO CHANNEL BOARD T REGISTER CONTROL T1 CLOCK FANOUT TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 16	60462210	PAGE JT-16	

BYTE COUNT = 2 OR 0 TEST (3.3)



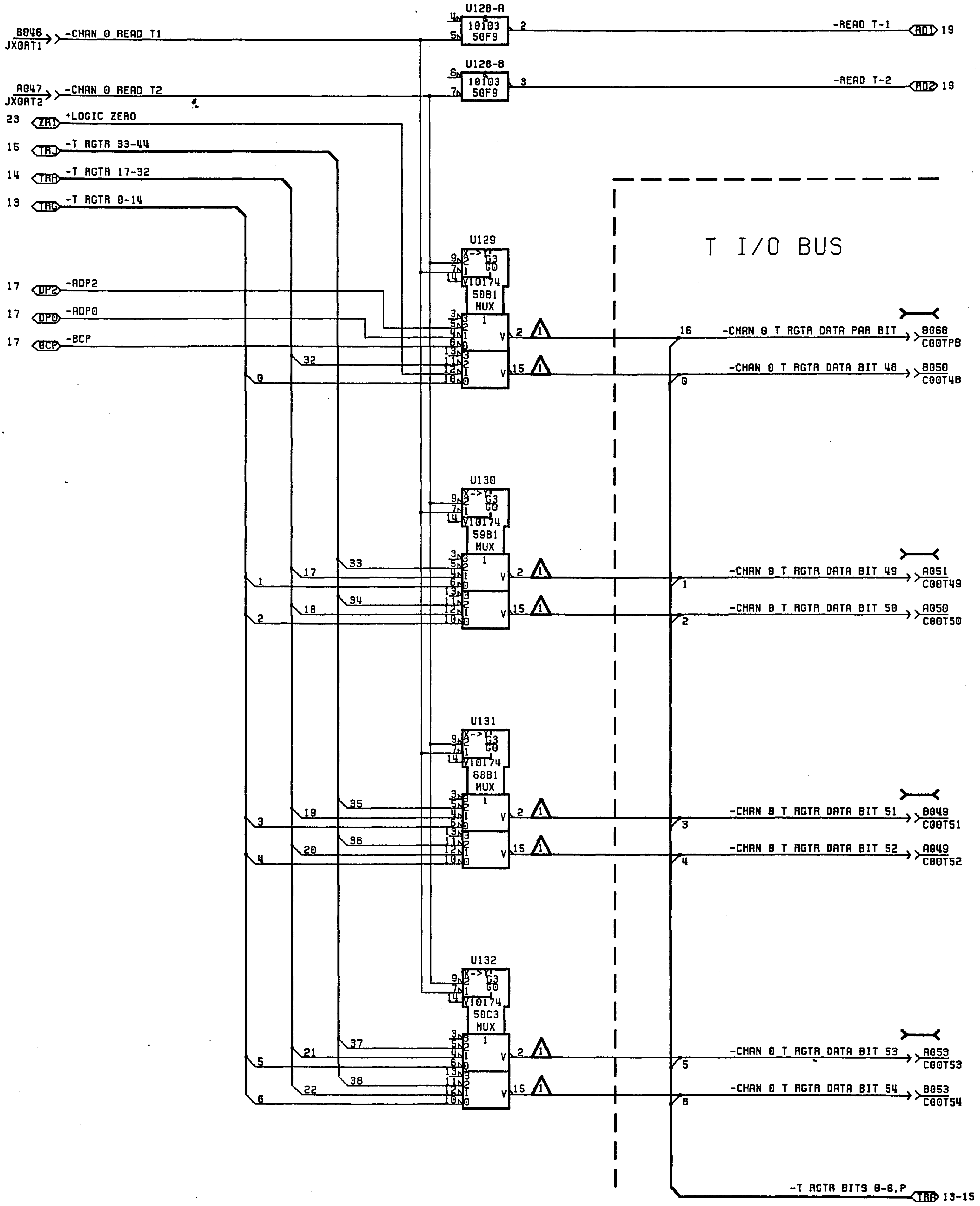
T REGISTER PARITY GENERATOR (3.3)



CONTROL DATA
CIO CHANNEL BOARD
BYTE COUNT = 2 OR 0 TEST
T REGISTER PARITY GENERATOR
TYPE 1JYH

	DWG NO.	DATE	REV
B	22185622	03/14/86	A
SHEET NO. 17	60462210	PAGE JY-17	

T REGISTER MUX BITS 0-6,PAR (3.2)


B046 JX0RT1 -CHAN 0 READ T1
A047 JX0RT2 -CHAN 0 READ T2
23 ZR1 +LOGIC ZERO
15 TRJ -T RGTR 33-44
14 TRR -T RGTR 17-32
13 TRG -T RGTR 0-14
17 DP2 -ADP2
17 DP0 -ADP0
17 BCP -BCP
U128-A 10103 50F9
U128-B 10103 50F9
-READ T-1 RD1 19
-READ T-2 RD2 19
U129 10174 50B1 MUX
U130 10174 59B1 MUX
U131 10174 68B1 MUX
U132 10174 50C3 MUX
T I/O BUS
-CHAN 0 T RGTR DATA PAR BIT B068 C00TPB
-CHAN 0 T RGTR DATA BIT 48 B050 C00T48
-CHAN 0 T RGTR DATA BIT 49 A051 C00T49
-CHAN 0 T RGTR DATA BIT 50 A050 C00T50
-CHAN 0 T RGTR DATA BIT 51 B049 C00T51
-CHAN 0 T RGTR DATA BIT 52 A049 C00T52
-CHAN 0 T RGTR DATA BIT 53 A053 C00T53
-CHAN 0 T RGTR DATA BIT 54 B053 C00T54
-T RGTR BITS 0-6,P TRB 13-15

⚠1 TERMINATE AT FARTHEST POINT FROM CONNECTOR PIN

CONTROL DATA

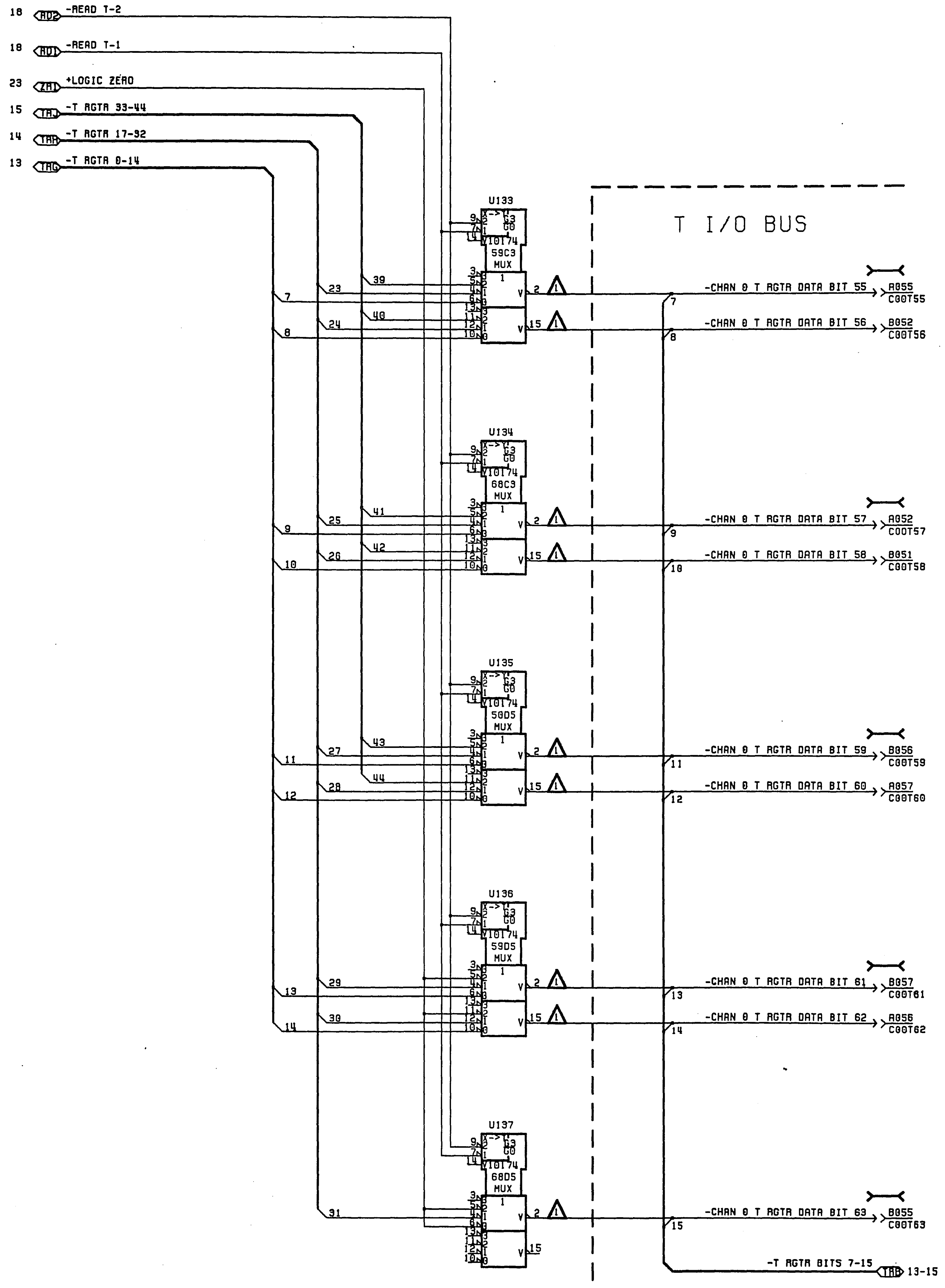
CIO CHANNEL BOARD

T REGISTER MUX BITS 0-6,PB
T I/O BUS
TYPE 1JYH

B | DWG NO. 22105622 | DATE 03/14/86 | REV A

SHEET NO. 18 | 60462210 | PAGE JY-18

T REGISTER MUX BITS 7-15 (3.2)

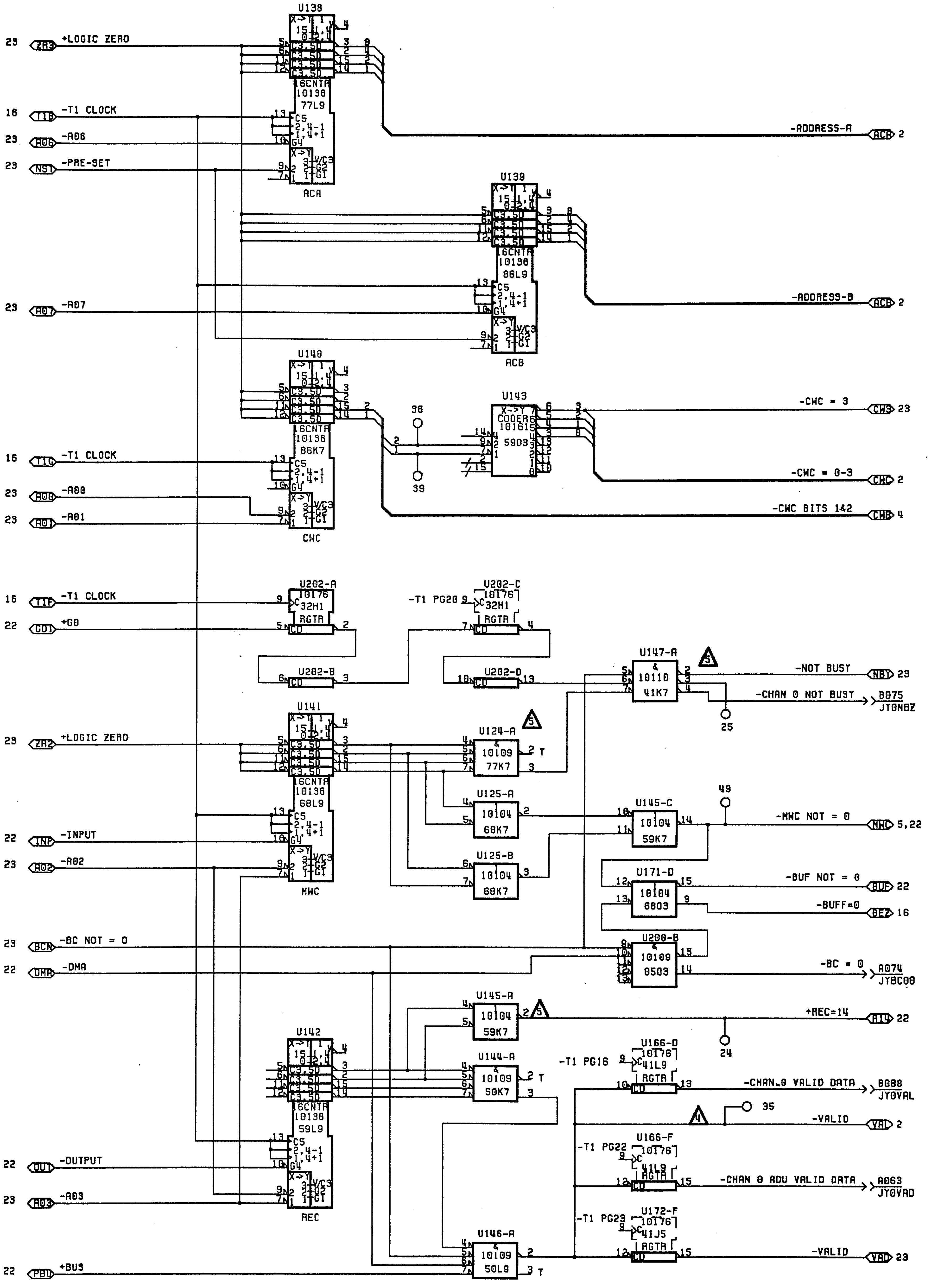


18 RD2 -READ T-2
18 RD1 -READ T-1
23 ZR1 +LOGIC ZERO
15 TAJ -T RGTR 33-44
14 TAH -T RGTR 17-32
13 TAG -T RGTR 0-14
T I/O BUS
U133 10174 59C3 MUX
U134 10174 68C3 MUX
U135 10174 58D5 MUX
U136 10174 59D5 MUX
U137 10174 68D5 MUX
-CHAN 0 T RGTR DATA BIT 55 A055 C00T55
-CHAN 0 T RGTR DATA BIT 56 B052 C00T56
-CHAN 0 T RGTR DATA BIT 57 A052 C00T57
-CHAN 0 T RGTR DATA BIT 58 B051 C00T58
-CHAN 0 T RGTR DATA BIT 59 B056 C00T59
-CHAN 0 T RGTR DATA BIT 60 A057 C00T60
-CHAN 0 T RGTR DATA BIT 61 B057 C00T61
-CHAN 0 T RGTR DATA BIT 62 A056 C00T62
-CHAN 0 T RGTR DATA BIT 63 B055 C00T63
-T RGTR BITS 7-15 TAB 13-15

⚠1 TERMINATE AT FARTHEST POINT FROM CONNECTOR PIN

CONTROL DATA	CIO CHANNEL BOARD T REGISTER MUX BITS 7-15 T I/O BUS TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 19	60462210	PAGE JY-19	

COUNTERS (3.4)

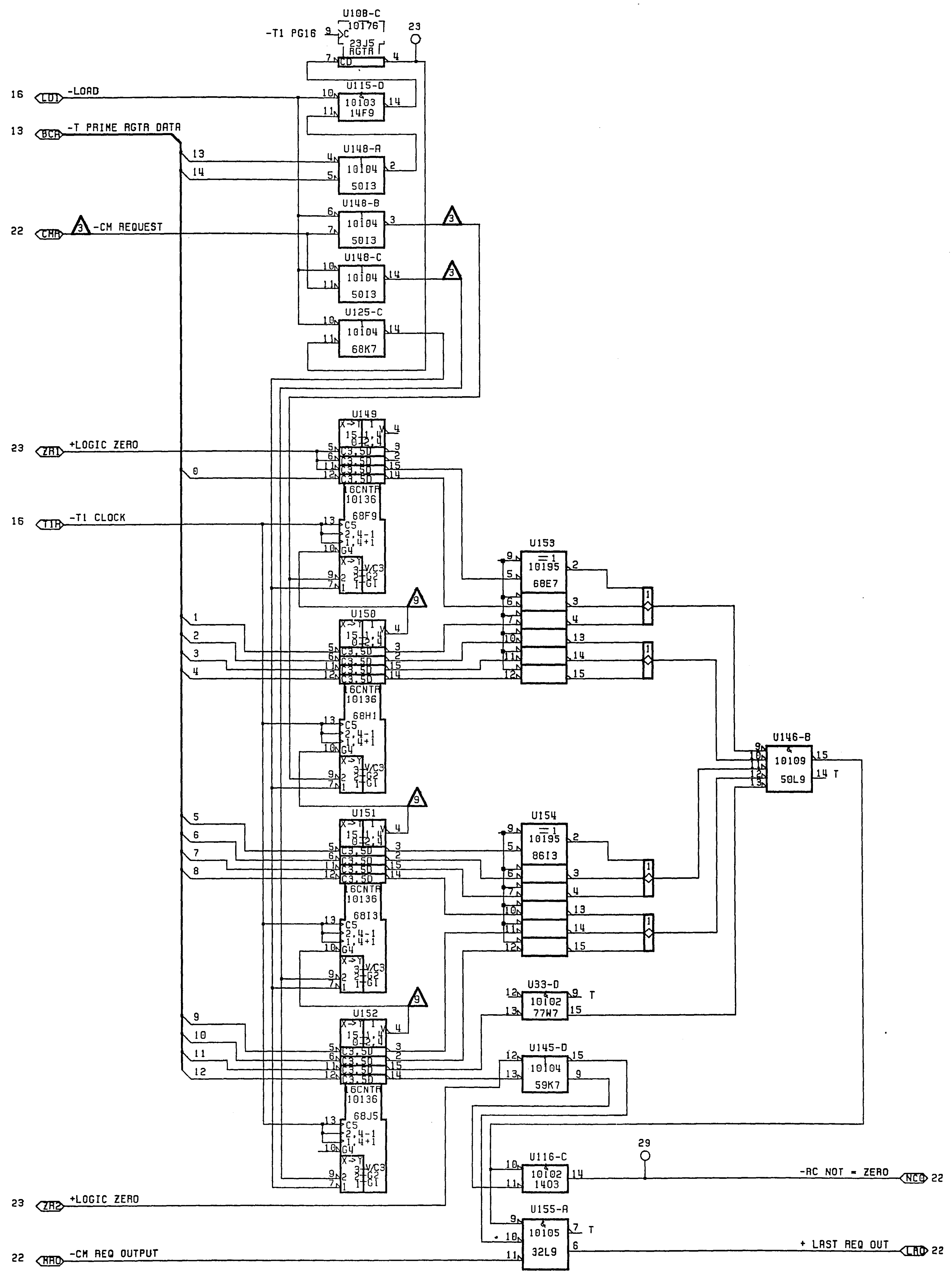


△4 12 INCH MAXIMUM

△5 3 INCH MAXIMUM LENGTH ON ALL INPUT/OUTPUT PINS UNLESS OTHERWISE INDICATED

CONTROL DATA	CIO CHANNEL BOARD COUNTERS TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		N	SHEET NO. 20	60462210	PAGE JY-20

REQUEST COUNTER (3.5)

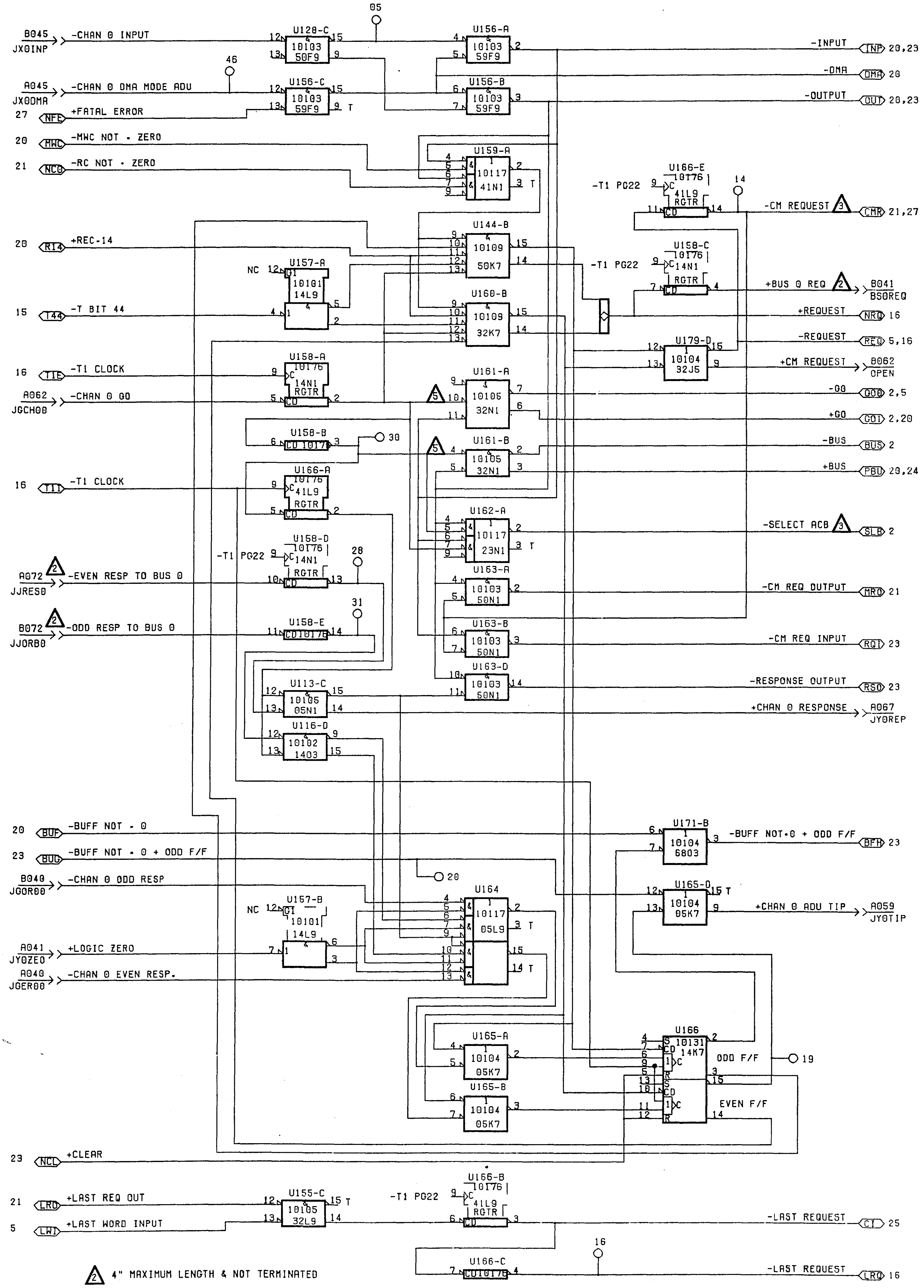


3 6 INCH MAXIMUM LENGTH

9 2 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD REQUEST COUNTER TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
			SHEET NO. 21	60462210	PAGE JY-21

CHANNEL GO/CM REQUEST/CM RESPONSE (3.5)



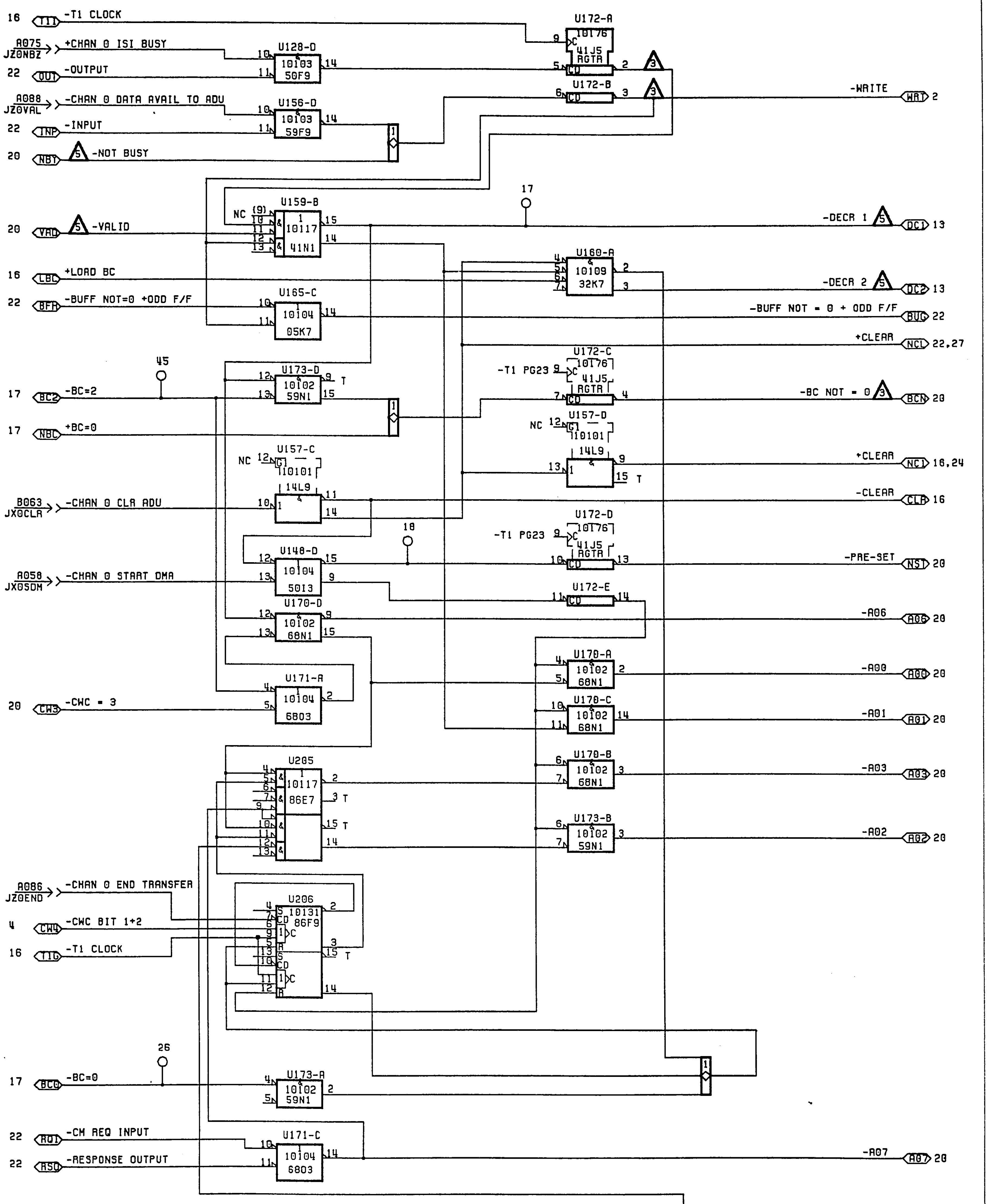
△2 4" MAXIMUM LENGTH & NOT TERMINATED

△3 6 INCH MAXIMUM LENGTH

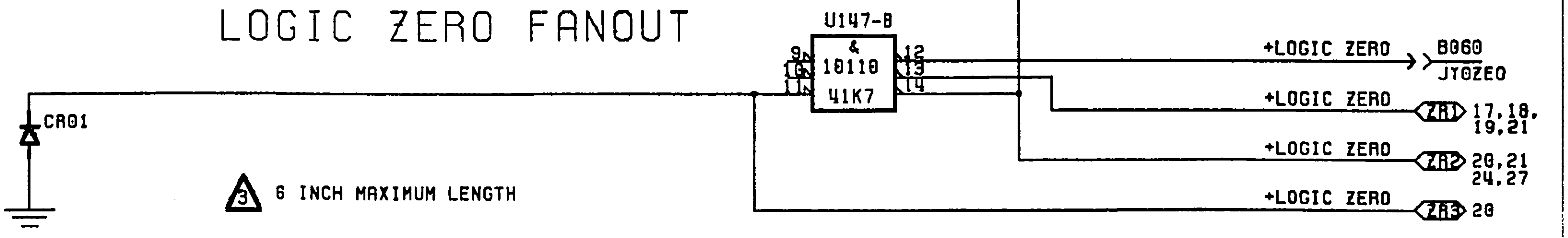
△5 3 INCH MAXIMUM LENGTH TO 10117 & 9 INCH MAX TOTAL LENGTH

CONTROL DATA	CIO CHANNEL BOARD CHANNEL GO / CM REQUEST / CM RESPONSE TYPE 1JYH	B	DWG NO. 22105622	DATE 06/14/88	REV B
		N	SHEET NO. 22	60462210	PAGE JY-22

COUNTER CONTROL (3.4)



LOGIC ZERO FANOUT

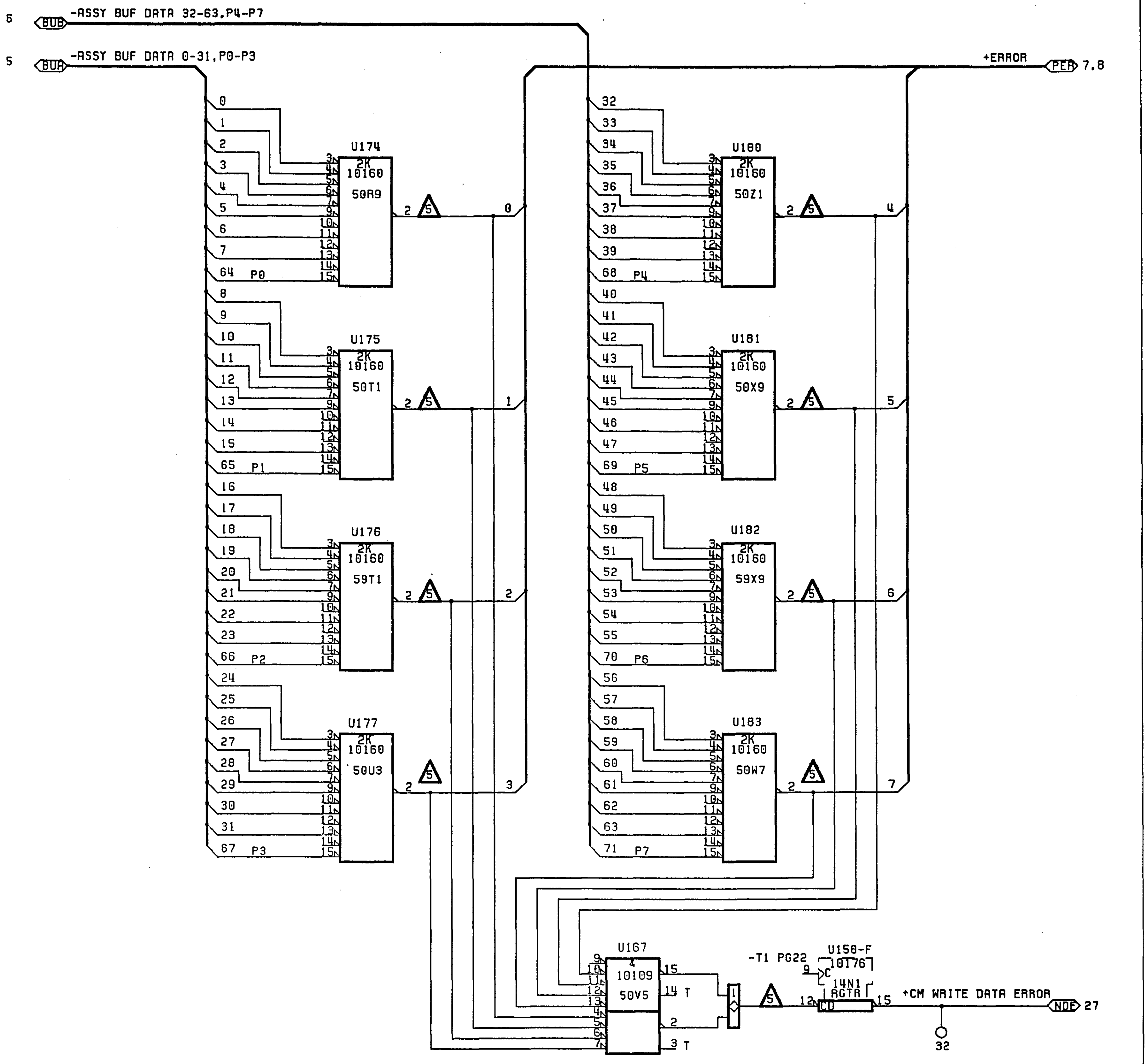


3 6 INCH MAXIMUM LENGTH

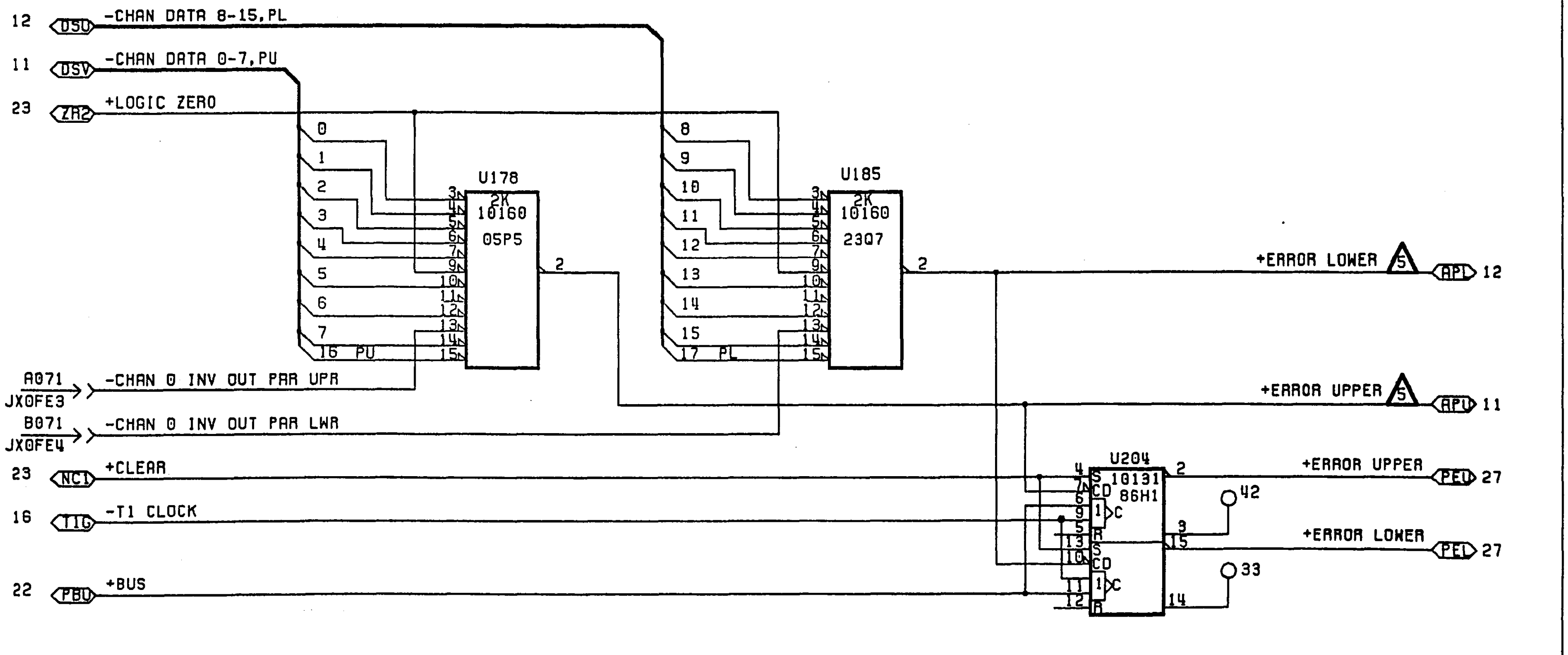
5 3 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD COUNTER CONTROL & LOGIC ZERO FANOUT TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 23	60462210	PAGE JT-23	

DATA PARITY CHECK (3.0)



DATA PARITY CHECK (3.1)



5 3 INCH MAXIMUM LENGTH

CONTROL DATA

CIO CHANNEL BOARD
DATA PARITY CHECK
TYPE 1JYH

B

DWG NO. 22105622

DATE 03/14/86

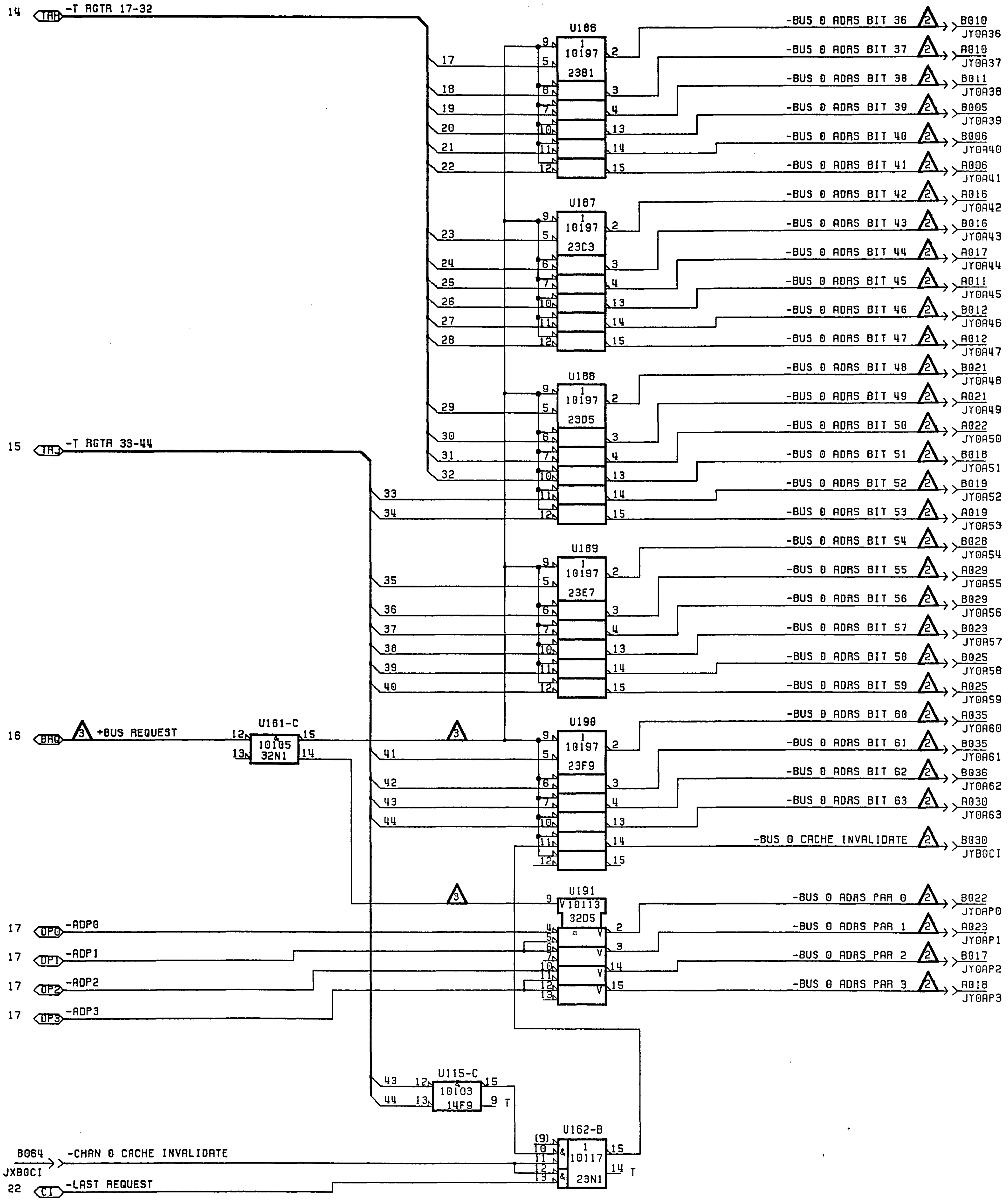
REV A

SHEET NO. 24

60462210

PAGE JY-24

CM ADDRESS TO CMI (3.3.)



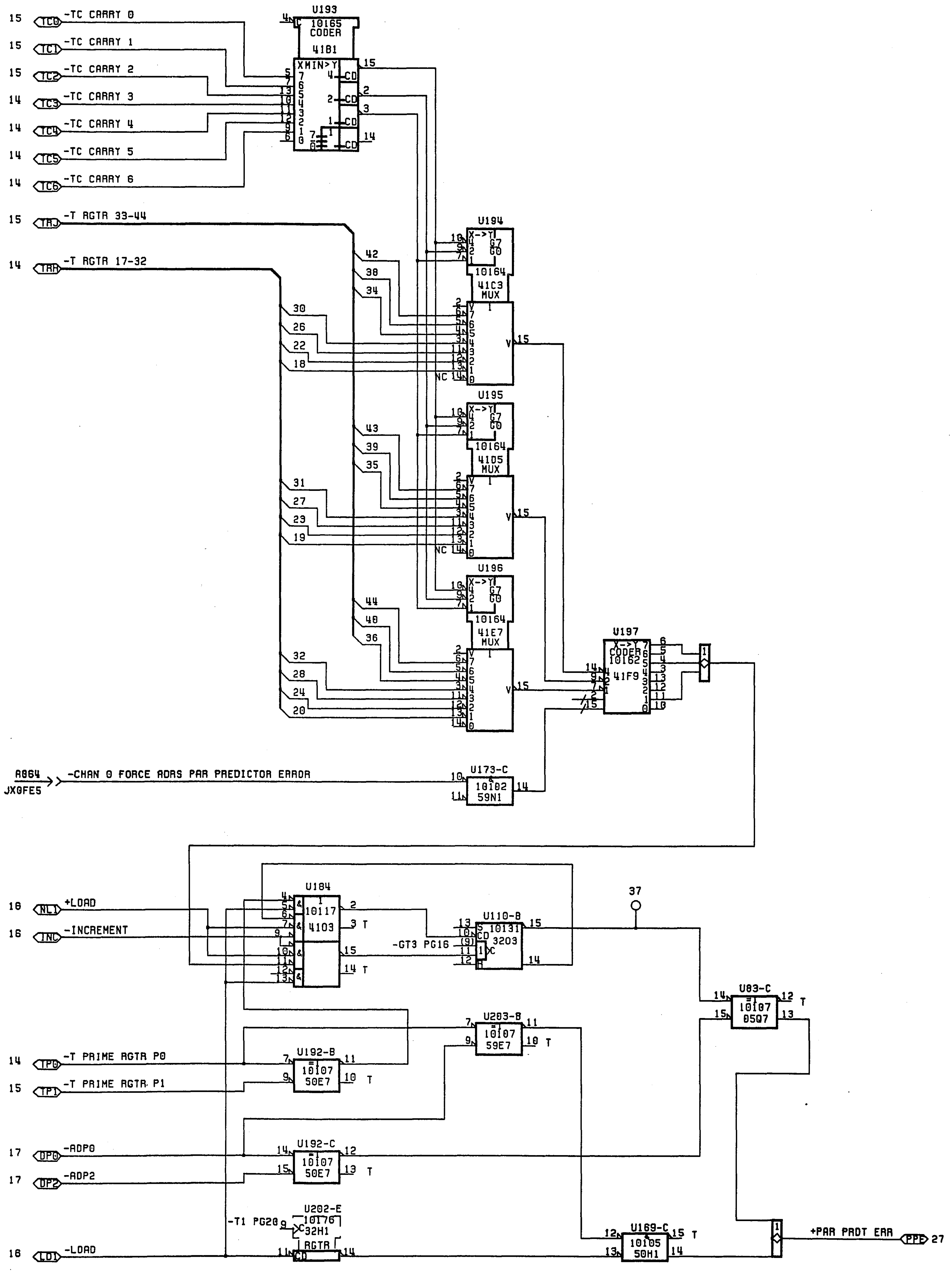
14 TAR -T RGTR 17-32
15 TAJ -T RGTR 33-44
16 BRQ 3 +BUS REQUEST
U161-C 10105 32N1
U186 10197 23B1
U187 10197 23C3
U188 10197 23D5
U189 10197 23E7
U190 10197 23F9
U191 10113 32D5
U115-C 10103 14F9
U162-B 10117 23N1
-BUS 0 ADRS BIT 36 2 B010 JY0A36
-BUS 0 ADRS BIT 37 2 A010 JY0A37
-BUS 0 ADRS BIT 38 2 B011 JY0A38
-BUS 0 ADRS BIT 39 2 B005 JY0A39
-BUS 0 ADRS BIT 40 2 B006 JY0A40
-BUS 0 ADRS BIT 41 2 A006 JY0A41
-BUS 0 ADRS BIT 42 2 A016 JY0A42
-BUS 0 ADRS BIT 43 2 B016 JY0A43
-BUS 0 ADRS BIT 44 2 A017 JY0A44
-BUS 0 ADRS BIT 45 2 A011 JY0A45
-BUS 0 ADRS BIT 46 2 B012 JY0A46
-BUS 0 ADRS BIT 47 2 A012 JY0A47
-BUS 0 ADRS BIT 48 2 B021 JY0A48
-BUS 0 ADRS BIT 49 2 A021 JY0A49
-BUS 0 ADRS BIT 50 2 A022 JY0A50
-BUS 0 ADRS BIT 51 2 B018 JY0A51
-BUS 0 ADRS BIT 52 2 B019 JY0A52
-BUS 0 ADRS BIT 53 2 A019 JY0A53
-BUS 0 ADRS BIT 54 2 B028 JY0A54
-BUS 0 ADRS BIT 55 2 A029 JY0A55
-BUS 0 ADRS BIT 56 2 B029 JY0A56
-BUS 0 ADRS BIT 57 2 B023 JY0A57
-BUS 0 ADRS BIT 58 2 B025 JY0A58
-BUS 0 ADRS BIT 59 2 A025 JY0A59
-BUS 0 ADRS BIT 60 2 A035 JY0A60
-BUS 0 ADRS BIT 61 2 B035 JY0A61
-BUS 0 ADRS BIT 62 2 B036 JY0A62
-BUS 0 ADRS BIT 63 2 A030 JY0A63
-BUS 0 CACHE INVALIDATE 2 B030 JYB0CI
-BUS 0 ADRS PAR 0 2 B022 JY0AP0
-BUS 0 ADRS PAR 1 2 A023 JY0AP1
-BUS 0 ADRS PAR 2 2 B017 JY0AP2
-BUS 0 ADRS PAR 3 2 A018 JY0AP3
17 DP0 -ADP0
17 DP1 -ADP1
17 DP2 -ADP2
17 DP3 -ADP3
B064 JXB0CI -CHAN 0 CACHE INVALIDATE
22 CI -LAST REQUEST

2 4" MAXIMUM LENGTH & NOT TERMINATED

3 6" MAXIMUM LENGTH

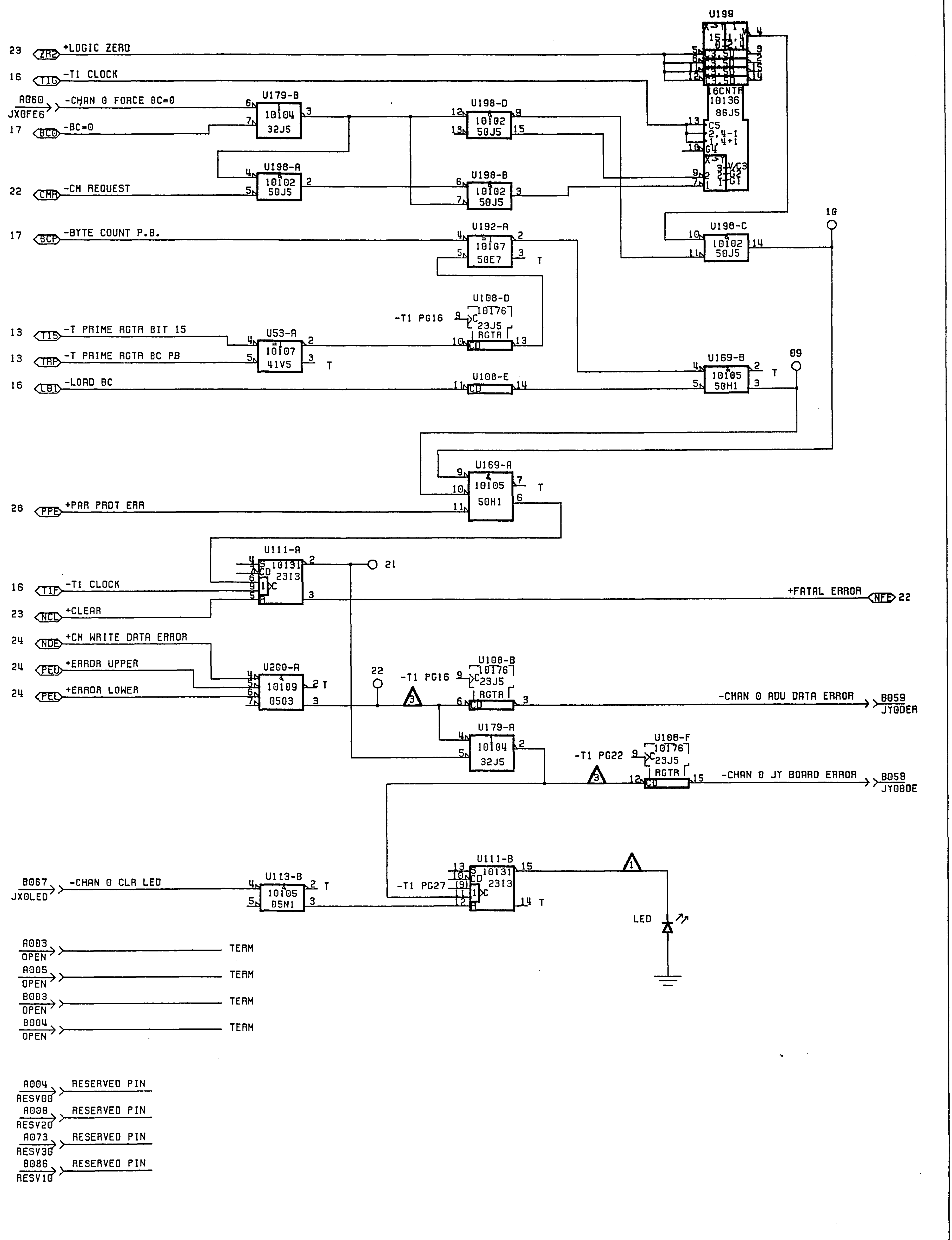
CONTROL DATA	CIO CHANNEL BOARD CM ADDRESS TO CMI TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 25	60462210	PAGE JY-25	

RMA PARITY PREDICTION (3.6)



CONTROL DATA	CIO CHANNEL BOARD RMA PARITY PREDICTION TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 26	60462210	PAGE JT-26	

ERROR FANIN (3.6)



△1 THIS LINE MUST BE TERMINATED

△3 6 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ERROR FANIN TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
			SHEET NO. 27	60462210	PAGE JY-27

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	16	-GATED T1 CLOCK	27	16	-T1 CLOCK
02	16	-INCREMENT RMA	28	22	-EVEN RESPONSE FLAG
03	15	-RMA BIT 63	29	21	-REQ CNT NOT ZERO
04	13	-BYTE COUNTER BIT 14	30	22	-CHANNEL GO
05	22	-INPUT	31	22	-ODD RESPONSE FLAG
06	16	-LOAD BYTE COUNT	32	24	-CM WRITE DATA ERROR
07	16	-RMA T PRIME EMPTY	33	24	+OUTPUT LOWER ERROR
08	16	-BC T PRIME EMPTY	34	02	-BUFFER ADRS BIT 3
09	27	+BYTE COUNT ERROR	35	20	-VALID OUTPUT DATA
10	27	+CM REQUEST ERROR	36	11	-OUTPUT DATA BIT 0
11	13	+WR T REG BITS 0-15	37	26	-PAR PREDICTOR F/F
12	15	+WR T REG BITS 32-47	38	20	-CWC BIT 1
13	14	+WR T REG BITS 16-31	39	20	-CWC BIT 0
14	22	-CM REQUEST	40	02	-BUFFER ADRS BIT 1
15	16	+LOAD RMA	41	02	-BUFFER ADRS BIT 2
16	22	-LAST CM REQUEST	42	24	-OUTPUT UPPER ERROR
17	23	-DECREMENT BYTE CNT	43	02	-BUFFER ADRS BIT 0
18	23	-CLEAR	44	02	-SELECT ADDRESS B
19	22	-EVEN REQUEST OUT	45	23	-BYTE COUNT EQUAL 2
20	22	-BUFF FULL/ODD REQ	46	22	-DMA MODE
21	27	-FATAL ERROR	47	05	-DATA BIT 0 TO CM
22	27	-DATA ERROR	48	05	-DATA BIT 16 TO CM
23	21	-INCREMENT REQ CNTR	49	20	-MWC NOT EQUAL ZERO
24	20	+RESPONSE CNT = 14	50	06	-DATA BIT 48 TO CM
25	20	+BUSY	51	06	-DATA BIT 32 TO CM
26	23	-BYTE COUNT = ZERO			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117,A037,A038,B037,B038,B128
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070
TERM	A003,B003,B004,A005
UNUSED	A004,A008,B008,A009,B009,A013,B013,A015,B015,A020,B020,A026,B026,A027,B027,A028,A031,B031,A032,B032,A033,B033,A036,A037,B037,A038,B038,A039,B039,A074,B074

CONTROL DATA	CIO CHANNEL BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JYH	B	DWG NO. 22105622	DATE 03/14/86	REV A
		SHEET NO. 28	60462210	PAGE JY-28	

Pages 4-811 through 4-840 deleted.
[JZ(53575518)-01 through -29.]

1JZH CIO CHANNEL BOARD ISI I/F

REVISION HISTORY B/M 41654701

DATE	REV	DESCRIPTION OF CHANGE	INIT
03/07/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	LHJ
01/27/87	B	ECO #48479 PAGES 8, 9, 10, 11, 12, 13,	
		22, 25, & 28	
01/21/88	C	ECO #49505 LOGIC DIAGRAM CORRECTIONS	
		TO SHEET 28.	DS

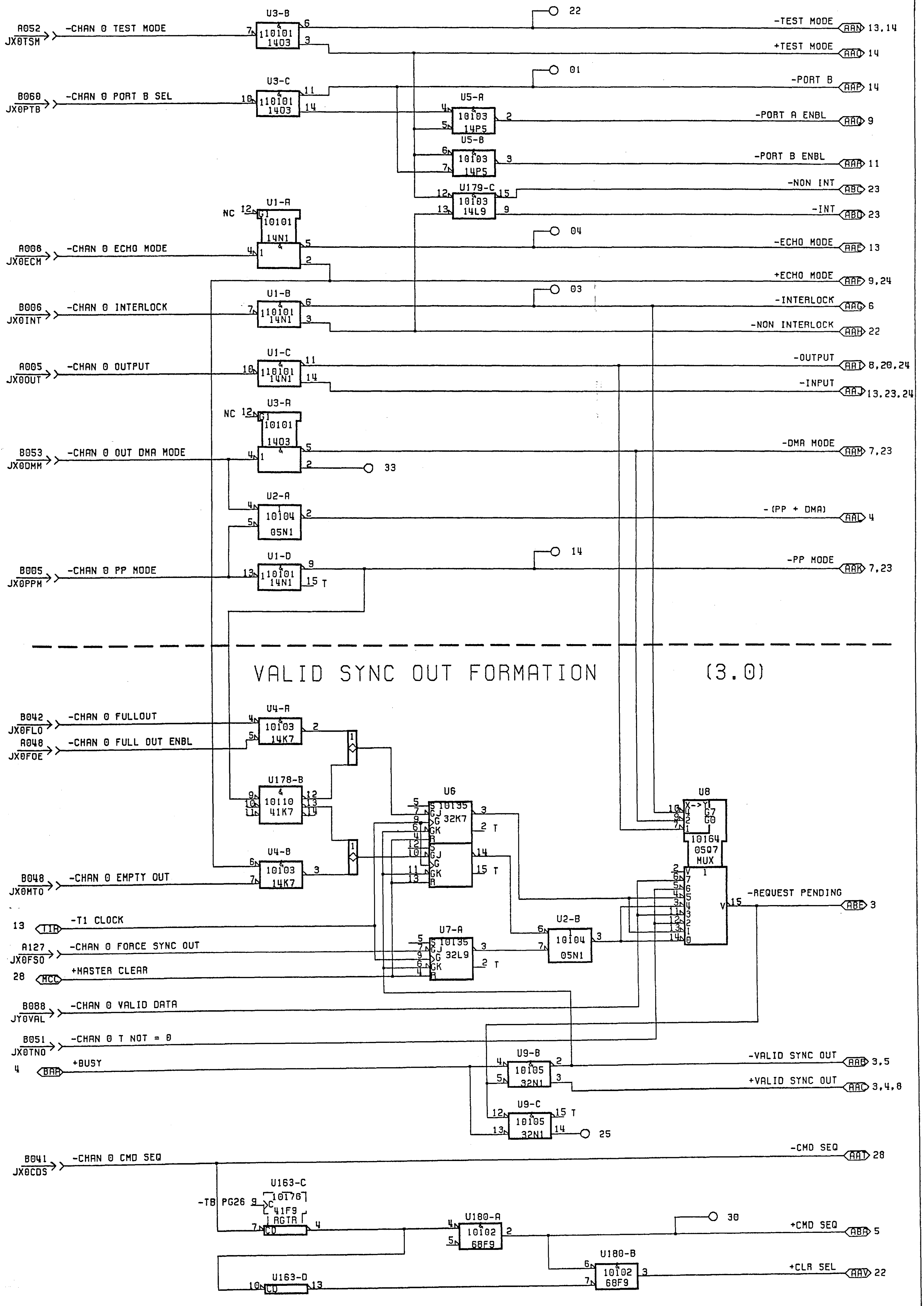
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D09,D12,D15,D18,D21
C09,C12,C15,C18,C21

DWN	L H JOHNSON	03/11/86
CHKD	L H JOHNSON	03/11/86
ENG	D A ZAHALAN	03/11/86
PUBS	R K BONDE	03/11/86
APP	D A ZAHALAN	03/11/86

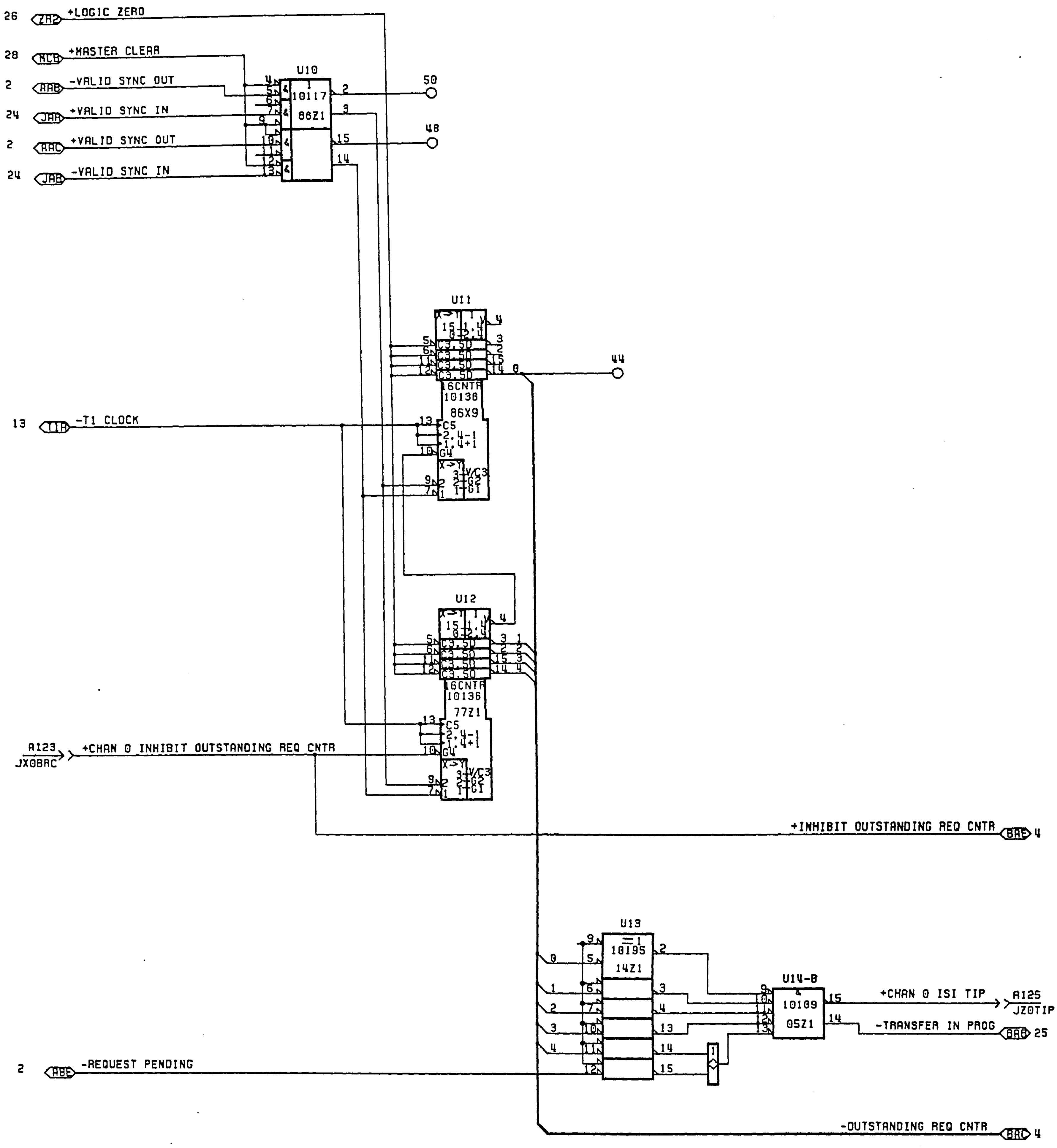
CONTROL DATA	REVISION HISTORY TYPE 1JZH	B	DWG NO. 22113019	DATE 06/15/88	REV C
		SHEET NO. 1	60462210	PAGE JZ-01	

MODE SELECT BITS (3.3)



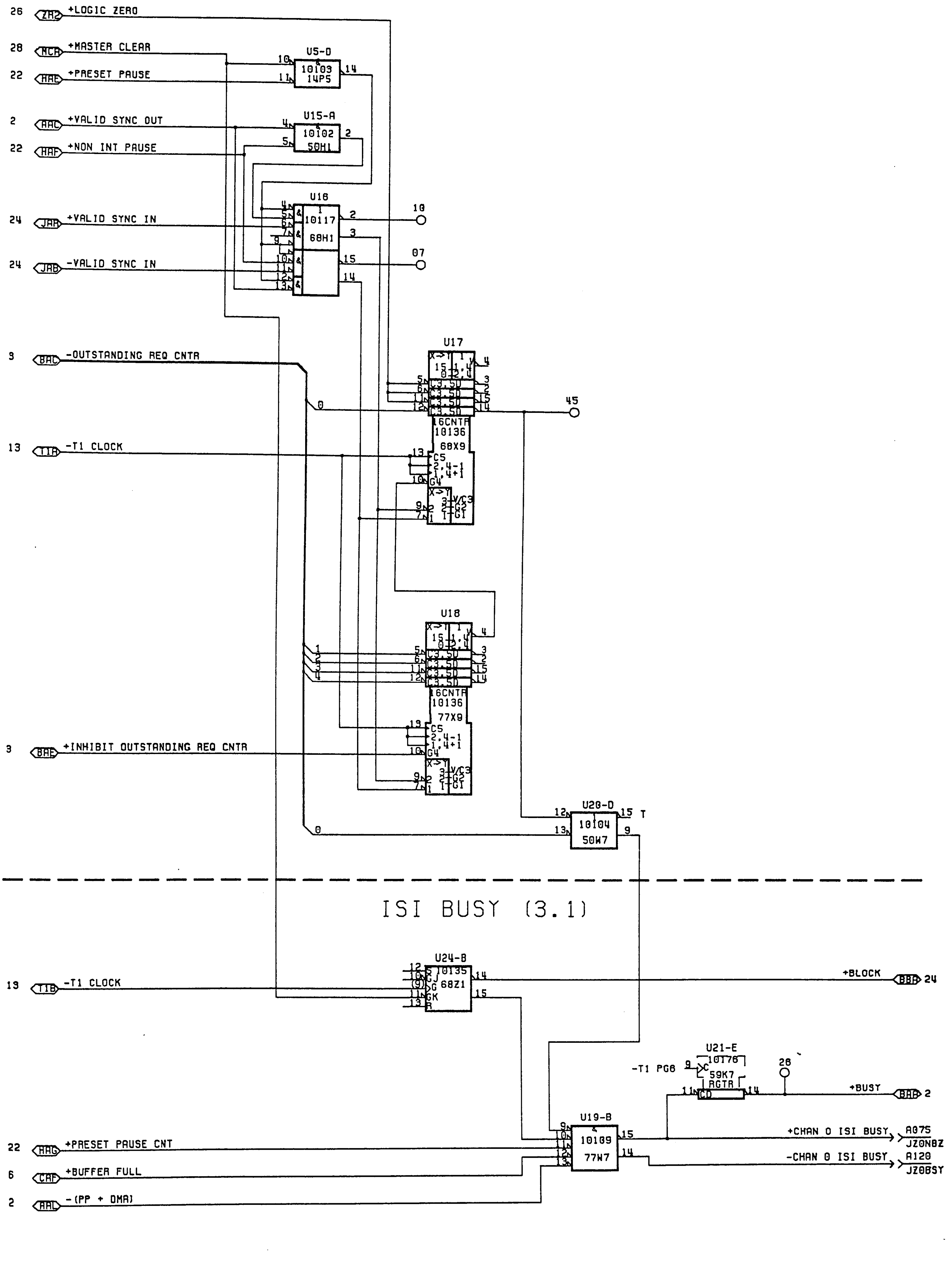
CONTROL DATA	CIO CHANNEL BOARD ISI I/F MODE SELECT BITS VALID SYNC OUT FORMATION TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 2	60462210	PAGE JZ-02	

OUTSTANDING REQ COUNTER (3.1)

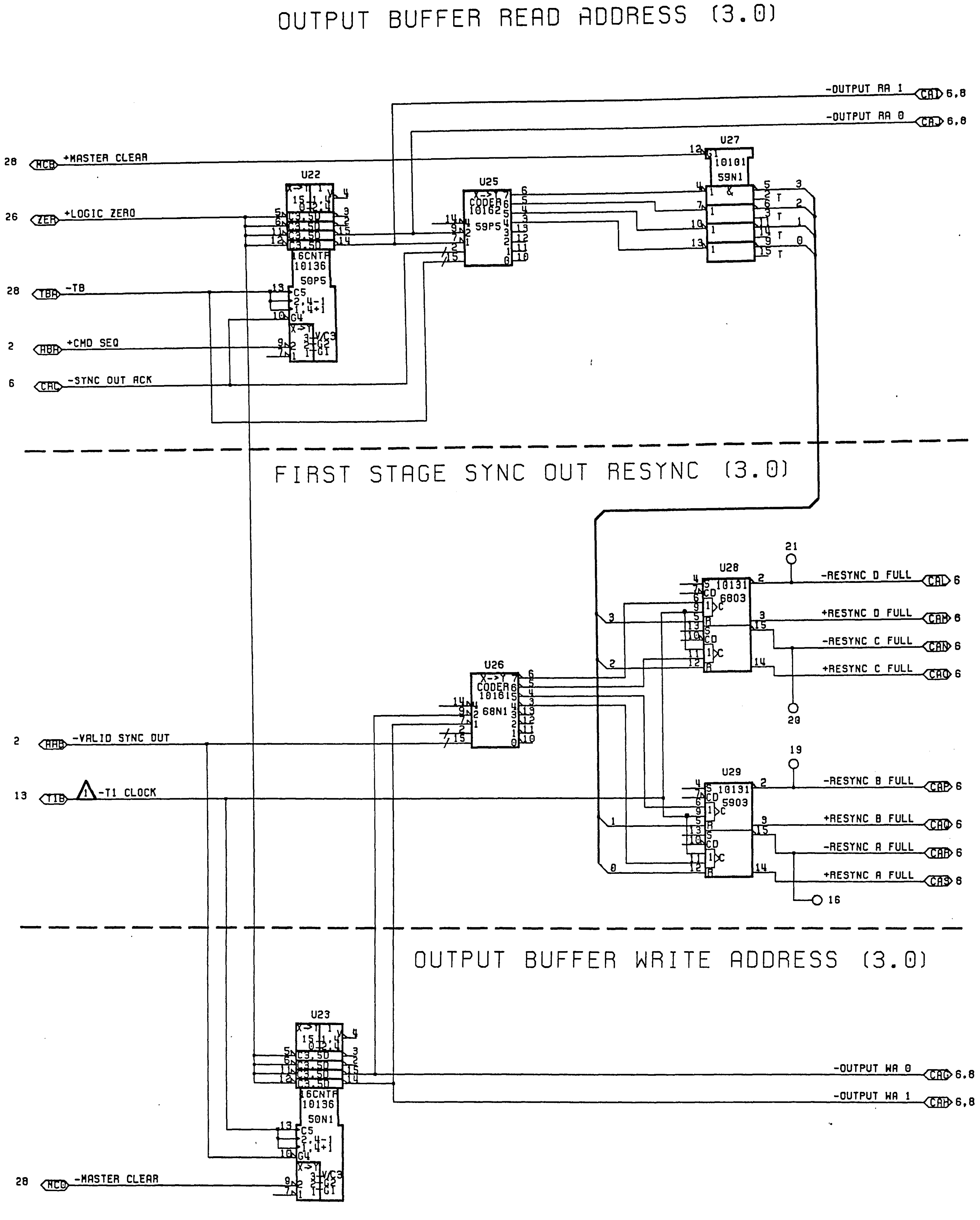


CONTROL DATA	CIO CHANNEL BOARD ISI I/F OUTSTANDING REQ COUNTER TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 3	60462210	PAGE JZ-03	

PAUSE COUNTER (3.1)



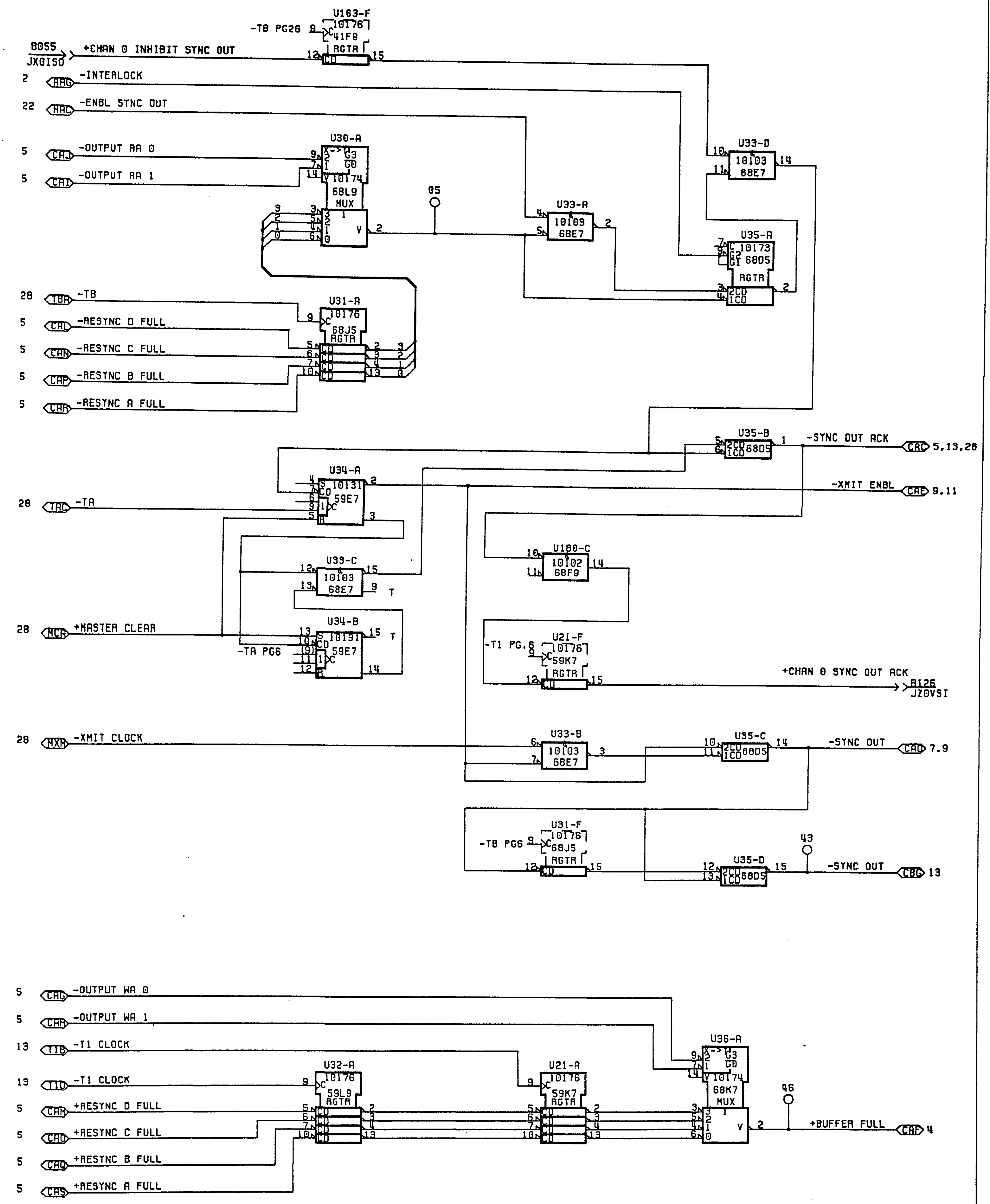
CONTROL DATA	CIO CHANNEL BOARD ISI I/F PAUSE COUNTER ISI BUSY TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 4	60462210	PAGE JZ-04	



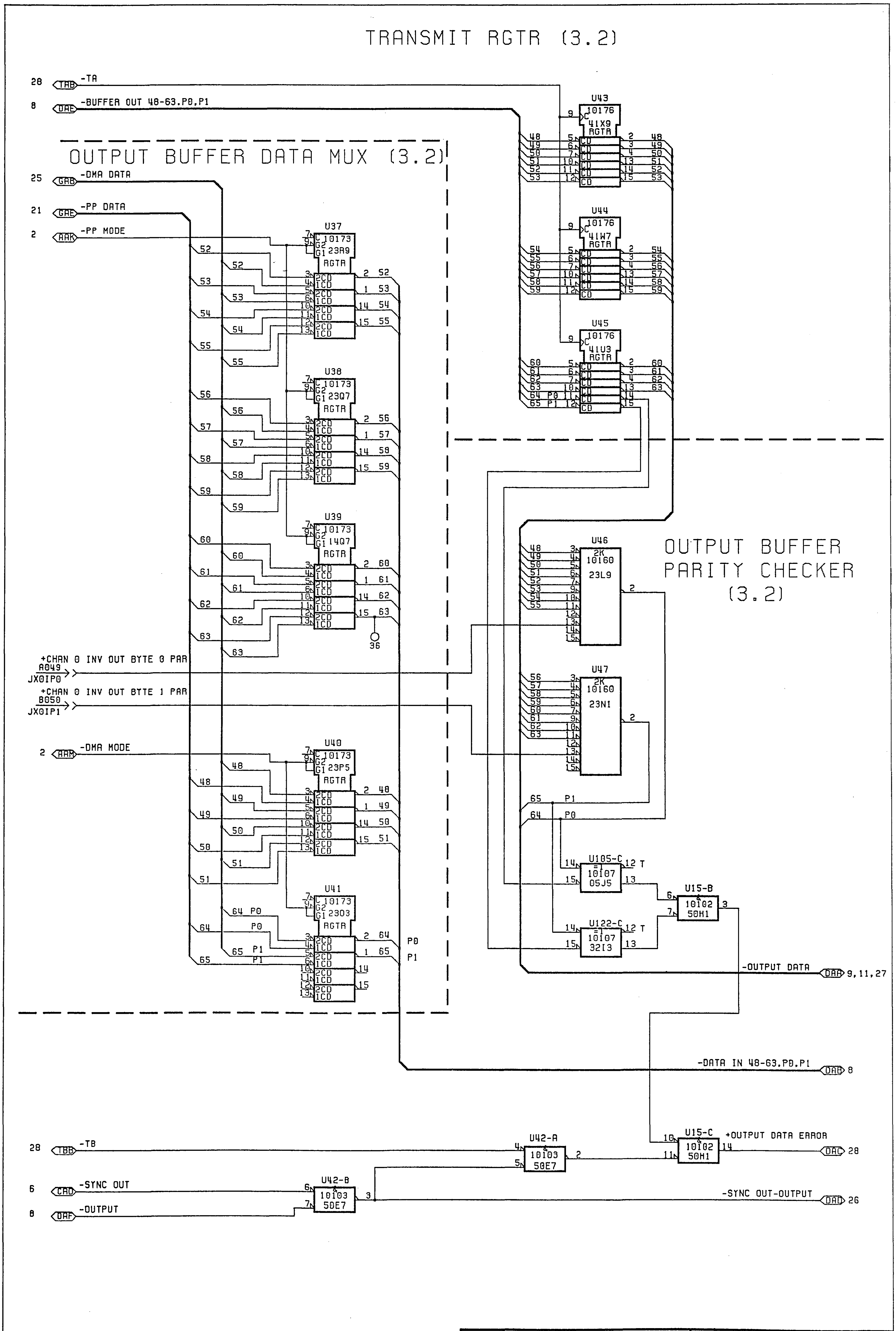
△ ROUTE CLOCK TO 10131 FIRST AND THEN TO 10136

CONTROL DATA	CIO CHANNEL BOARD ISI I/F OUTPUT BUFF READ & WRITE ADDR FIRST STAGE SYNC OUT RESYNC TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		N	SHEET NO. 5	60462210	PAGE JZ-05

SYNC OUT RESYNC STAGE 2&3 (3.0)



CONTROL DATA	CIO CHANNEL BOARD ISI I/F SYNC OUT RESYNC STAGE 2 & 3	B	DWG NO. 22113019	DATE 03/07/86	REV A
	TYPE 1JZH	SHEET NO. 6	60462210	PAGE JZ-06	

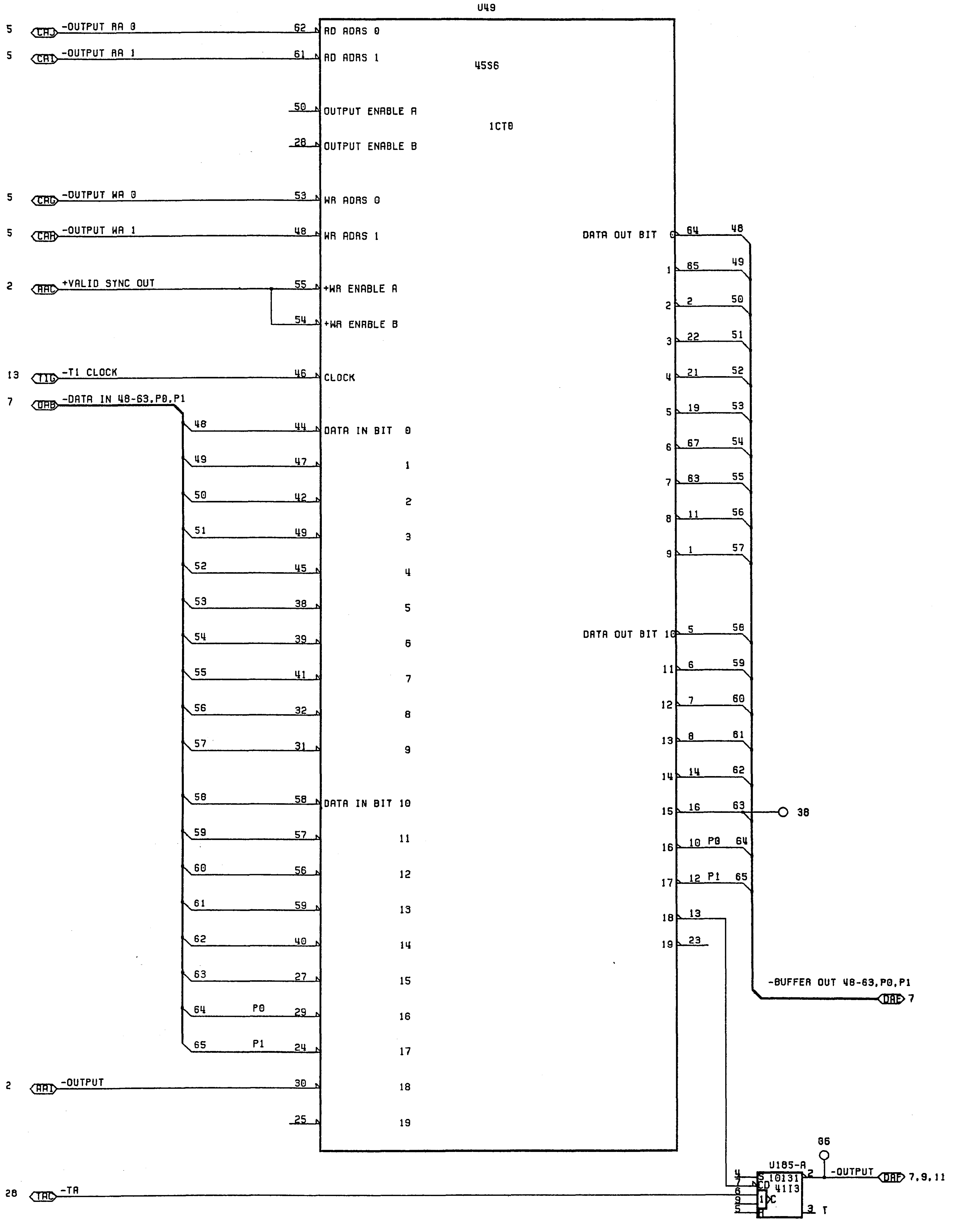


CONTROL DATA

CIO CHANNEL BOARD ISI I/F
OUTPUT BUFF DATA MUX, PARITY
CHECKER, & TRANSMIT RGTR
TYPE 1JZH

B	DWG NO. 22113019	DATE 03/07/86	REV A
SHEET NO. 7	60462210	PAGE JZ-07	

DATA OUTPUT BUFFER (3.2)

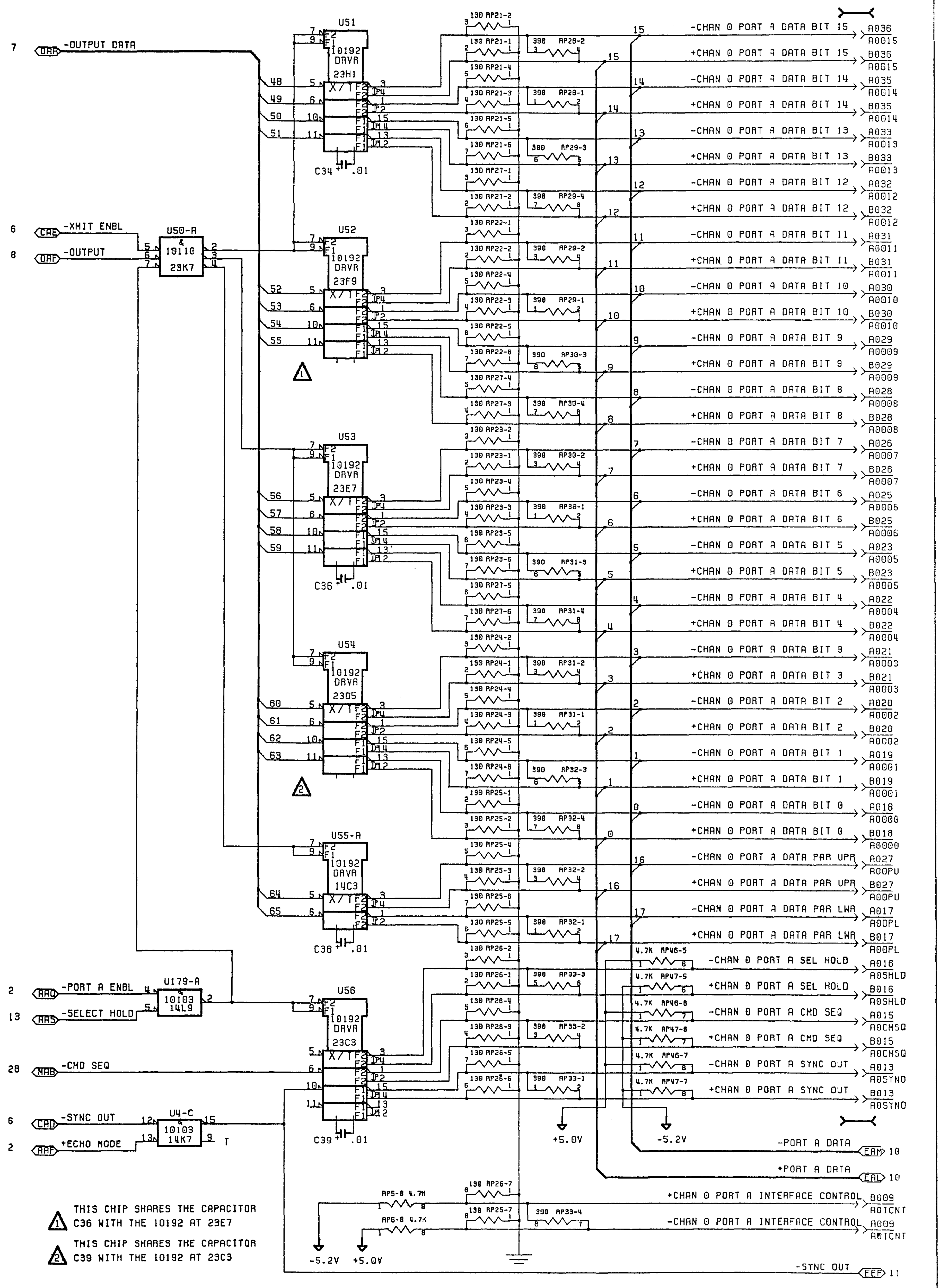


CONTROL DATA

CIO CHANNEL BOARD ISI I/F
DATA OUTPUT BUFFER
TYPE 1JZH

B	DWG NO.	22113019	DATE 01/27/87	REV B
N	SHEET NO. 8	60462210	PAGE JZ-08	

PORT A TRANSMITTERS (3.3)


7 -OUTPUT DATA (DAA)
6 -XMIT ENBL (CAE)
8 -OUTPUT (DAF)
U50-A 10110 23K7
U51 10192 DRVR 23H1
C34 .01
U52 10192 DRVR 23F9
U53 10192 DRVR 23E7
C36 .01
U54 10192 DRVR 23D5
U55-A 10192 DRVR 14C3
C38 .01
U56 10192 DRVR 23C3
C39 .01
2 -PORT A ENBL (AAQ)
13 -SELECT HOLD (AAS)
U179-A 10103 14L9
28 -CMD SEQ (HAB)
6 -SYNC OUT (CAD)
2 +ECHO MODE (AAF)
U4-C 10103 14K7
-CHAN 0 PORT A DATA BIT 15 A036 A0015
+CHAN 0 PORT A DATA BIT 15 B036 A0015
-CHAN 0 PORT A DATA BIT 14 A035 A0014
+CHAN 0 PORT A DATA BIT 14 B035 A0014
-CHAN 0 PORT A DATA BIT 13 A033 A0013
+CHAN 0 PORT A DATA BIT 13 B033 A0013
-CHAN 0 PORT A DATA BIT 12 A032 A0012
+CHAN 0 PORT A DATA BIT 12 B032 A0012
-CHAN 0 PORT A DATA BIT 11 A031 A0011
+CHAN 0 PORT A DATA BIT 11 B031 A0011
-CHAN 0 PORT A DATA BIT 10 A030 A0010
+CHAN 0 PORT A DATA BIT 10 B030 A0010
-CHAN 0 PORT A DATA BIT 9 A029 A0009
+CHAN 0 PORT A DATA BIT 9 B029 A0009
-CHAN 0 PORT A DATA BIT 8 A028 A0008
+CHAN 0 PORT A DATA BIT 8 B028 A0008
-CHAN 0 PORT A DATA BIT 7 A026 A0007
+CHAN 0 PORT A DATA BIT 7 B026 A0007
-CHAN 0 PORT A DATA BIT 6 A025 A0006
+CHAN 0 PORT A DATA BIT 6 B025 A0006
-CHAN 0 PORT A DATA BIT 5 A023 A0005
+CHAN 0 PORT A DATA BIT 5 B023 A0005
-CHAN 0 PORT A DATA BIT 4 A022 A0004
+CHAN 0 PORT A DATA BIT 4 B022 A0004
-CHAN 0 PORT A DATA BIT 3 A021 A0003
+CHAN 0 PORT A DATA BIT 3 B021 A0003
-CHAN 0 PORT A DATA BIT 2 A020 A0002
+CHAN 0 PORT A DATA BIT 2 B020 A0002
-CHAN 0 PORT A DATA BIT 1 A019 A0001
+CHAN 0 PORT A DATA BIT 1 B019 A0001
-CHAN 0 PORT A DATA BIT 0 A018 A0000
+CHAN 0 PORT A DATA BIT 0 B018 A0000
-CHAN 0 PORT A DATA PAR UPR A027 A0OPU
+CHAN 0 PORT A DATA PAR UPR B027 A0OPU
-CHAN 0 PORT A DATA PAR LWR A017 A0OPL
+CHAN 0 PORT A DATA PAR LWR B017 A0OPL
-CHAN 0 PORT A SEL HOLD A016 A0SHLD
+CHAN 0 PORT A SEL HOLD B016 A0SHLD
-CHAN 0 PORT A CMD SEQ A015 A0CMSQ
+CHAN 0 PORT A CMD SEQ B015 A0CMSQ
-CHAN 0 PORT A SYNC OUT A013 A0SYNO
+CHAN 0 PORT A SYNC OUT B013 A0SYNO
+5.0V
-5.2V
-PORT A DATA EAM 10
+PORT A DATA EAL 10
+CHAN 0 PORT A INTERFACE CONTROL B009 A0ICNT
-CHAN 0 PORT A INTERFACE CONTROL A009 A0ICNT
-SYNC OUT EEF 11
RP5-8 4.7K
RP6-8 4.7K
130 RP26-7
130 RP25-7
390 RP33-4

1 THIS CHIP SHARES THE CAPACITOR C36 WITH THE 10192 AT 23E7

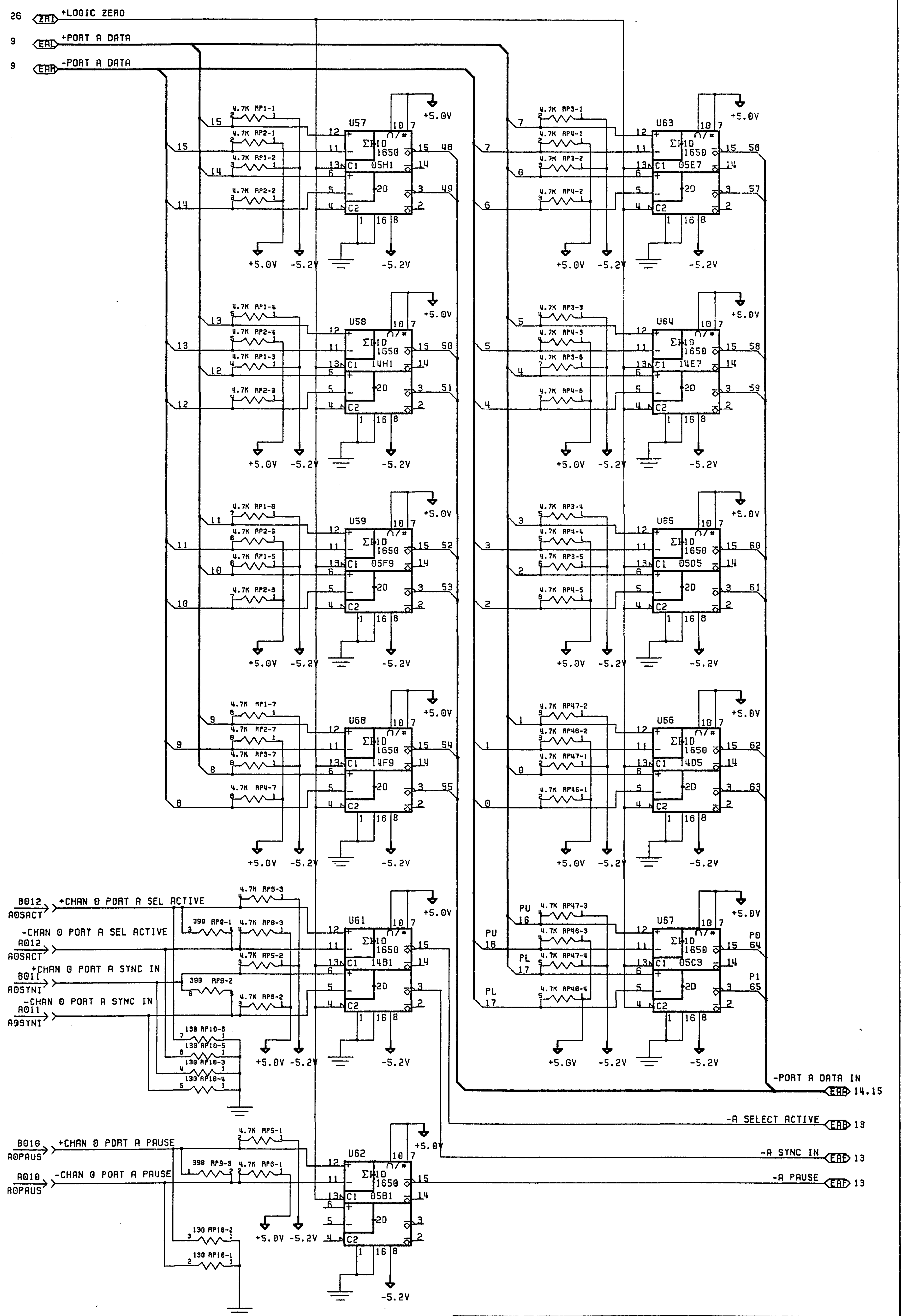
2 THIS CHIP SHARES THE CAPACITOR C39 WITH THE 10192 AT 23C3

CONTROL DATA

CIO CHANNEL BOARD ISI I/F
PORT A TRANSMITTERS
TYPE 1JZH

	DWG NO.	DATE	REV
B	22113019	01/27/87	B
SHEET NO. 9	60462210	PAGE JZ-09	

PORT A RECEIVERS (3.3)



CONTROL DATA

CIO CHANNEL BOARD ISI I/F
PORT A RECEIVERS

TYPE 1JZH

B

DWG NO. 22113019

DATE 01/27/87

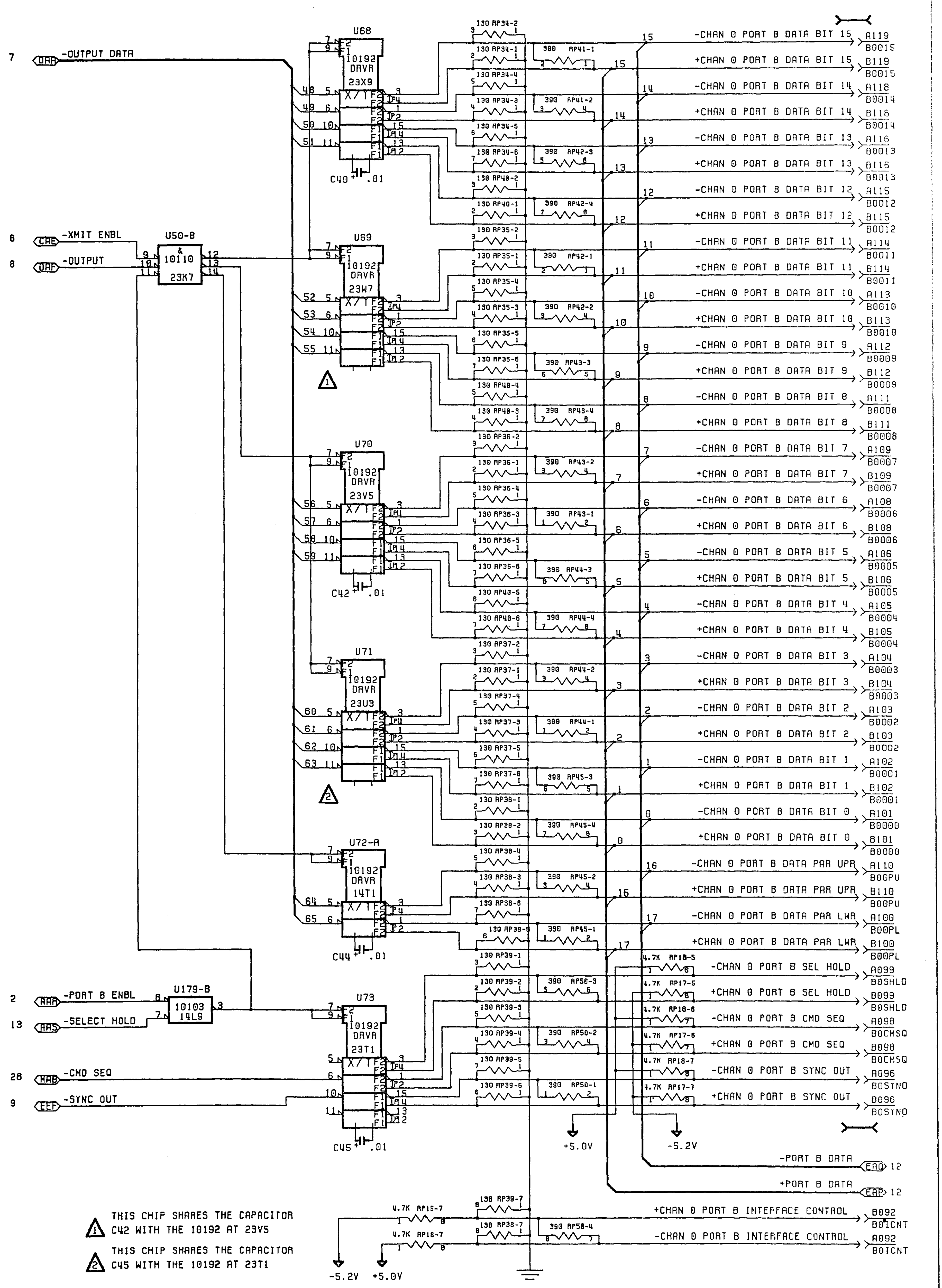
REV B

SHEET NO. 10

60462210

PAGE JZ-10

PORT B TRANSMITTERS (3.3)


7 DAA -OUTPUT DATA
6 CAE -XMIT ENBL
8 DAF -OUTPUT
U50-B 10110 23K7
2 AAA -PORT B ENBL
13 AAS -SELECT HOLD
U179-B 10103 14L9
28 AAB -CMD SEQ
9 EEF -SYNC OUT
U68 10192 DRVR 23X9
C40 .01
U69 10192 DRVR 23W7
U70 10192 DRVR 23V5
C42 .01
U71 10192 DRVR 23U3
U72-A 10192 DRVR 14T1
C44 .01
U73 10192 DRVR 23T1
C45 .01
130 RP34 · 130 RP35 · 130 RP36 · 130 RP37 · 130 RP38 · 130 RP39 · 130 RP40
390 RP41 · 390 RP42 · 390 RP43 · 390 RP44 · 390 RP45 · 390 RP50
4.7K RP15 · 4.7K RP16 · 4.7K RP17 · 4.7K RP18
-CHAN 0 PORT B DATA BIT 15 A119 B0015
+CHAN 0 PORT B DATA BIT 15 B119 B0015
-CHAN 0 PORT B DATA BIT 14 A118 B0014
+CHAN 0 PORT B DATA BIT 14 B118 B0014
-CHAN 0 PORT B DATA BIT 13 A116 B0013
+CHAN 0 PORT B DATA BIT 13 B116 B0013
-CHAN 0 PORT B DATA BIT 12 A115 B0012
+CHAN 0 PORT B DATA BIT 12 B115 B0012
-CHAN 0 PORT B DATA BIT 11 A114 B0011
+CHAN 0 PORT B DATA BIT 11 B114 B0011
-CHAN 0 PORT B DATA BIT 10 A113 B0010
+CHAN 0 PORT B DATA BIT 10 B113 B0010
-CHAN 0 PORT B DATA BIT 9 A112 B0009
+CHAN 0 PORT B DATA BIT 9 B112 B0009
-CHAN 0 PORT B DATA BIT 8 A111 B0008
+CHAN 0 PORT B DATA BIT 8 B111 B0008
-CHAN 0 PORT B DATA BIT 7 A109 B0007
+CHAN 0 PORT B DATA BIT 7 B109 B0007
-CHAN 0 PORT B DATA BIT 6 A108 B0006
+CHAN 0 PORT B DATA BIT 6 B108 B0006
-CHAN 0 PORT B DATA BIT 5 A106 B0005
+CHAN 0 PORT B DATA BIT 5 B106 B0005
-CHAN 0 PORT B DATA BIT 4 A105 B0004
+CHAN 0 PORT B DATA BIT 4 B105 B0004
-CHAN 0 PORT B DATA BIT 3 A104 B0003
+CHAN 0 PORT B DATA BIT 3 B104 B0003
-CHAN 0 PORT B DATA BIT 2 A103 B0002
+CHAN 0 PORT B DATA BIT 2 B103 B0002
-CHAN 0 PORT B DATA BIT 1 A102 B0001
+CHAN 0 PORT B DATA BIT 1 B102 B0001
-CHAN 0 PORT B DATA BIT 0 A101 B0000
+CHAN 0 PORT B DATA BIT 0 B101 B0000
-CHAN 0 PORT B DATA PAR UPR A110 B00PU
+CHAN 0 PORT B DATA PAR UPR B110 B00PU
-CHAN 0 PORT B DATA PAR LWR A100 B00PL
+CHAN 0 PORT B DATA PAR LWR B100 B00PL
-CHAN 0 PORT B SEL HOLD A099 B0SHLD
+CHAN 0 PORT B SEL HOLD B099 B0SHLD
-CHAN 0 PORT B CMD SEQ A098 B0CMSQ
+CHAN 0 PORT B CMD SEQ B098 B0CMSQ
-CHAN 0 PORT B SYNC OUT A096 B0STNO
+CHAN 0 PORT B SYNC OUT B096 B0STNO
+5.0V
-5.2V
-PORT B DATA EAQ 12
+PORT B DATA EAP 12
+CHAN 0 PORT B INTERFACE CONTROL B092 B0ICNT
-CHAN 0 PORT B INTERFACE CONTROL A092 B0ICNT
-5.2V +5.0V

⚠1 THIS CHIP SHARES THE CAPACITOR C42 WITH THE 10192 AT 23V5

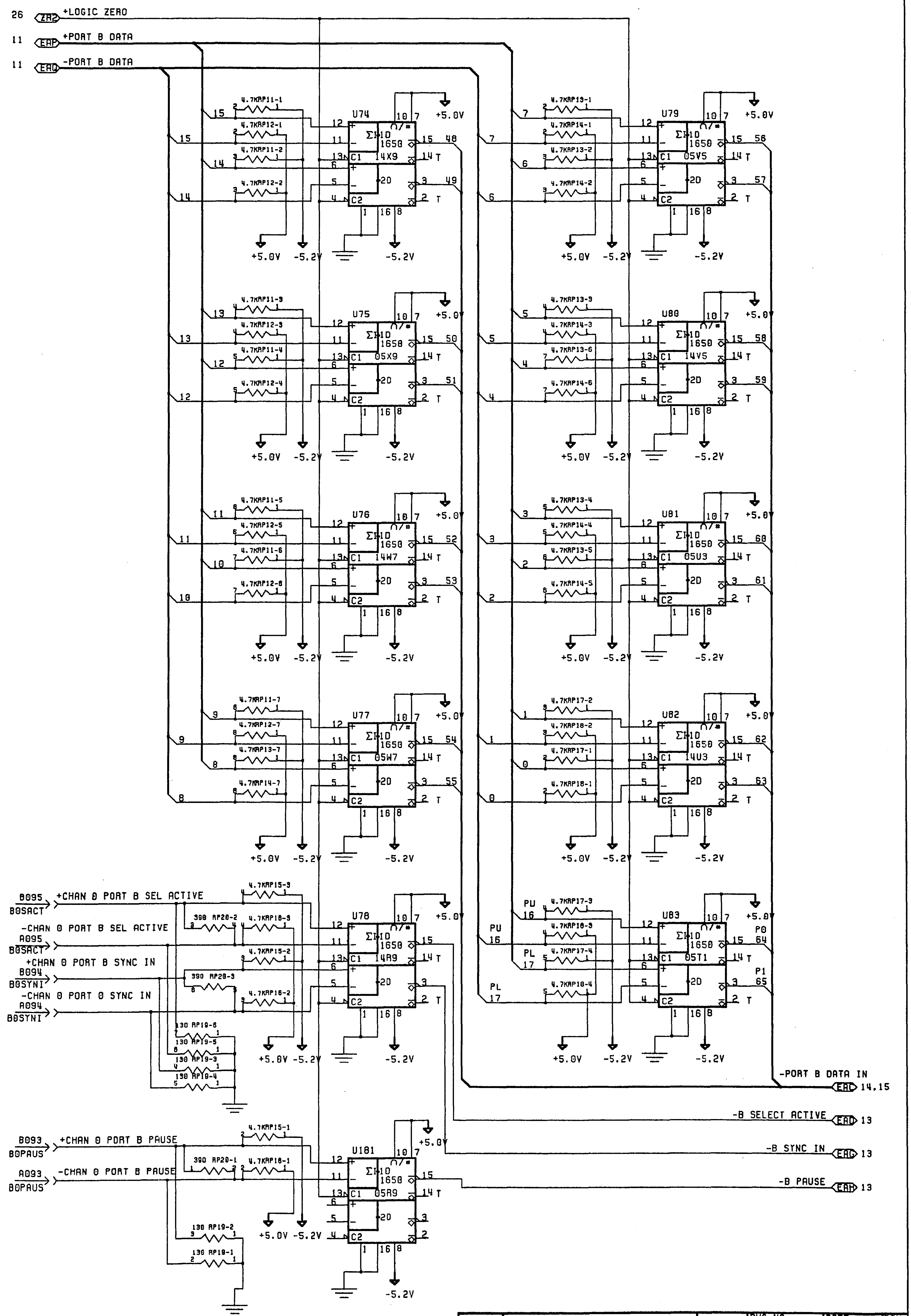
⚠2 THIS CHIP SHARES THE CAPACITOR C45 WITH THE 10192 AT 23T1

CONTROL DATA

CIO CHANNEL BOARD ISI I/F
PORT B TRANSMITTERS
TYPE 1JZH

B	DWG NO. 22113019		DATE 01/27/87	REV B
N	SHEET NO. 11	60462210	PAGE JZ-11	

PORT B RECEIVERS (3.3)



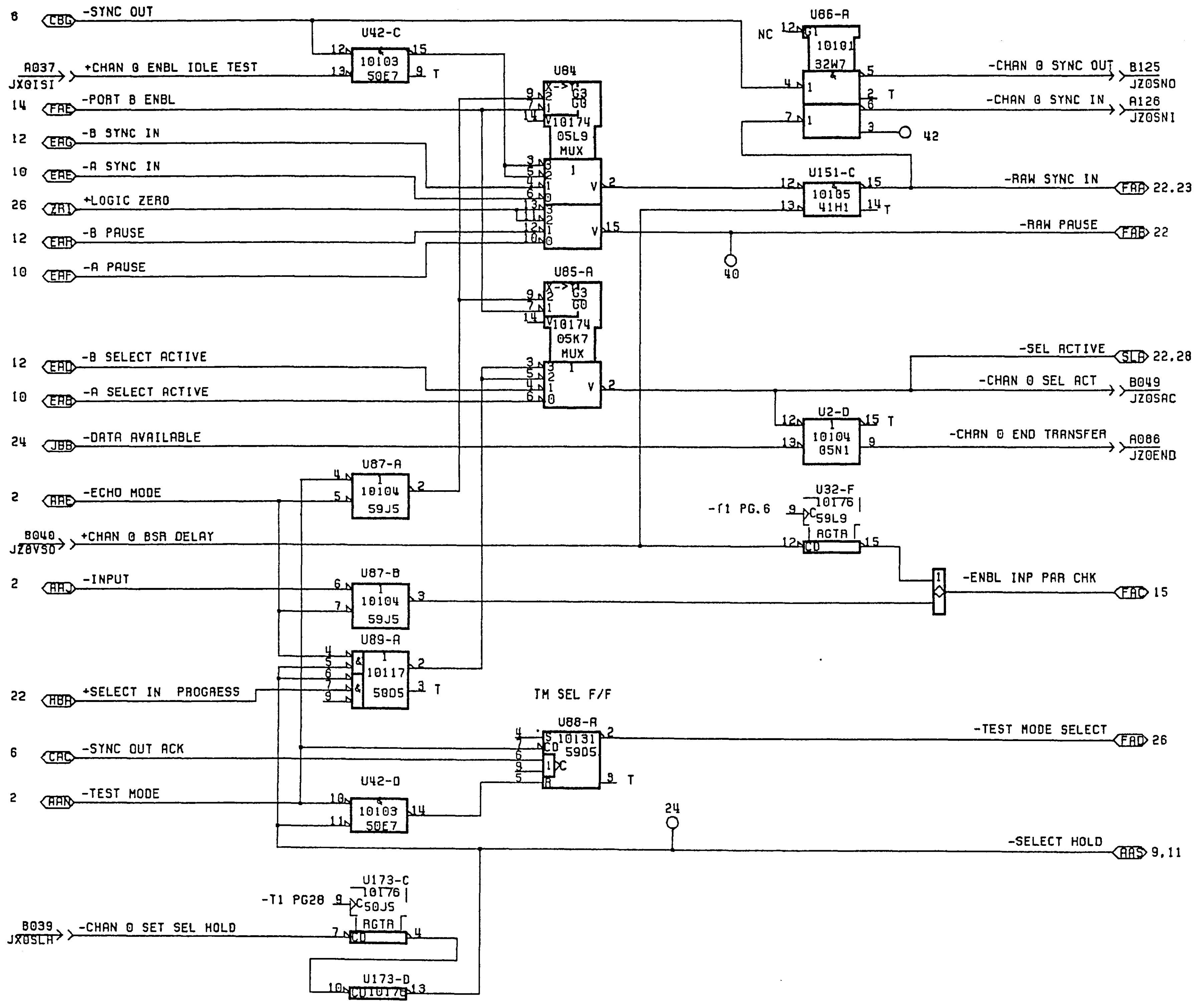
CONTROL DATA

CID CHANNEL BOARD ISI I/F
PORT B RECEIVERS

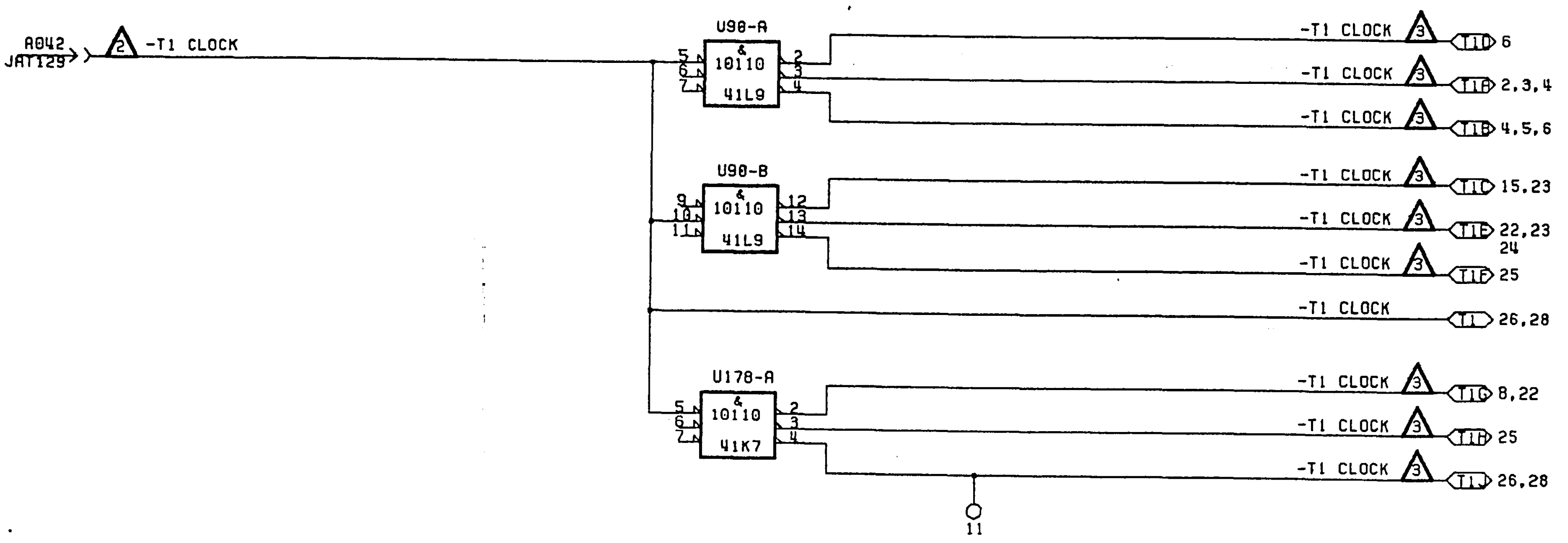
TYPE 1JZH

B	DWG NO. 22113019		DATE 03/07/86	REV B
SHEET NO. 12		60462210	PAGE JZ-12	

CONTROL SIGNAL INPUT MUX (3.3)



T1 CLOCK FANOUT

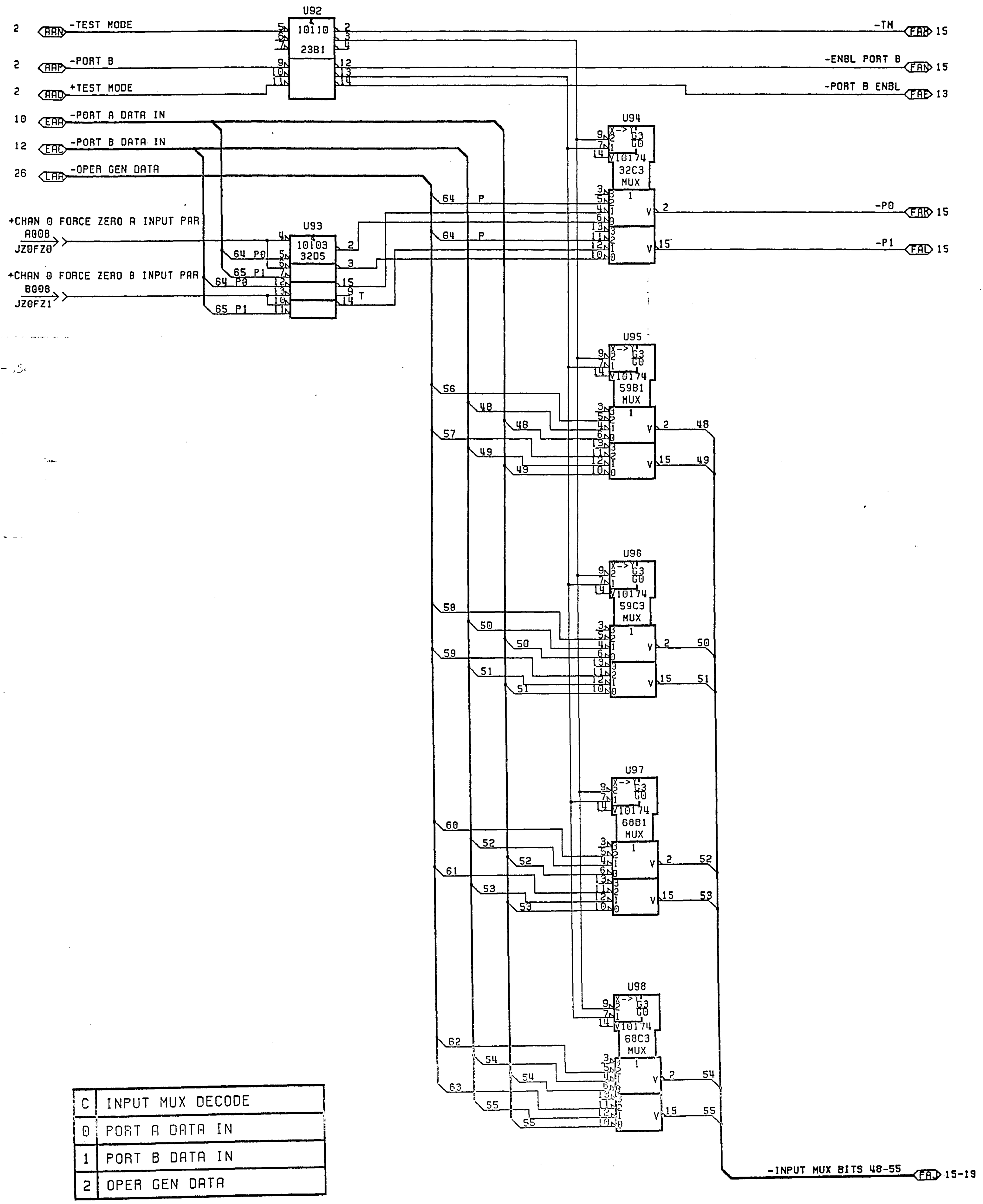


△2 7 INCH MAXIMUM LENGTH

△3 12 INCH MAXIMUM LENGTH

CONTROL DATA	CIO CHANNEL BOARD ISI I/F CONTROL SIGNAL INPUT MUX T1 CLOCK FANOUT TYPE 1JZH	B	DWG NO. 22113019	DATE 01/27/87	REV B
		N	SHEET NO. 13	60462210	PAGE JZ-13

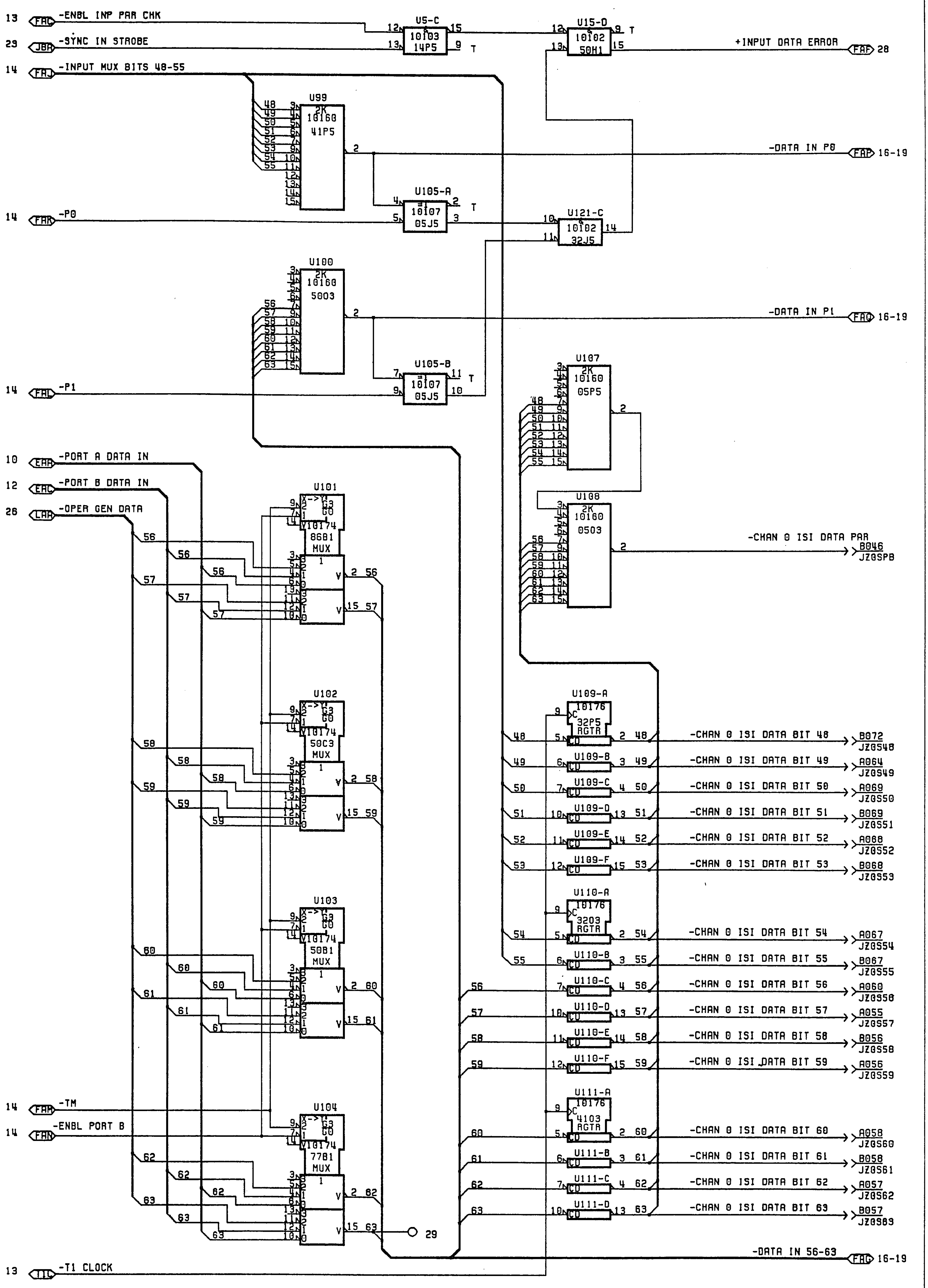
PORT FAN-IN INPUT MUX BITS 48-55 (3.4)



C	INPUT MUX DECODE
0	PORT A DATA IN
1	PORT B DATA IN
2	OPER GEN DATA

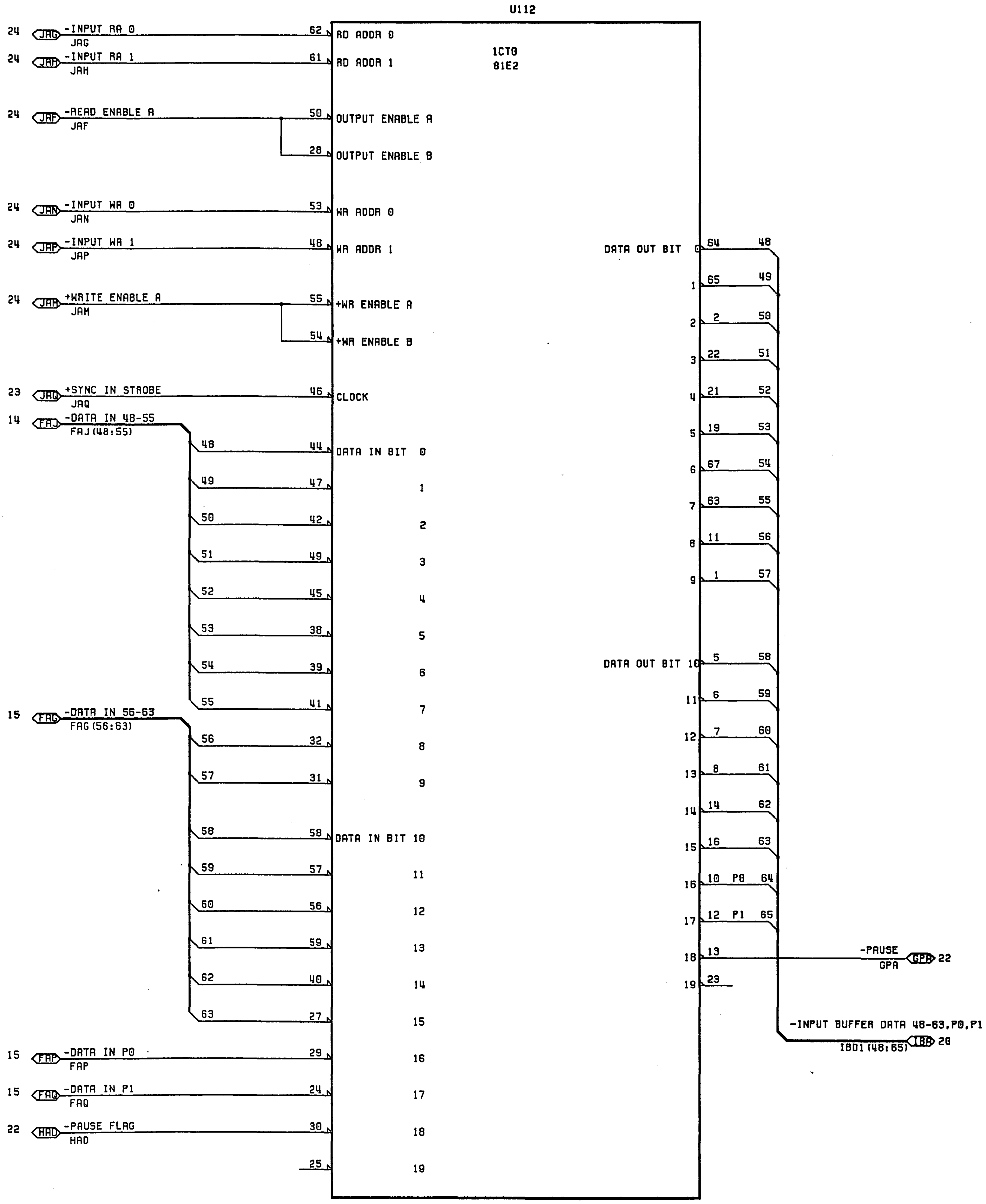
CONTROL DATA	CIO CHANNEL BOARD ISI I/F PORT FAN-IN INPUT MUX BITS 48-55 TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
			SHEET NO. 14	60462210	PAGE JZ-14

PORT FAN-IN INPUT MUX BITS 56-63 (3.4)


13 FAC -ENBL INP PAR CHK
23 JBA -SYNC IN STROBE
14 FAJ -INPUT MUX BITS 48-55
U5-C 10103 14P5
U15-D 10102 50H1
+INPUT DATA ERROR FAF 28
U99 2K 10160 41P5
-DATA IN P0 FAP 16-19
14 FAK -P0
U105-A 10107 05J5
U121-C 10102 32J5
U100 2K 10160 50O3
-DATA IN P1 FAQ 16-19
14 FAL -P1
U105-B 10107 05J5
U107 2K 10160 05P5
U108 2K 10160 05O3
-CHAN 0 ISI DATA PAR B046 JZ0SPB
10 EAA -PORT A DATA IN
12 EAC -PORT B DATA IN
26 LAA -OPER GEN DATA
U101 10174 86B1 MUX
U102 10174 50C3 MUX
U103 10174 50B1 MUX
U104 10174 77B1 MUX
14 FAM -TM
14 FAN -ENBL PORT B
U109-A 10176 32P5 RGTR
U110-A 10176 32O3 RGTR
U111-A 10176 41O3 RGTR
-CHAN 0 ISI DATA BIT 48 B072 JZ0S48
-CHAN 0 ISI DATA BIT 49 A064 JZ0S49
-CHAN 0 ISI DATA BIT 50 A069 JZ0S50
-CHAN 0 ISI DATA BIT 51 B069 JZ0S51
-CHAN 0 ISI DATA BIT 52 A068 JZ0S52
-CHAN 0 ISI DATA BIT 53 B068 JZ0S53
-CHAN 0 ISI DATA BIT 54 A067 JZ0S54
-CHAN 0 ISI DATA BIT 55 B067 JZ0S55
-CHAN 0 ISI DATA BIT 56 A060 JZ0S56
-CHAN 0 ISI DATA BIT 57 A055 JZ0S57
-CHAN 0 ISI DATA BIT 58 B056 JZ0S58
-CHAN 0 ISI DATA BIT 59 A056 JZ0S59
-CHAN 0 ISI DATA BIT 60 A058 JZ0S60
-CHAN 0 ISI DATA BIT 61 B058 JZ0S61
-CHAN 0 ISI DATA BIT 62 A057 JZ0S62
-CHAN 0 ISI DATA BIT 63 B057 JZ0S63
29
-DATA IN 56-63 FAR 16-19
13 TIC -T1 CLOCK

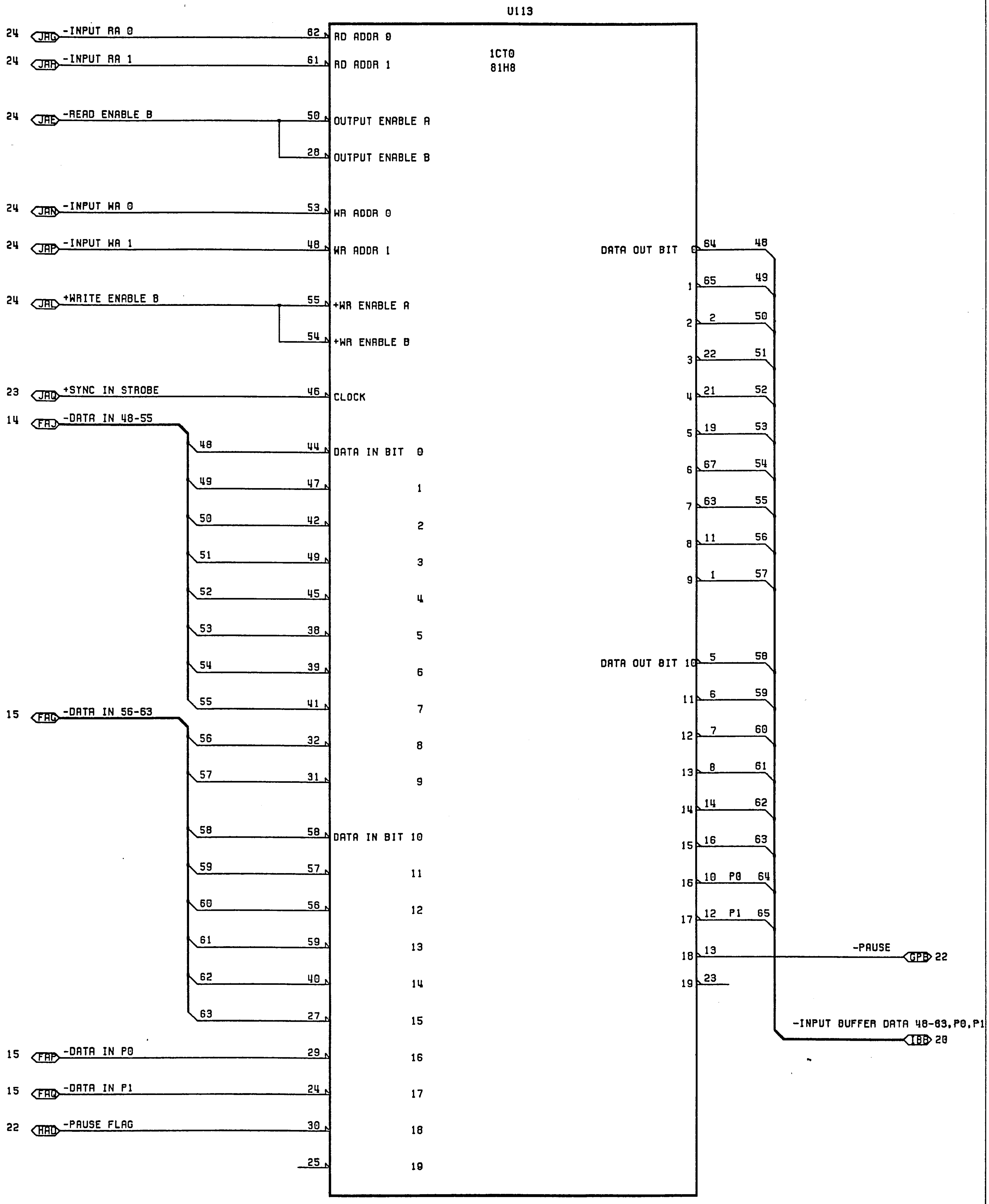
CONTROL DATA	CIO CHANNEL BOARD ISI I/F PORT FAN-IN INPUT MUX BITS 56-63	B	DWG NO. 22113019	DATE 03/07/86	REV A
	TYPE 1JZH	N	SHEET NO. 15	60462210	PAGE JZ-15

DATA INPUT BUFFER
CHIP A (3.4)


U112
1CT0
81E2
24 JAG -INPUT RA 0 JAG 62 RD ADDR 0
24 JAH -INPUT RA 1 JAH 61 RD ADDR 1
24 JAF -READ ENABLE A JAF 50 OUTPUT ENABLE A
28 OUTPUT ENABLE B
24 JAN -INPUT WA 0 JAN 53 WA ADDR 0
24 JAP -INPUT WA 1 JAP 48 WA ADDR 1
24 JAM +WRITE ENABLE A JAM 55 +WA ENABLE A
54 +WA ENABLE B
23 JAQ +SYNC IN STROBE JAQ 46 CLOCK
14 FAJ -DATA IN 48-55 FAJ (48:55)
48 44 DATA IN BIT 0
49 47 1
50 42 2
51 49 3
52 45 4
53 38 5
54 39 6
55 41 7
15 FAG -DATA IN 56-63 FAG (56:63)
56 32 8
57 31 9
58 58 DATA IN BIT 10
59 57 11
60 56 12
61 59 13
62 40 14
63 27 15
15 FAP -DATA IN P0 FAP 29 16
15 FAQ -DATA IN P1 FAQ 24 17
22 HAD -PAUSE FLAG HAD 30 18
25 19
DATA OUT BIT 0 64 48
1 65 49
2 2 50
3 22 51
4 21 52
5 19 53
6 67 54
7 63 55
8 11 56
9 1 57
DATA OUT BIT 10 5 58
11 6 59
12 7 60
13 8 61
14 14 62
15 16 63
16 10 P0 64
17 12 P1 65
18 13 -PAUSE GPA GPA 22
19 23
-INPUT BUFFER DATA 48-63,P0,P1
IBD1 (48:65) IBD 20

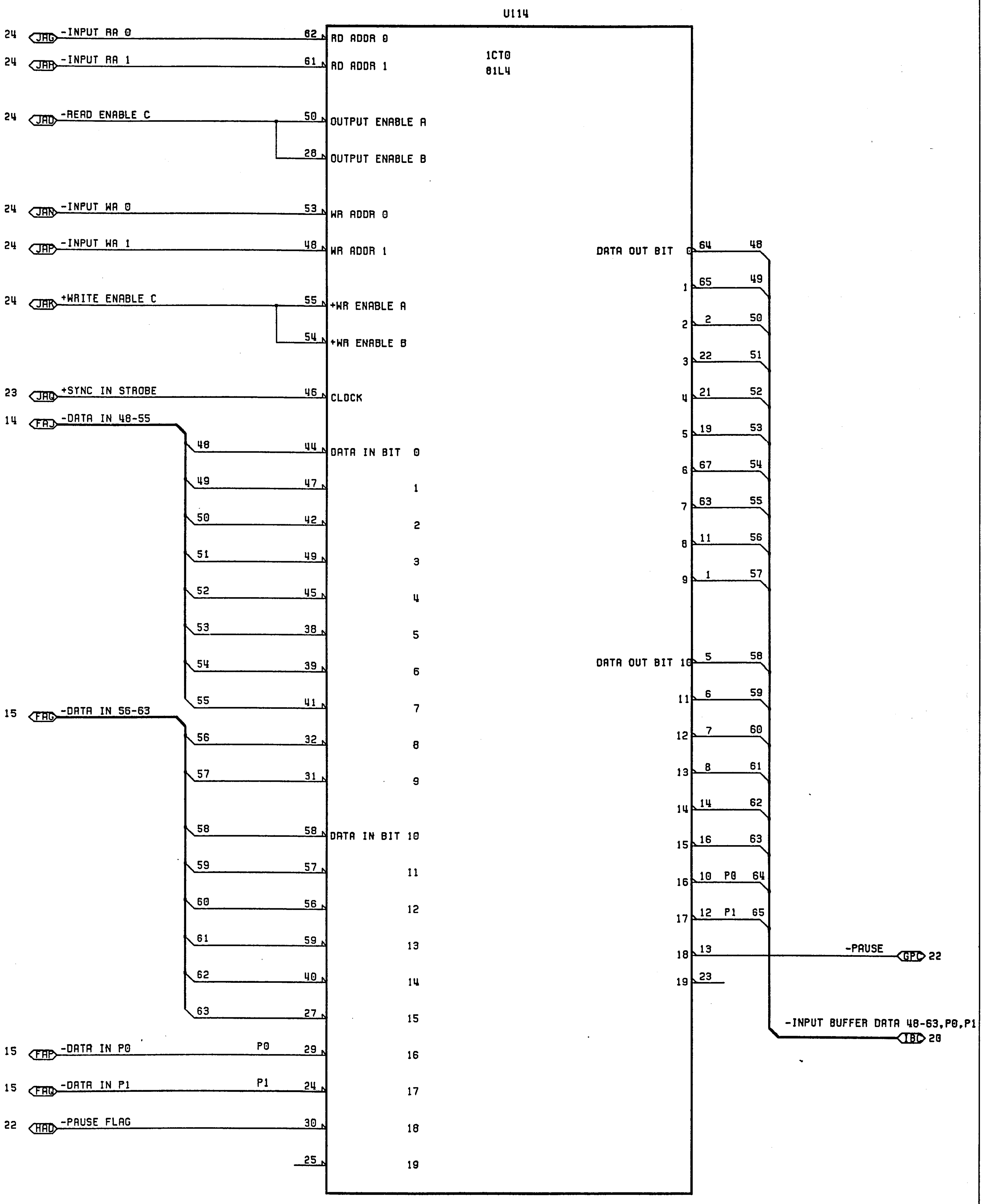
CONTROL DATA	CIO CHANNEL BOARD ISI I/F DATA INPUT BUFFER CHIP A TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
	N	SHEET NO. 16	60462210	PAGE JZ-16	

DATA INPUT BUFFER
CHIP B (3.4)



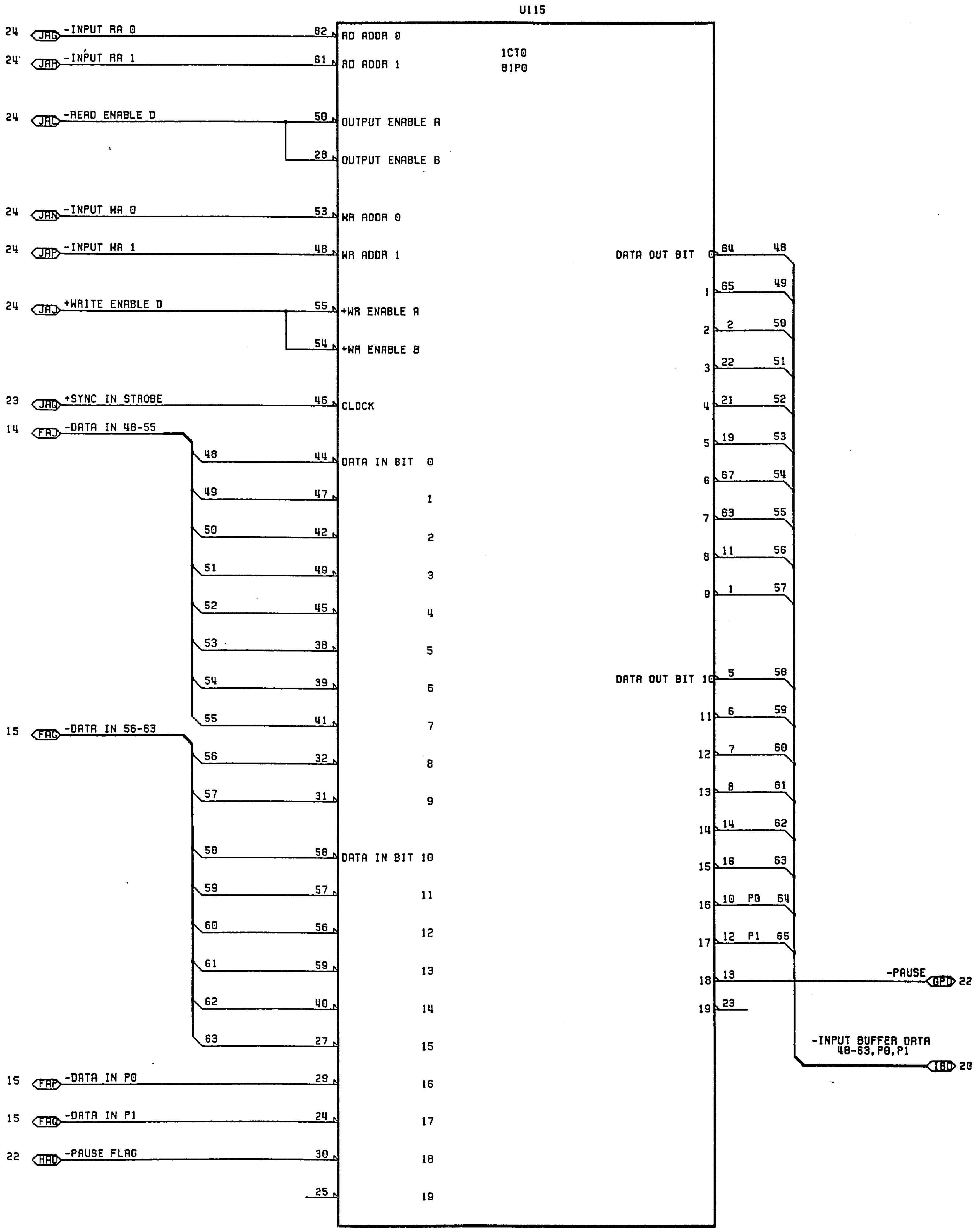
CONTROL DATA	CIO CHANNEL BOARD ISI I/F DATA INPUT BUFFER CHIP B TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 17	60462210	PAGE JZ-17	

DATA INPUT BUFFER
CHIP C (3.4)

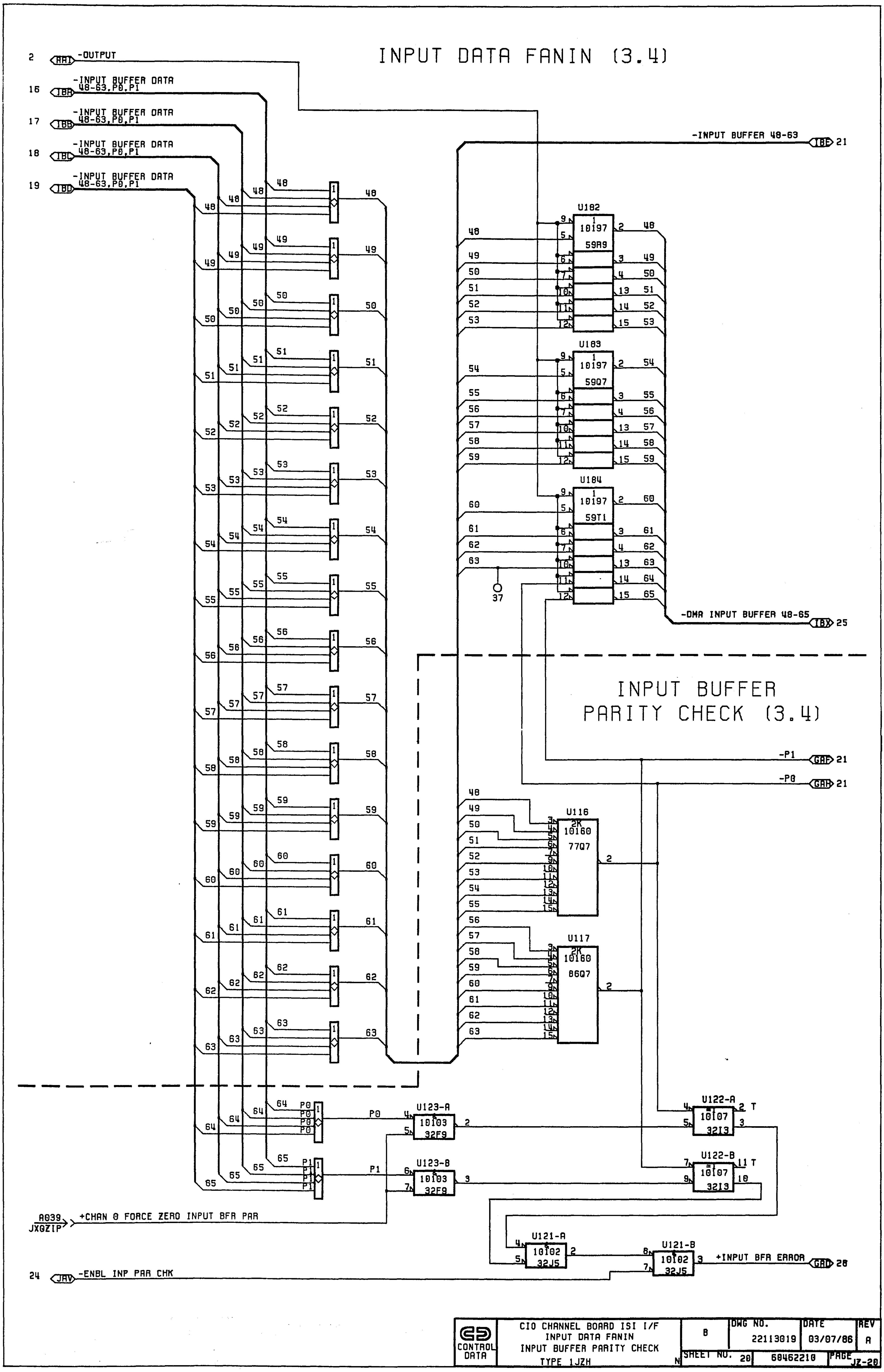


CONTROL DATA	CIO CHANNEL BOARD ISI I/F DATA INPUT BUFFER CHIP C TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 18	60462210	PAGE JZ-18	

DATA INPUT BUFFER
CHIP D (3.4)

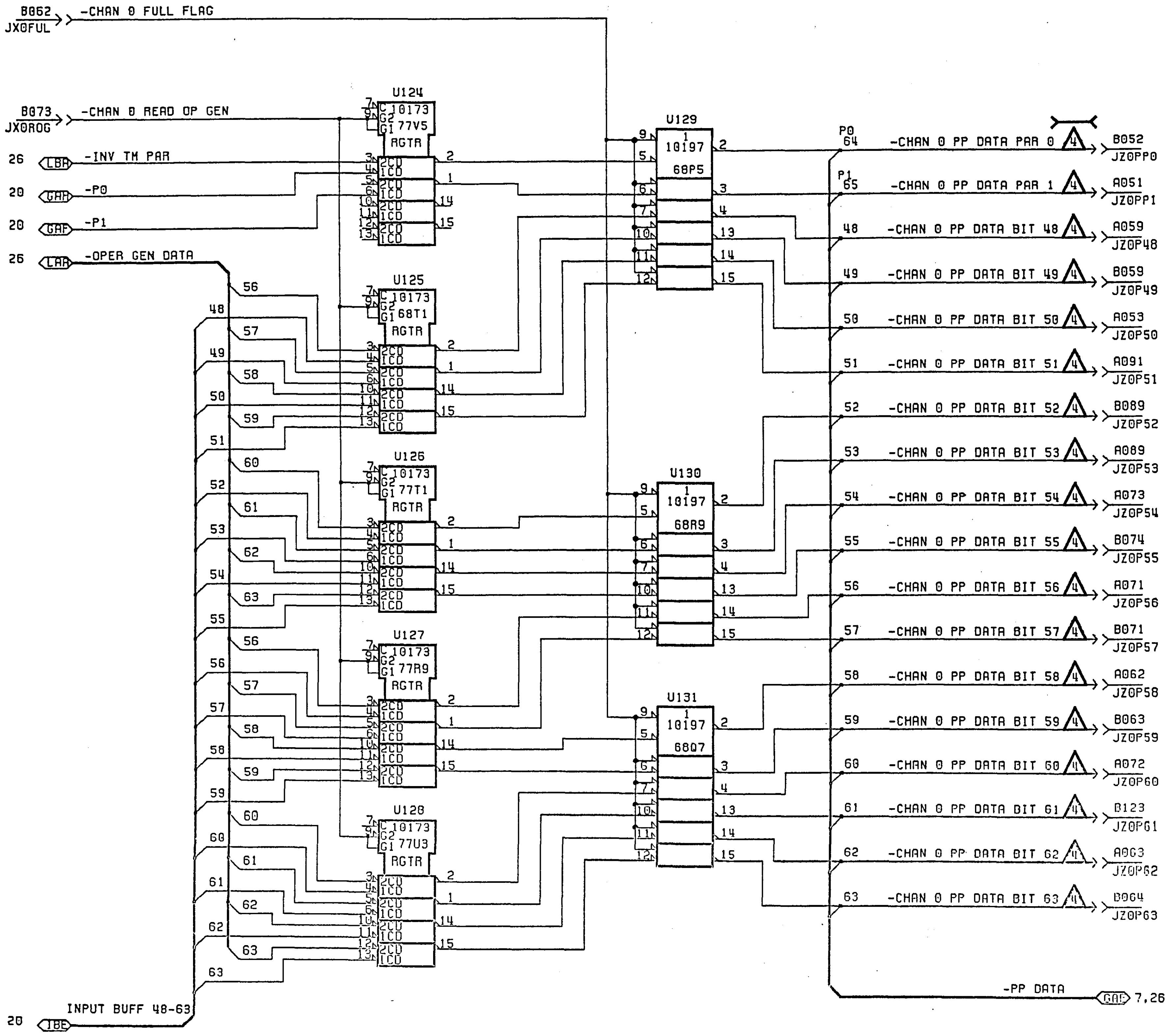


CONTROL DATA	CIO CHANNEL BOARD ISI I/F DATA INPUT BUFFER CHIP D TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 19	60462210	PAGE JZ-19	



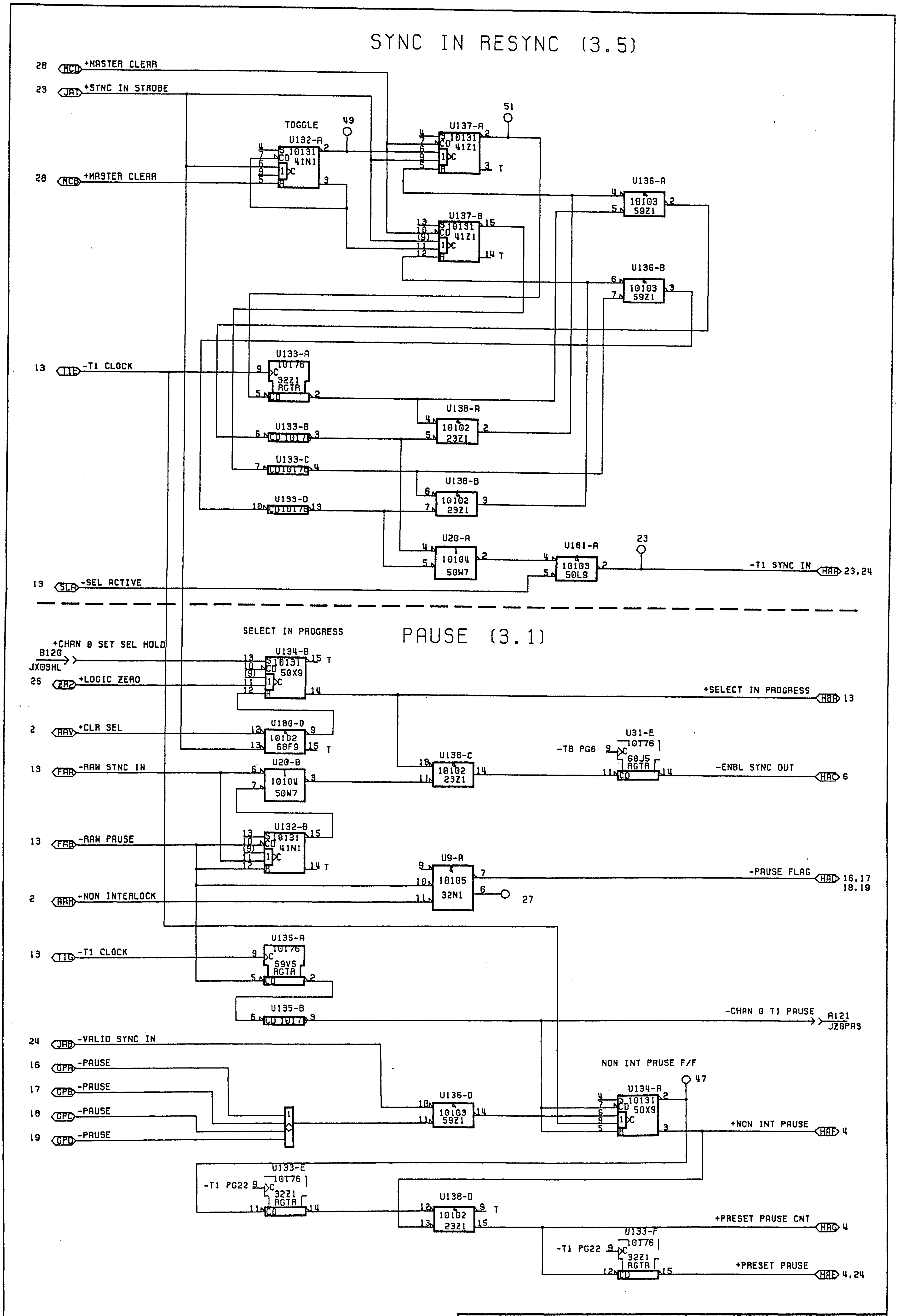
CONTROL DATA	CIO CHANNEL BOARD ISI I/F INPUT DATA FANIN INPUT BUFFER PARITY CHECK TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
			SHEET NO. 20	60462210	PAGE JZ-20

PP INPUT DATA MUX (3.4)


B062 JX0FUL -CHAN 0 FULL FLAG
B073 JX0ROG -CHAN 0 READ OP GEN
26 LBA -INV TM PAR
20 GAH -P0
20 GAF -P1
26 LAA -OPER GEN DATA
20 IBE INPUT BUFF 48-63
U124 10173 77V5 RGTR
U125 10173 68T1 RGTR
U126 10173 77T1 RGTR
U127 10173 77A9 RGTR
U128 10173 77U3 RGTR
U129 10197 68P5
U130 10197 68A9
U131 10197 66Q7
P0 64 -CHAN 0 PP DATA PAR 0 B052 JZ0PP0
P1 65 -CHAN 0 PP DATA PAR 1 A051 JZ0PP1
48 -CHAN 0 PP DATA BIT 48 A059 JZ0P48
49 -CHAN 0 PP DATA BIT 49 B059 JZ0P49
50 -CHAN 0 PP DATA BIT 50 A053 JZ0P50
51 -CHAN 0 PP DATA BIT 51 A091 JZ0P51
52 -CHAN 0 PP DATA BIT 52 B089 JZ0P52
53 -CHAN 0 PP DATA BIT 53 A089 JZ0P53
54 -CHAN 0 PP DATA BIT 54 A073 JZ0P54
55 -CHAN 0 PP DATA BIT 55 B074 JZ0P55
56 -CHAN 0 PP DATA BIT 56 A071 JZ0P56
57 -CHAN 0 PP DATA BIT 57 B071 JZ0P57
58 -CHAN 0 PP DATA BIT 58 A062 JZ0P58
59 -CHAN 0 PP DATA BIT 59 B063 JZ0P59
60 -CHAN 0 PP DATA BIT 60 A072 JZ0P60
61 -CHAN 0 PP DATA BIT 61 B123 JZ0P61
62 -CHAN 0 PP DATA BIT 62 A063 JZ0P62
63 -CHAN 0 PP DATA BIT 63 B064 JZ0P63
-PP DATA GAP 7,26

4 TERMINATE AT FARTHEST POINT FROM CONNECTOR PIN

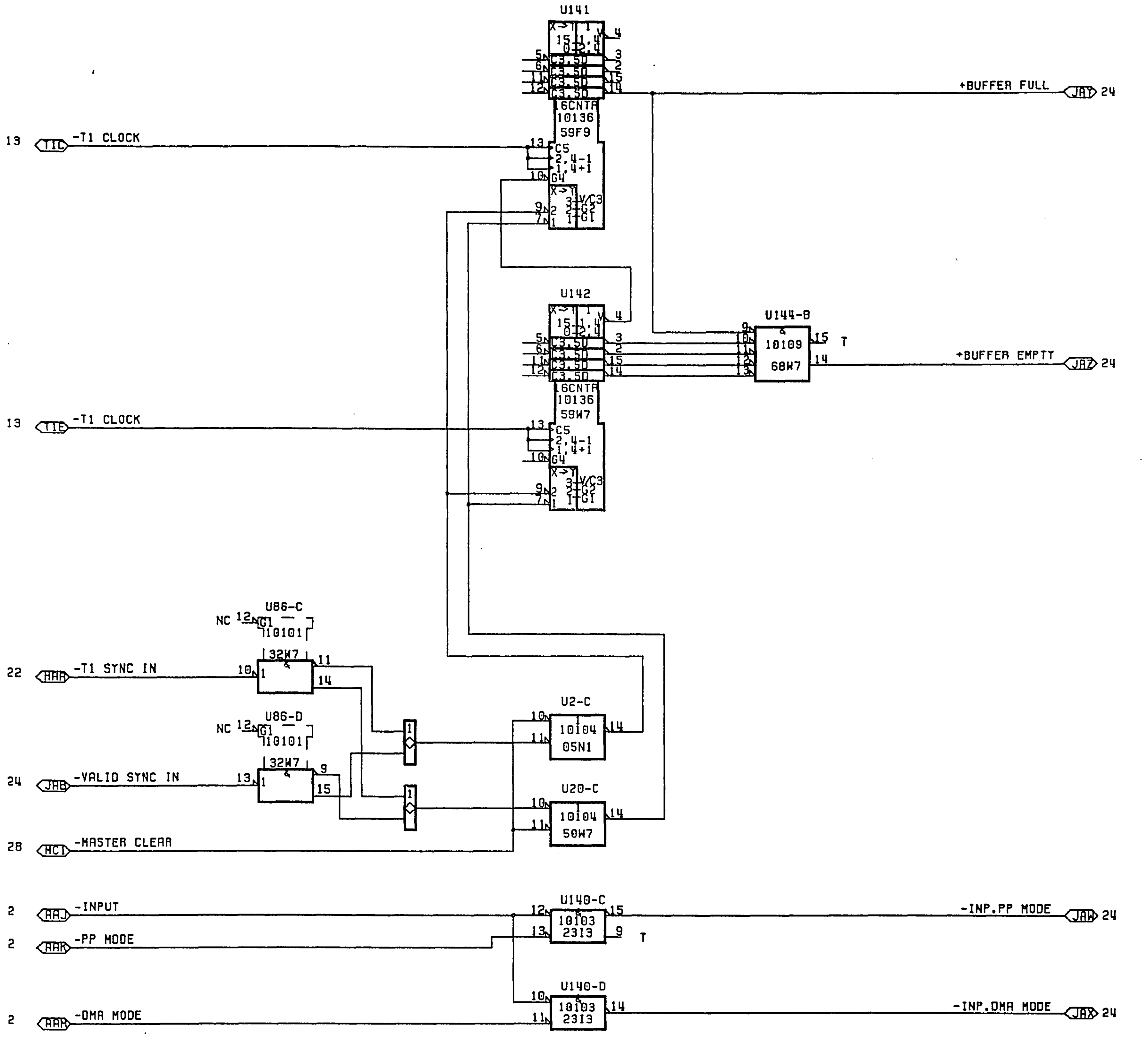
CONTROL DATA	CIO CHANNEL BOARD ISI I/F PP INPUT DATA MUX	B	DWG NO. 22113019	DATE 03/07/86	REV A
	TYPE 1JZH	N	SHEET NO. 21	60462210	PAGE JZ-21



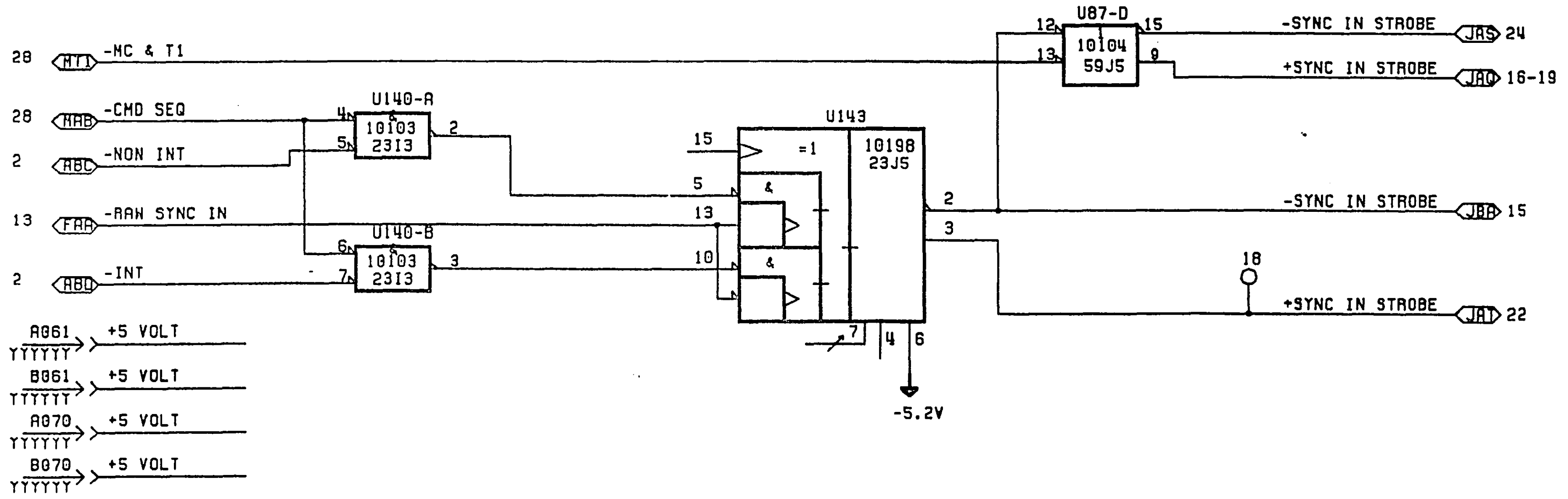
CONTROL DATA

CIO CHANNEL BOARD ISI I/F SYNC IN RESYNC, PAUSE TYPE 1JZH	B	DWG NO. 22113019		DATE 01/27/87	REV B
N		SHEET NO.	22	60462210	PAGE JZ-22

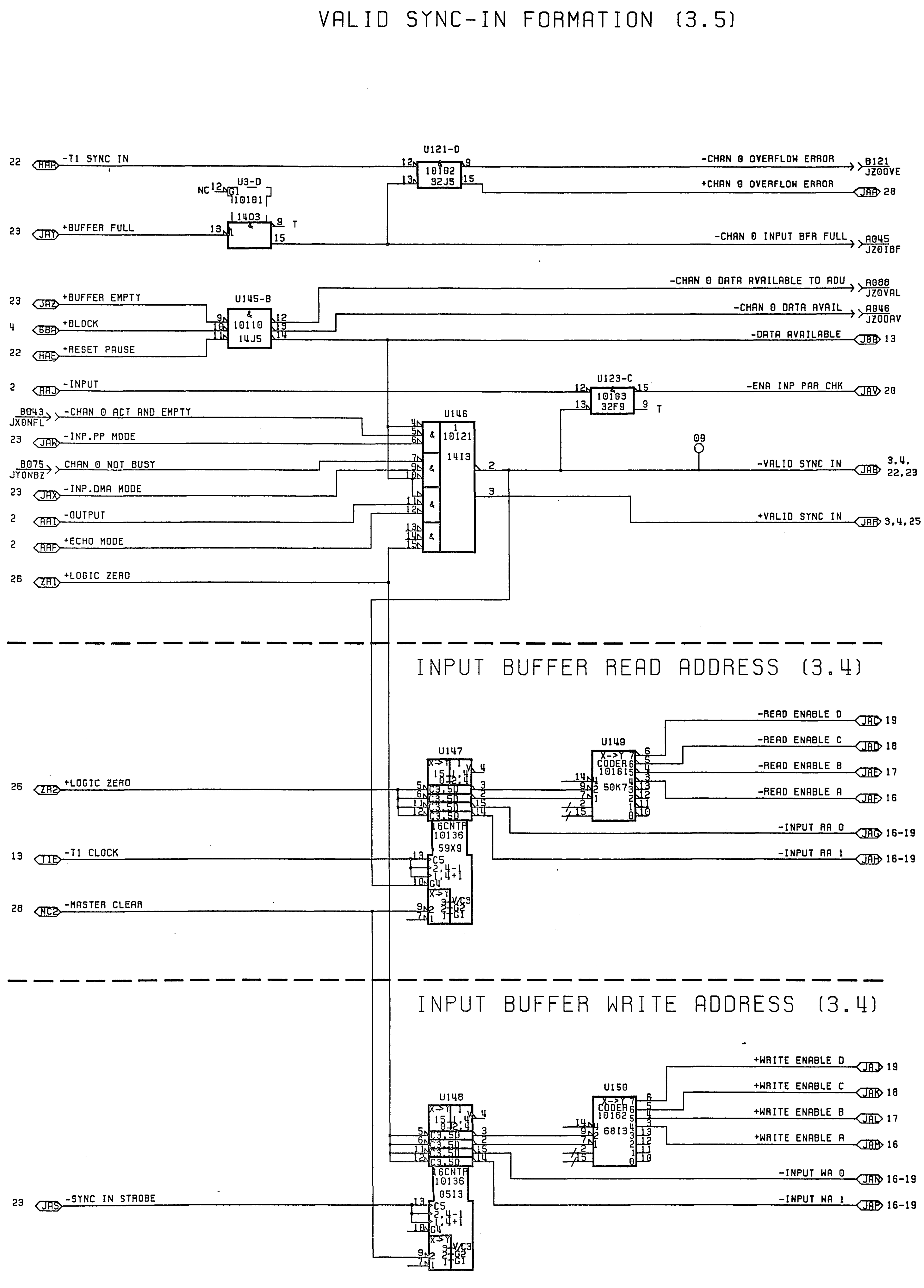
INPUT BUFFER WORD COUNTER (3.5)



SYNC IN ONE-SHOT (3.5)



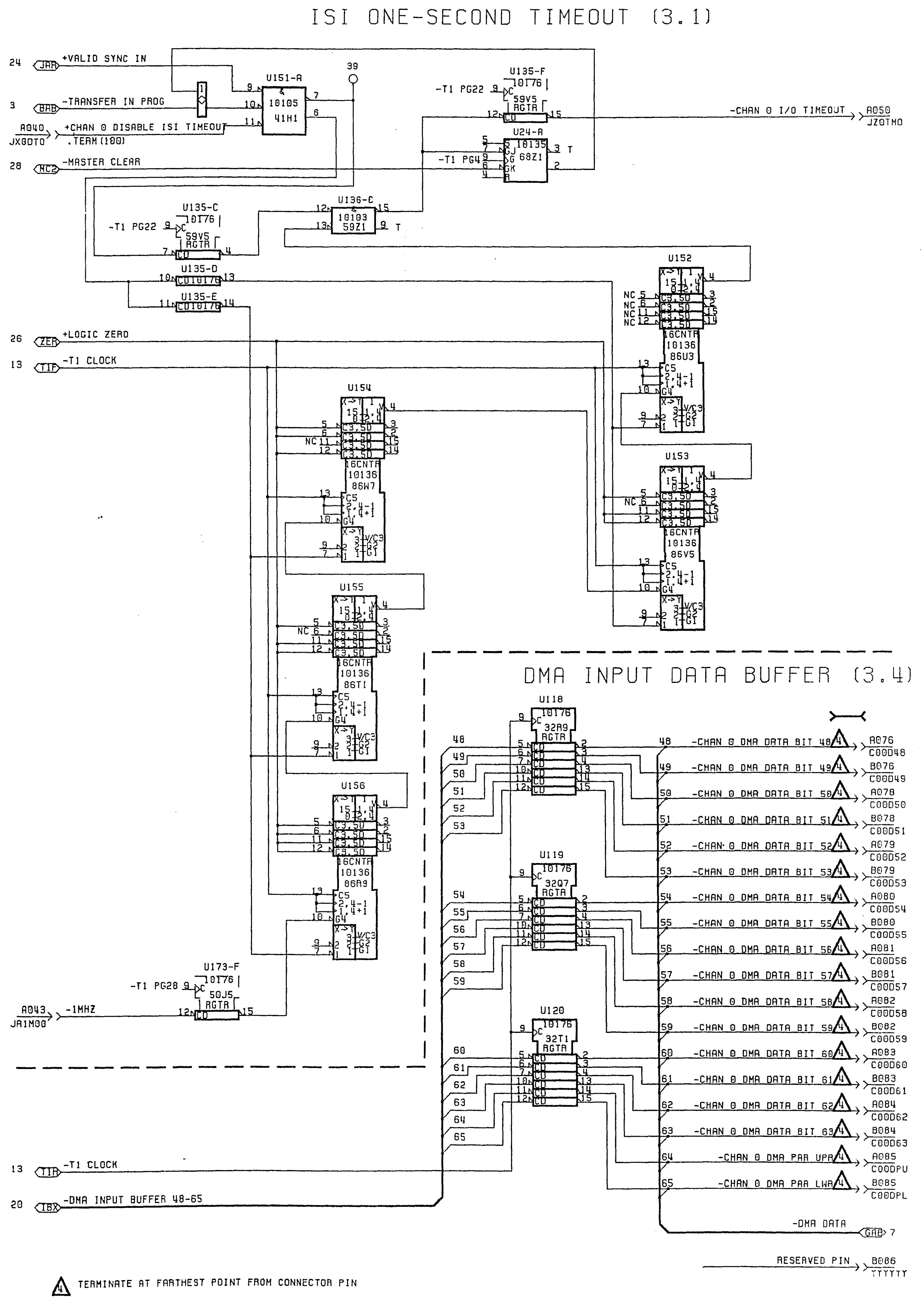
CONTROL DATA	CIO CHANNEL BOARD ISI I/F INPUT BUFFER WORD COUNTER SYNC IN ONE-SHOT TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		SHEET NO. 23	60462210	PAGE JZ-23	



CONTROL DATA

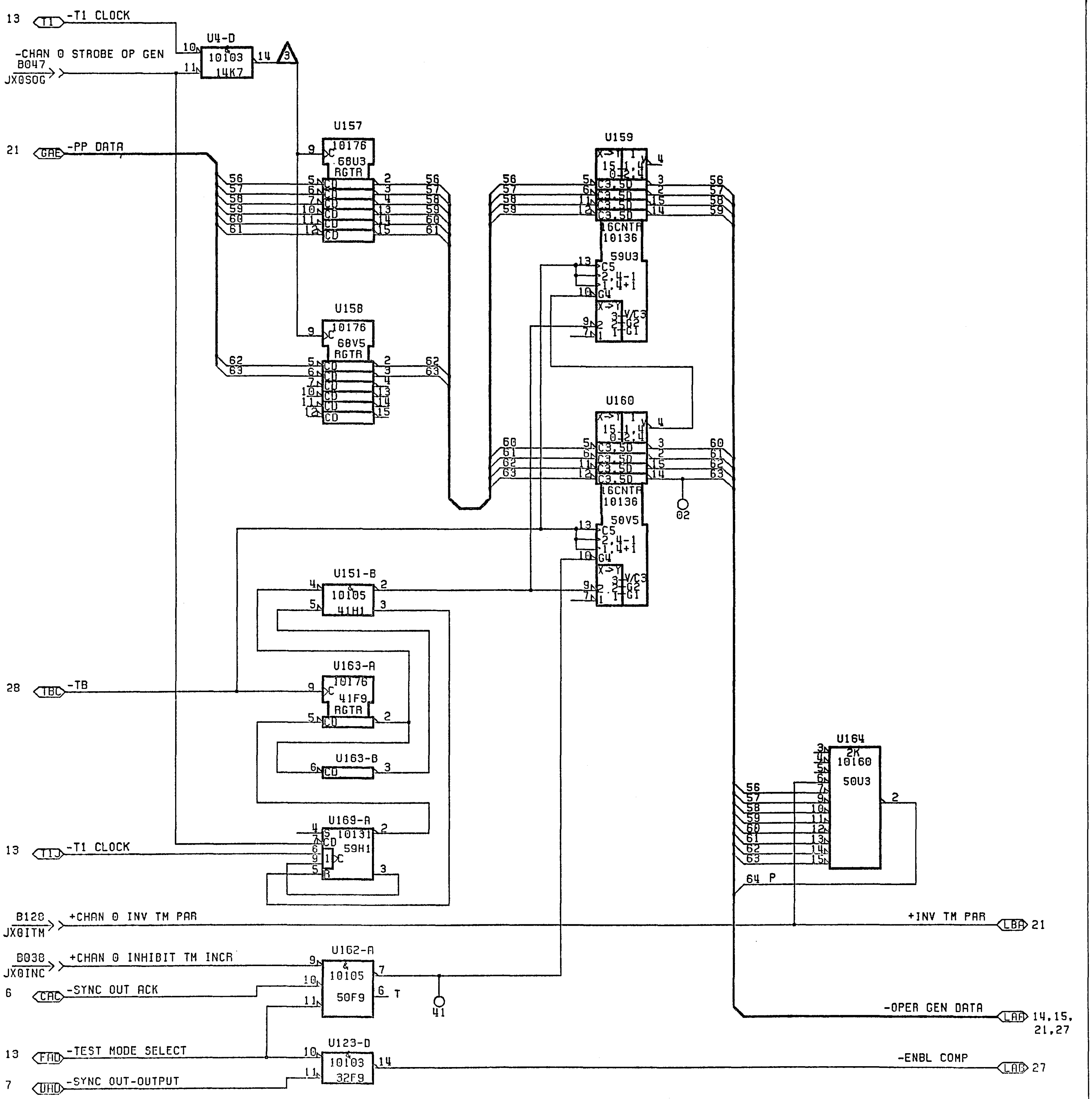
CIO CHANNEL BOARD ISI I/F
VALID SYNC IN FORMATION
INPUT BUFFER READ & WRITE ADRS
TYPE 1JZH

B	DWG NO. 22113019	DATE 03/07/86	REV A
SHEET NO. 24	60462210	PAGE JZ-24	

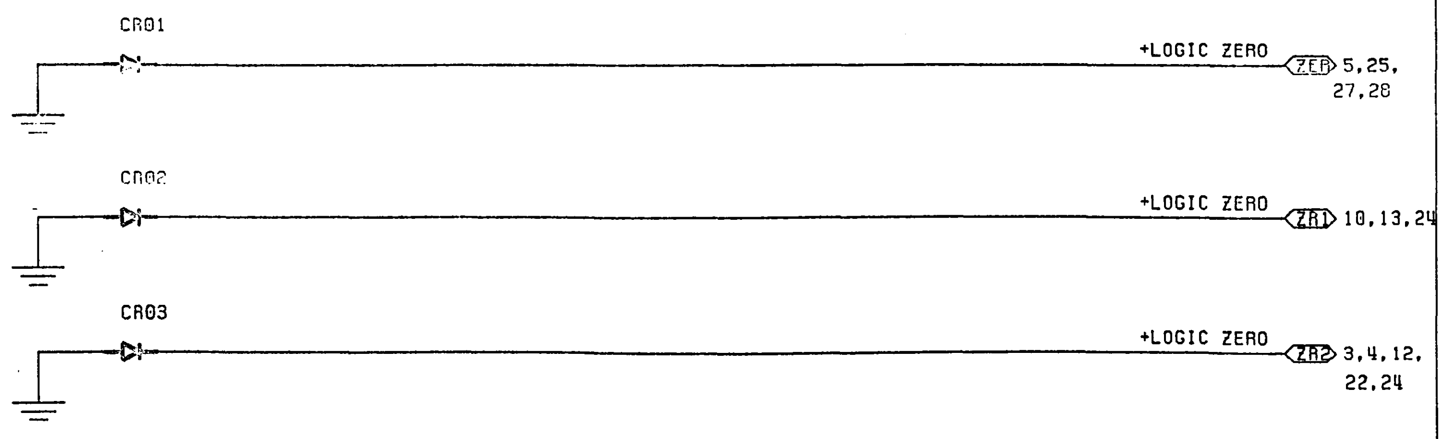

ISI ONE-SECOND TIMEOUT (3.1)
24 JAA +VALID SYNC IN
3 BAB -TRANSFER IN PROG
A040 JX0DTO +CHAN 0 DISABLE ISI TIMEOUT
.TERM (100)
28 NC2 -MASTER CLEAR
39
U151-A 10105 41H1
U135-F 10176 59V5 RGTR
-T1 PG22
-CHAN 0 I/O TIMEOUT A050 JZOTMO
U24-A 10135 68Z1
-T1 PG4
U135-C 10176 59V5 RGTR
-T1 PG22
U136-C 10103 59Z1
U135-D CD10176
U135-E CD10176
U152 16CNTR 10136 86U3
NC
26 ZER +LOGIC ZERO
13 T1F -T1 CLOCK
U154 16CNTR 10136 86W7
U153 16CNTR 10136 86V5
U155 16CNTR 10136 86T1
U156 16CNTR 10136 86R9
U173-F 10176 50J5 RGTR
-T1 PG28
A043 JA1M00 -1MHZ
DMA INPUT DATA BUFFER (3.4)
U118 10176 32R9 RGTR
U119 10176 32Q7 RGTR
U120 10176 32T1 RGTR
48 -CHAN 0 DMA DATA BIT 48 A076 C00D48
49 -CHAN 0 DMA DATA BIT 49 B076 C00D49
50 -CHAN 0 DMA DATA BIT 50 A078 C00D50
51 -CHAN 0 DMA DATA BIT 51 B078 C00D51
52 -CHAN 0 DMA DATA BIT 52 A079 C00D52
53 -CHAN 0 DMA DATA BIT 53 B079 C00D53
54 -CHAN 0 DMA DATA BIT 54 A080 C00D54
55 -CHAN 0 DMA DATA BIT 55 B080 C00D55
56 -CHAN 0 DMA DATA BIT 56 A081 C00D56
57 -CHAN 0 DMA DATA BIT 57 B081 C00D57
58 -CHAN 0 DMA DATA BIT 58 A082 C00D58
59 -CHAN 0 DMA DATA BIT 59 B082 C00D59
60 -CHAN 0 DMA DATA BIT 60 A083 C00D60
61 -CHAN 0 DMA DATA BIT 61 B083 C00D61
62 -CHAN 0 DMA DATA BIT 62 A084 C00D62
63 -CHAN 0 DMA DATA BIT 63 B084 C00D63
64 -CHAN 0 DMA PAR UPR A085 C00DPU
65 -CHAN 0 DMA PAR LWR B085 C00DPL
13 T1F -T1 CLOCK
20 IBX -DMA INPUT BUFFER 48-65
-DMA DATA GAB 7
RESERVED PIN B086 YYYYYY
4 TERMINATE AT FARTHEST POINT FROM CONNECTOR PIN

CONTROL DATA	CIO CHANNEL BOARD ISI I/F DMA INPUT DATA BUFFER ISI ONE SECOND TIMEOUT TYPE 1JZH	B	DWG NO. 22113019	DATE 01/27/87	REV B
		SHEET NO. 25	60462210	PAGE JZ-25	

OPERAND GENERATOR (3.6)



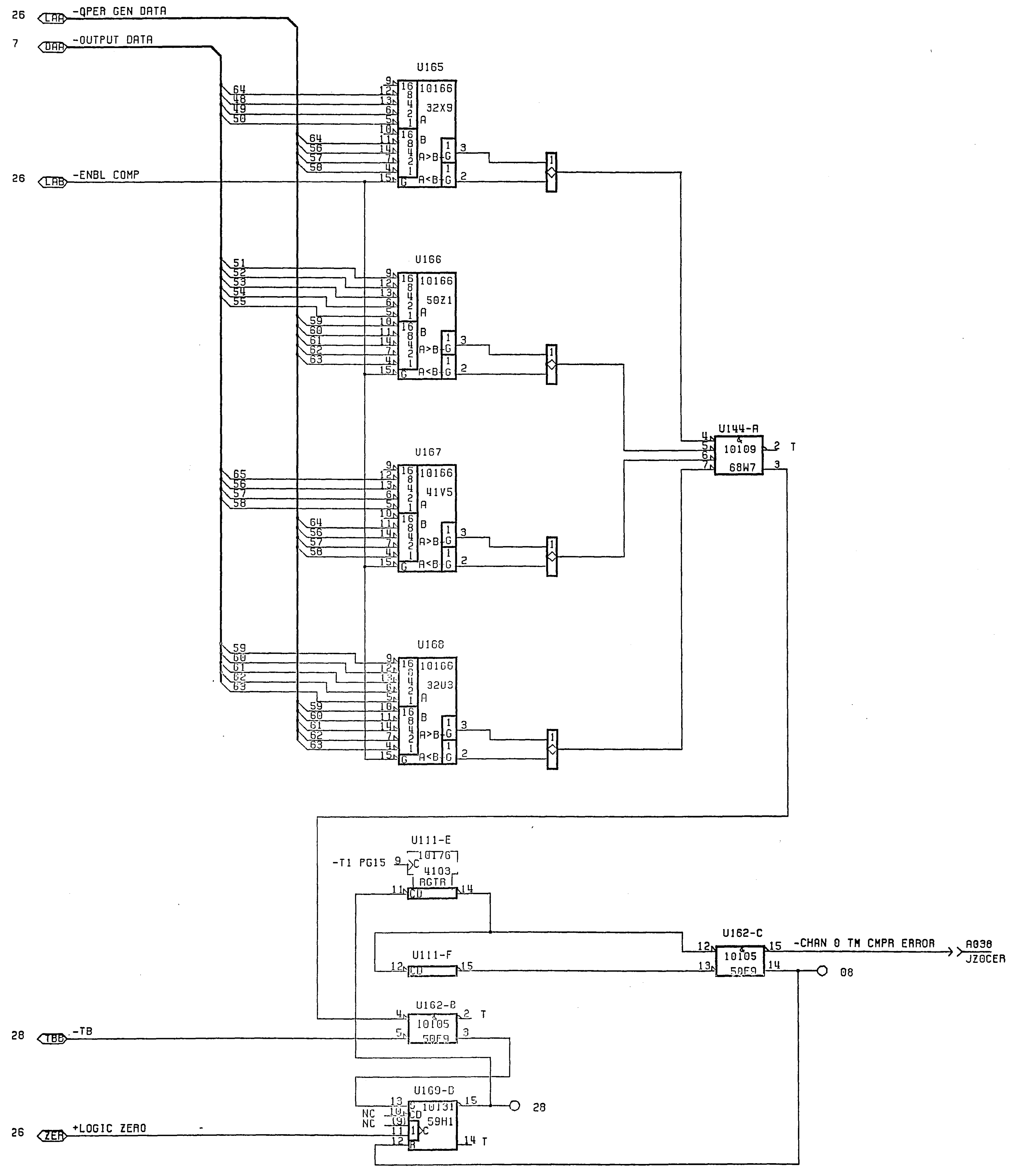
LOGIC ZERO SOURCE



3 12 INCH MAXIMUM LENGTH

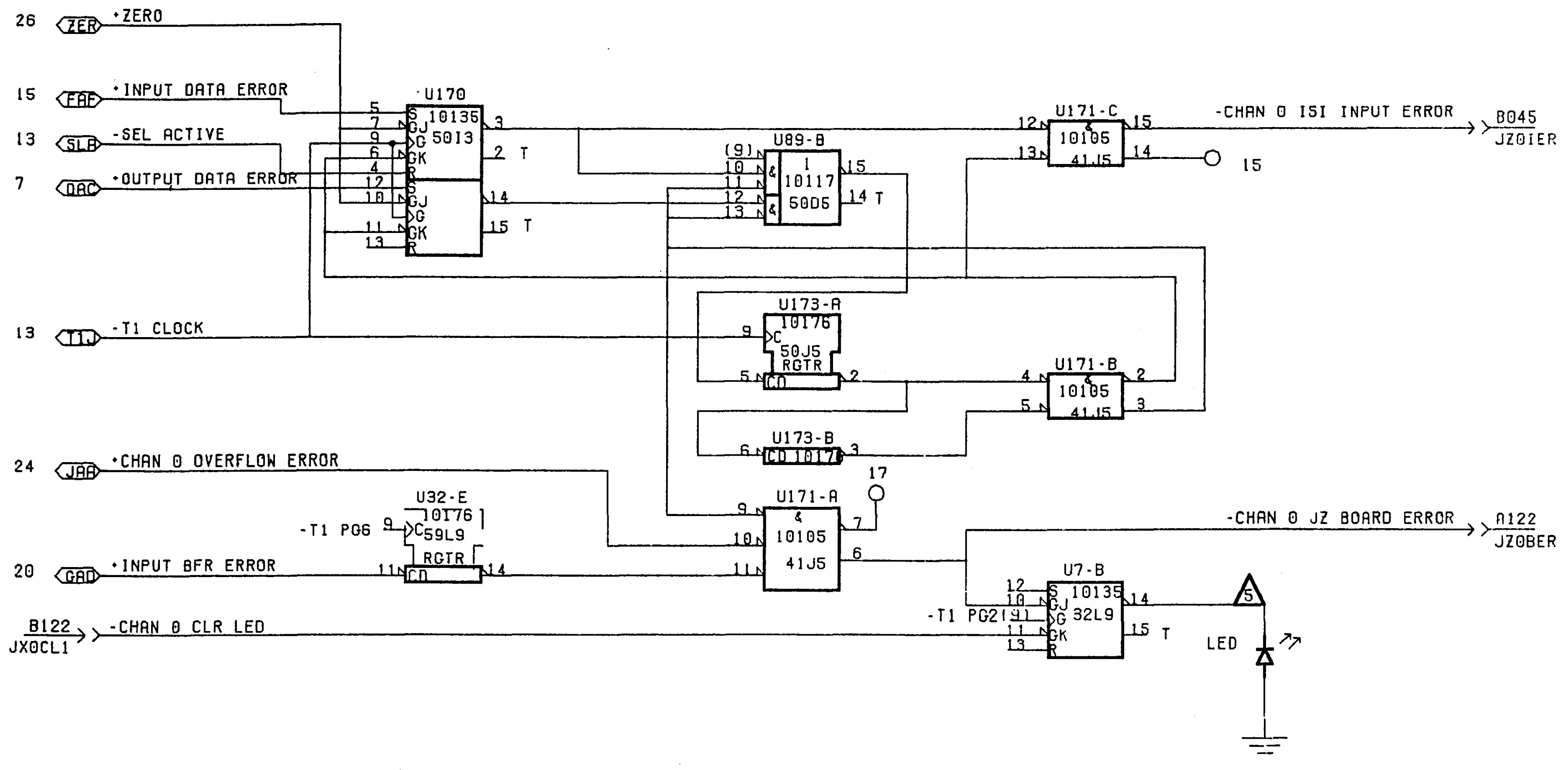
CONTROL DATA	CIO CHANNEL BOARD ISI I/F OPERAND GENERATOR LOGIC ZERO SOURCE TYPE 1JZH	B	DWG NO. 22113019	DATE 03/07/86	REV A
		N	SHEET NO. 26	60462210	PAGE JZ-26

COMPARE NETWORK (3.6)

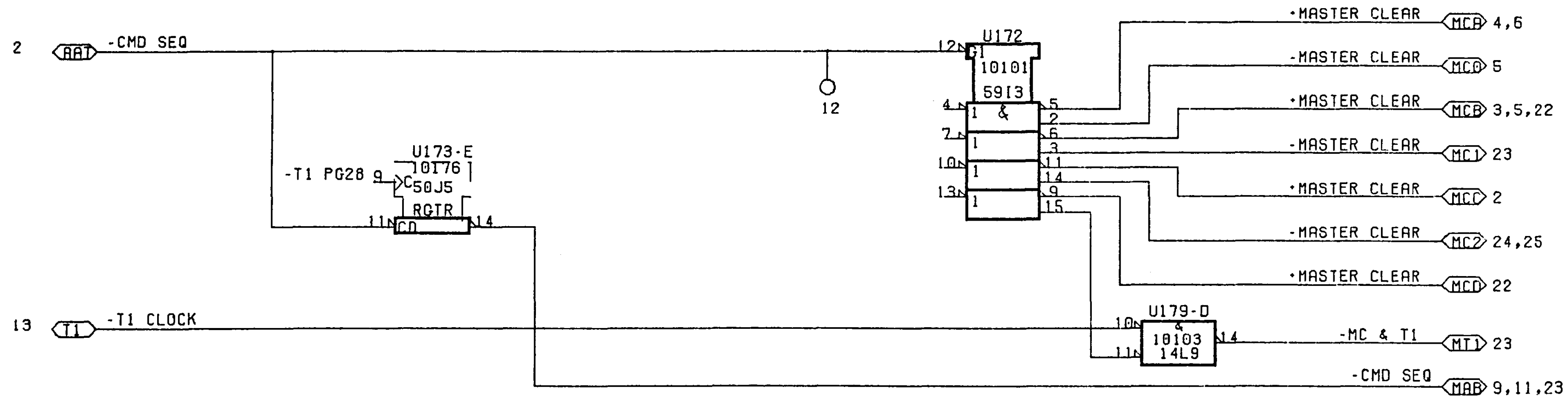


CONTROL DATA	CIO CHANNEL BOARD ISI I/F COMPARE NETWORK	B	DWG NO. 22113019	DATE 03/07/86	REV A
	TYPE 1JZH	N	SHEET NO. 27	60462210	PAGE JZ-27

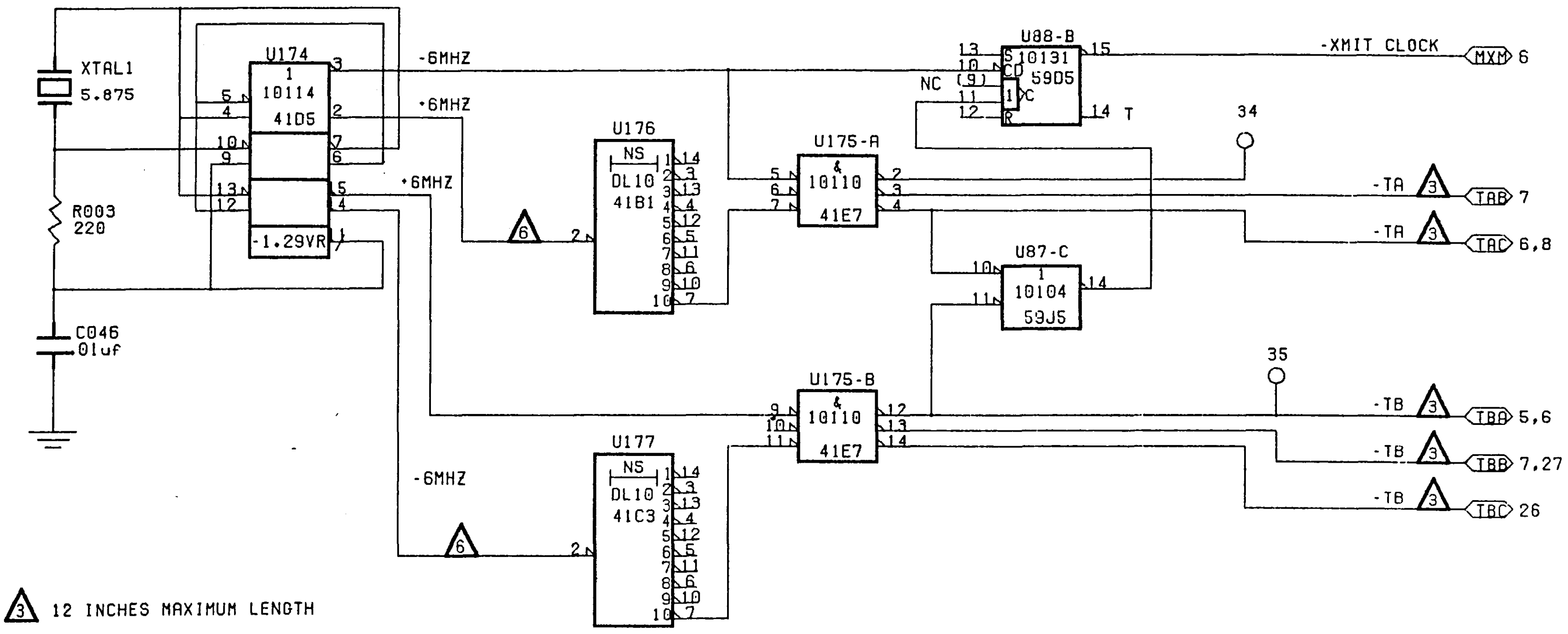
BOARD ERROR (3.2)



MASTER CLEAR FANOUT (3.5)



6 MHZ CLOCK GENERATOR (3.0)



3 12 INCHES MAXIMUM LENGTH

5 TERMINATE

6 NOT TERMINATED

CONTROL DATA	CIO CHANNEL BOARD ISI I/F BOARD ERROR ,MASTER CLEAR FANOUT 6 MHZ CLOCK GENERATOR TYPE 1JZH	B	DWG NO. 22113019	DATE 06/15/88	REV C
		N	SHEET NO. 28	60462210	PAGE JZ-28

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	02	-PORT B SEL	27	22	+PAUSE FLAG
02	26	-OPER GEN BIT 63	28	27	-TM CMP ERR "TB"
03	02	-INTERLOCK	29	15	-DATA IN BIT 63
04	02	-ECHO MODE	30	02	+CMD SEQ
05	06	-RESYNC FULL	31	,	,
06	08	-OUTPUT	32	,	,
07	04	+INCR PAUSE CNTR	33	02	+DMA MODE
08	27	+TM CMP ERR "T1"	34	28	-TA
09	24	-VALID SYNC IN	35	28	-TB
10	04	+DECR PAUSE CNTR	36	07	-OUT DATA MUX BIT 63
11	13	-T1 CLOCK	37	20	-DATA FANIN BIT 63
12	28	-CMD SEQ	38	08	-OUTPUT BFR BIT 63
13	,	,	39	25	-ENBL 1 SEC TIMEOUT
14	02	-PP MODE	40	13	-RAW PAUSE
15	28	+CHAN 0 ISI IN ERR	41	26	-INC OP GEN
16	05	-RESYNC A FULL	42	13	+SYNC IN
17	28	+JZ BOARD ERROR	43	06	-SYNC OUT
18	23	+SYNC IN STROBE	44	03	-REQ CNTR BIT 0
19	05	-RESYNC B FULL	45	04	-PAUSE CNTR BIT 0
20	05	-RESYNC C FULL	46	06	+BUFFER FULL
21	05	-RESYNC D FULL	47	22	-NON INT PAUSE
22	02	-TEST MODE	48	03	+INCR REQ CNTR
23	22	-T1 SYNC IN	49	22	-SYNC IN RESYNC TOG
24	13	-SELECT HOLD	50	03	+DEC REQ CNTR
25	02	+VALID SYNC OUT	51	22	-SYNC IN RESYNC F/F
26	04	+BUSY			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065, B065,A066,B066,A077,B077,A097,B097,A107,B107, A117,B117,A037,A038,B037,B038,B128
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070
TERM	NONE
UNUSED	A003,B003,A004,B004,B037,A041,A047,A074,B086, A090,B090,B091,B127,A128

CONTROL DATA

CIO CHANNEL BOARD ISI I/F
TESTPOINTS & SIGNAL NAMES
AND CONNECTOR PINS
TYPE 1JZH

	DWG NO.	DATE	REV
B	22113819	03/07/86	A
SHEET NO. 29	60462210	PAGE JZ-29	

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1KAH TERMINATOR BOARD

REVISION HISTORY B/M 41654901			
DATE	REV	DESCRIPTION OF CHANGE	INIT
05/15/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	LHJ
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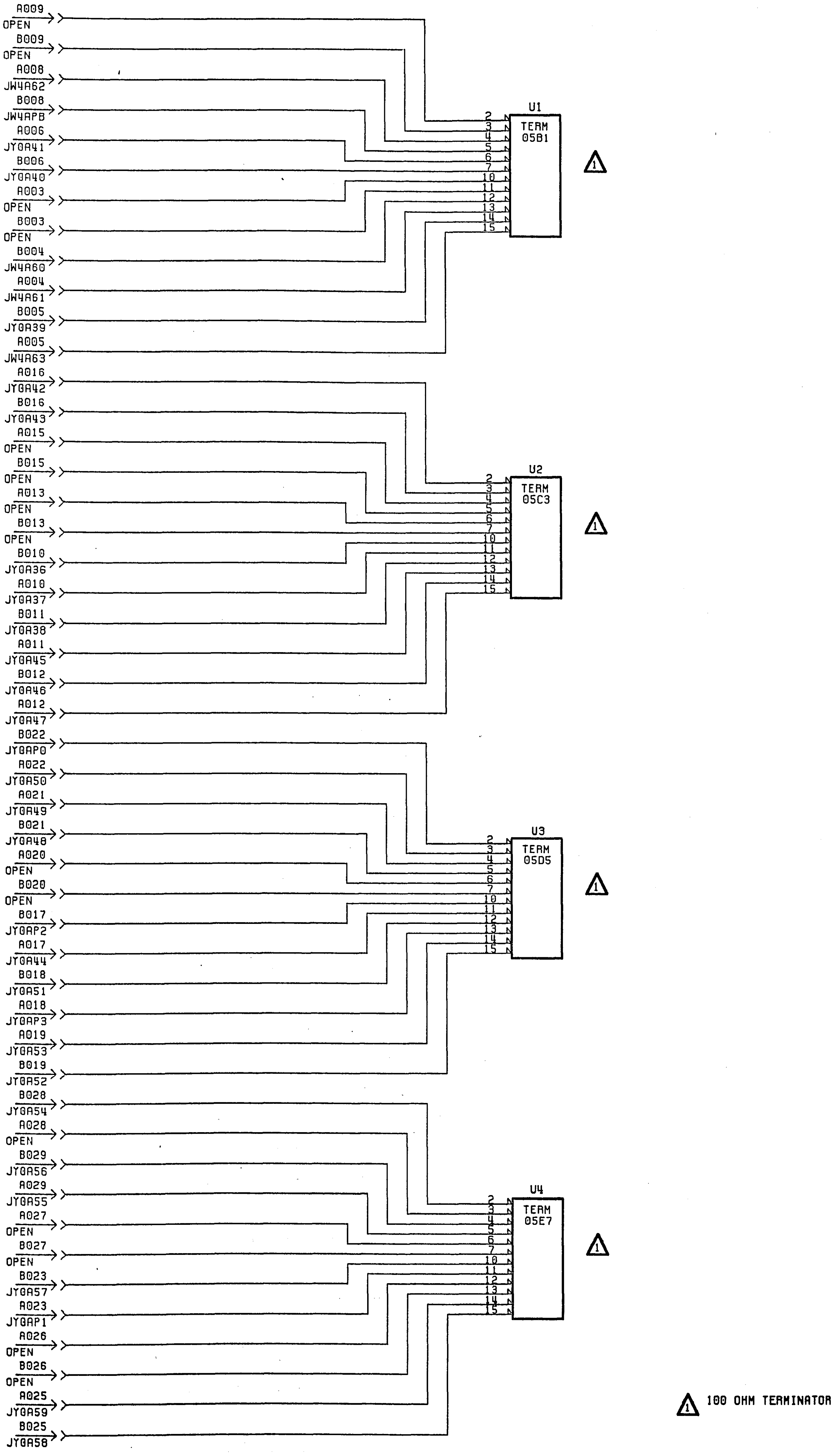
DWN	L H JOHNSON	05/15/86
CHKD	LH Johnson	5/15/86
ENG		5/15/86
PUBS		5/15/86
APP		5/15/86

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D08,C08

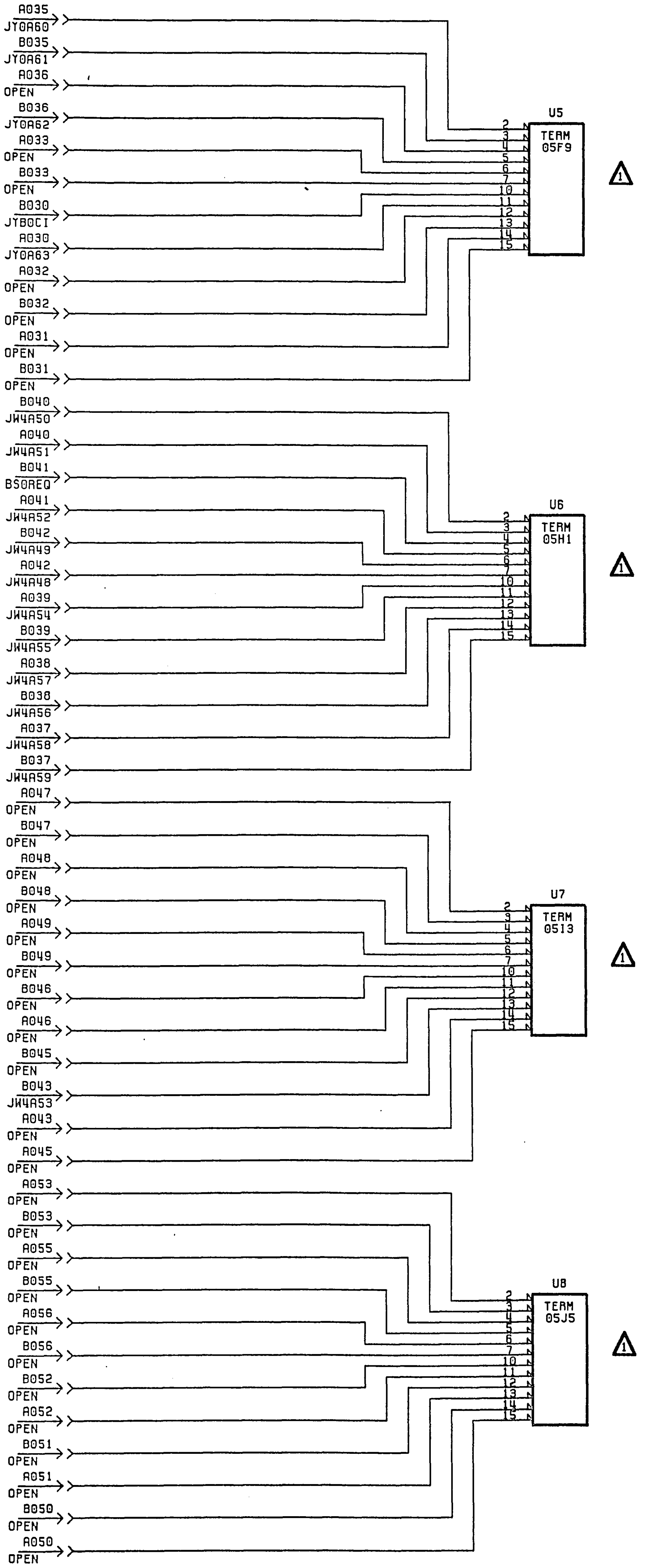
CONTROL DATA	TERMINATOR BOARD TYPE 1KAH	B	DWG NO. 22127690	DATE 05/15/86	REV A
		SHEET NO. 1	60462210	PAGE KA-01	

TERMINATORS



CONTROL DATA	TERMINATOR BOARD , . TYPE 1KAH	B	DWG NO. 22127690	DATE 05/15/86	REV A
	N	SHEET NO. 2	60462210	PAGE KA-02	

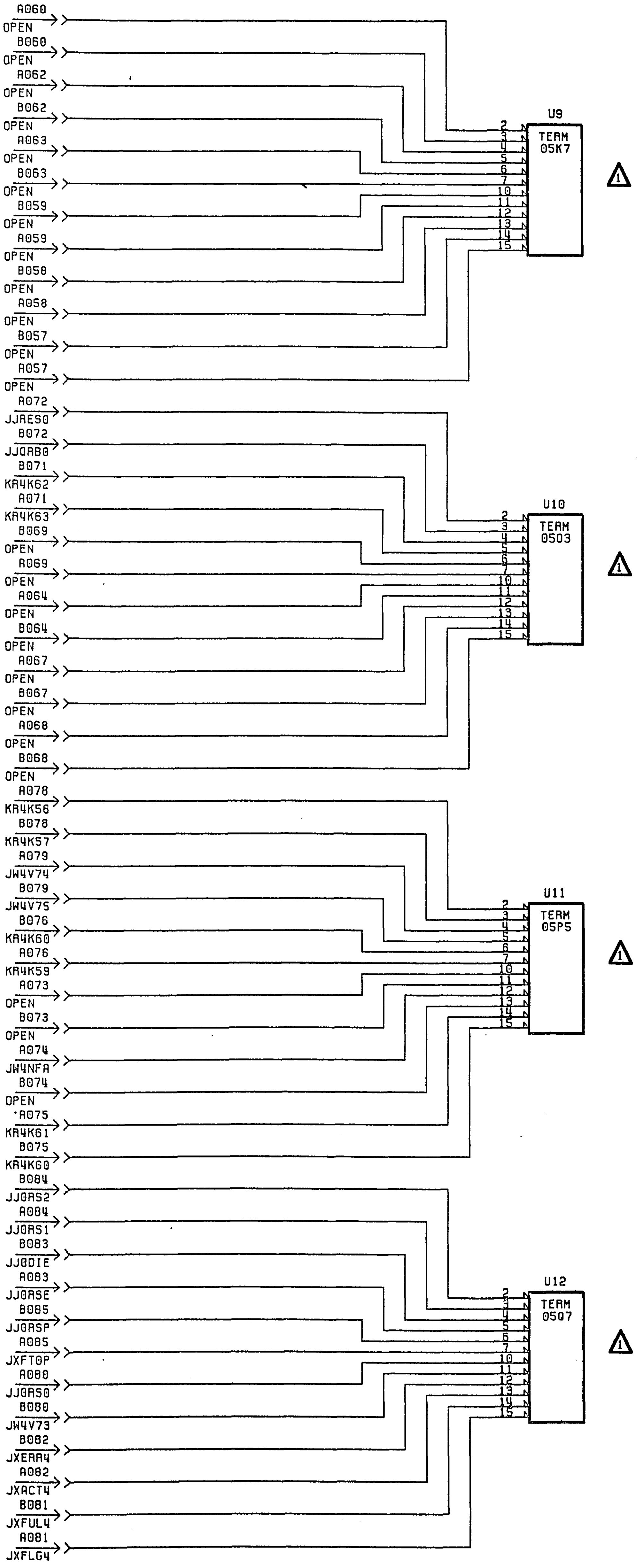
TERMINATORS



△1 100 OHM TERMINATOR

CONTROL DATA
TERMINATOR BOARD
.
.
TYPE 1KAH
B
DWG NO. 22127690
DATE 05/15/86
REV A
SHEET NO. 3
60462210
PAGE KA-09

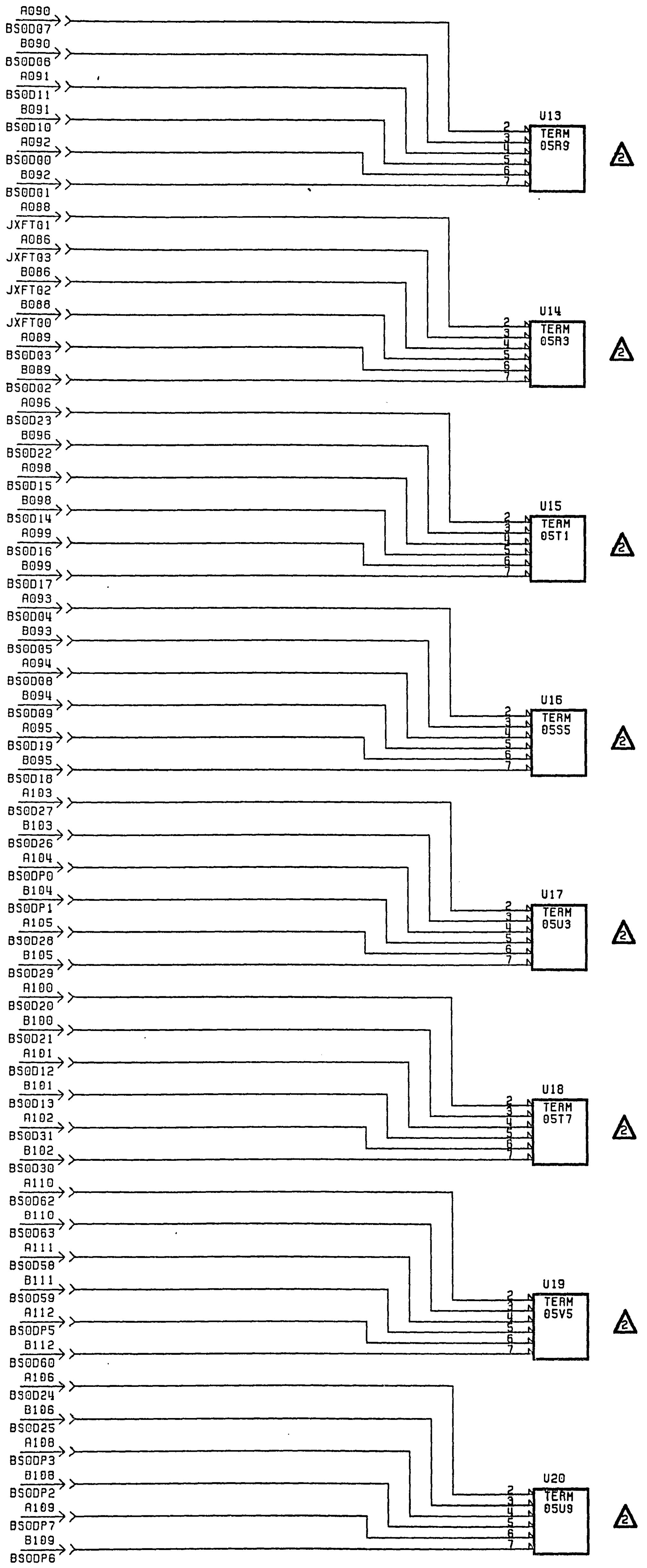
TERMINATORS



△1 100 OHM TERMINATOR

CONTROL DATA	TERMINATOR BOARD TYPE 1KAH	B	DWG NO. 22127690	DATE 05/15/86	REV A
		SHEET NO. 4	60462210	PAGE KA-04	

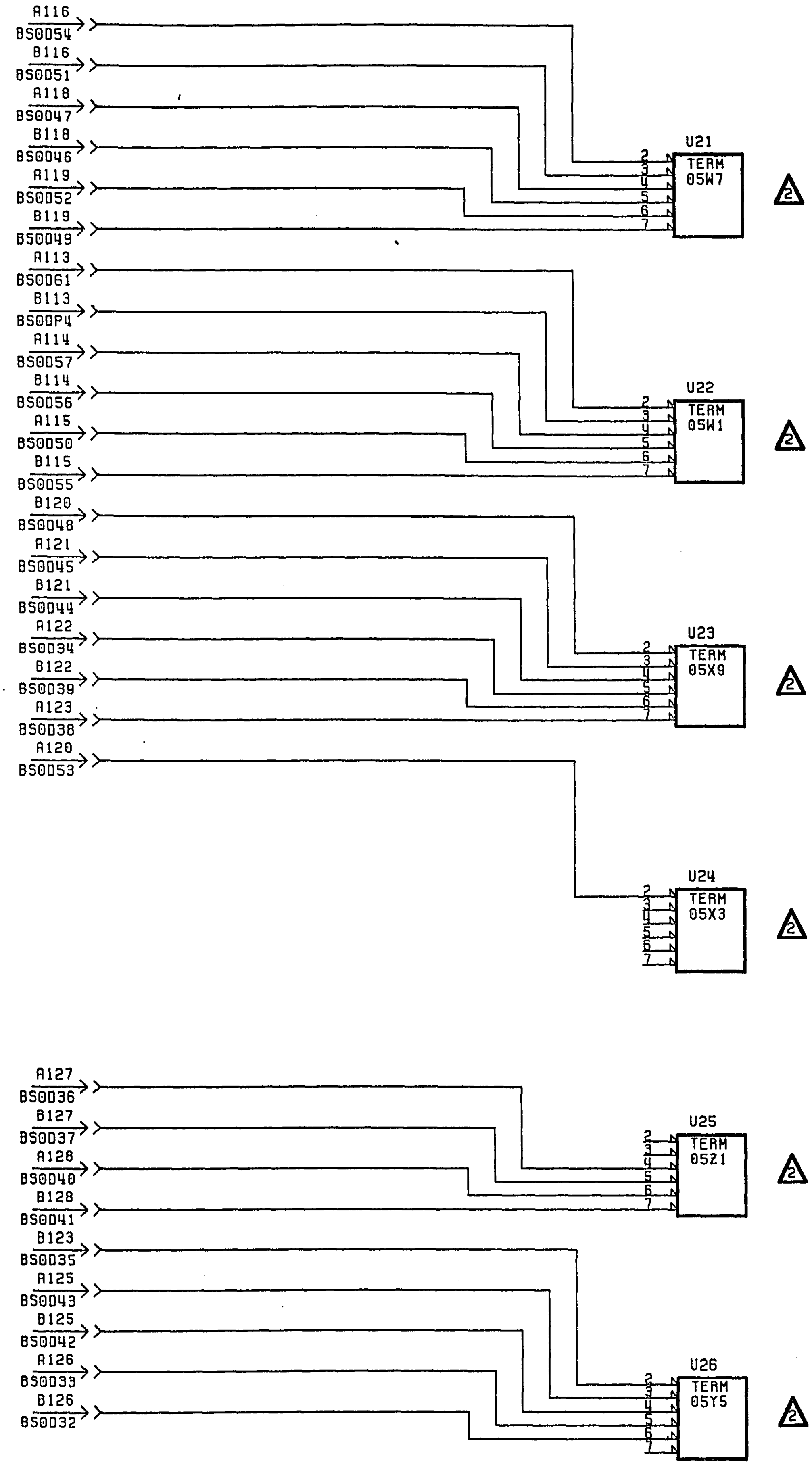
TERMINATORS



2 120 OHM TERMINATOR

CONTROL DATA	TERMINATOR BOARD , , TYPE 1KAH	8	DWG NO. 22127690	DATE 05/15/86	REV A
		SHEET NO. 5	60462210	PAGE KA-05	

TERMINATORS



△2 120 OHM TERMINATOR

CONTROL DATA
TERMINATOR BOARD
.
.
TYPE 1KAH
B
DWG NO. 22127690
DATE 05/15/86
REV A
SHEET NO. 6
60462210
PAGE KA-06

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1KAH TERMINATOR BOARD

REVISION HISTORY B/M 41654900			
DATE	REV	DESCRIPTION OF CHANGE	INIT
11/01/85	A	CLASS A RELEASE OF LOGIC DIAGRAMS.	LHJ
06/10/86	B	ECO 47740 PAGES 5 & 6.	LHJ
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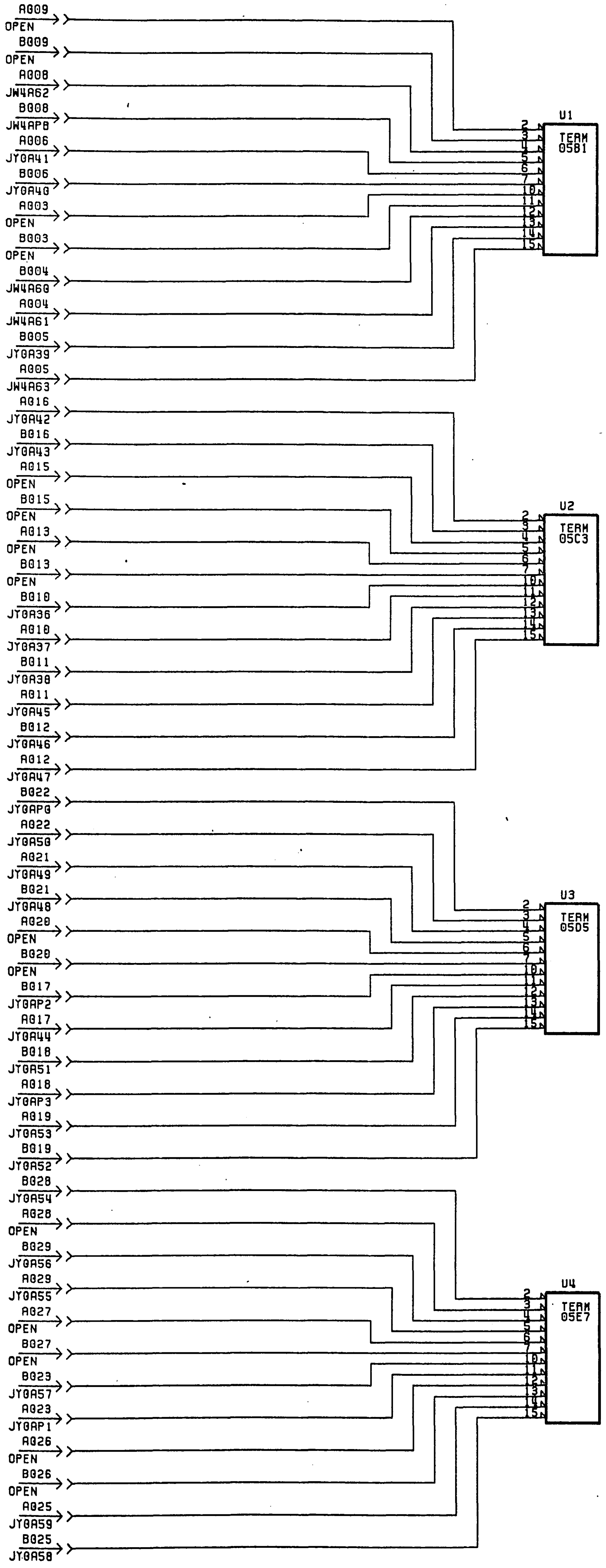
DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	D R FORD	12/04/85
PUBS	R K BONDE	12/04/85
APP	D R FORD	12/04/85

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D08,C08

CONTROL DATA	TERMINATOR BOARD TYPE 1KAH N	B	DWG NO. 22105810	DATE 06/10/86	REV B
		SHEET NO. 1	60462210	PAGE KA-01	

TERMINATORS



CONTROL DATA

TERMINATOR BOARD

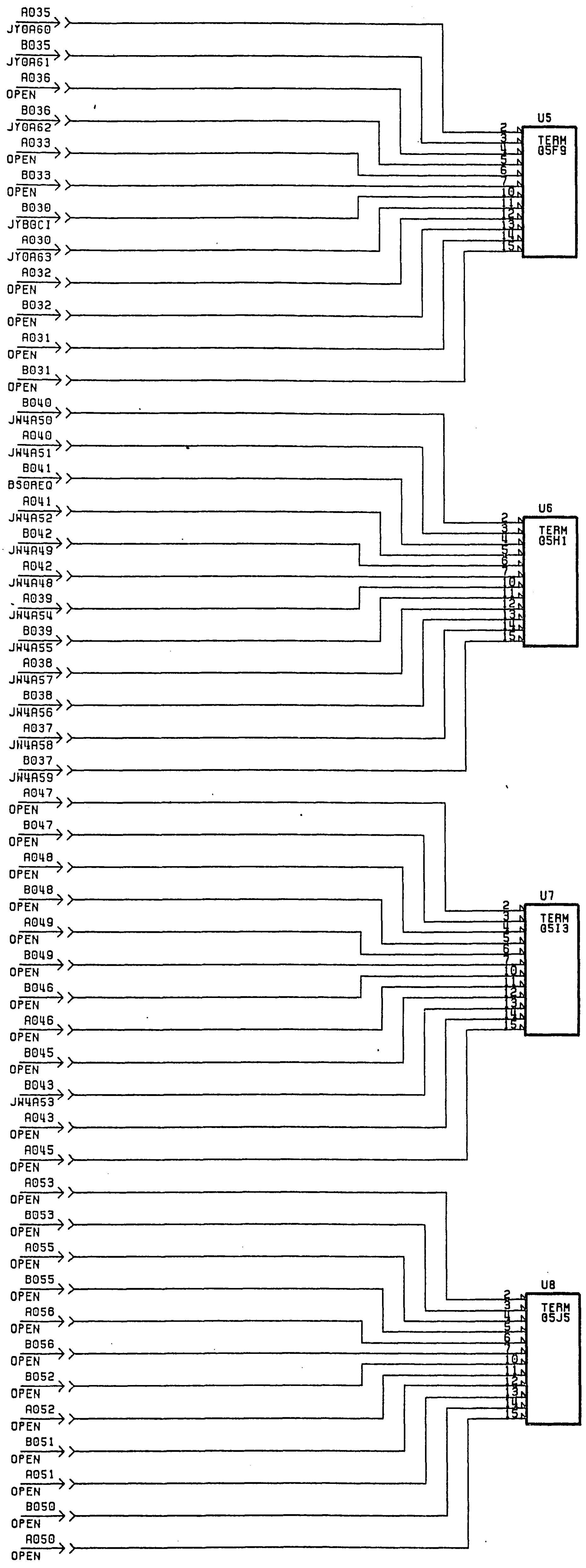
.

.

TYPE 1KAH

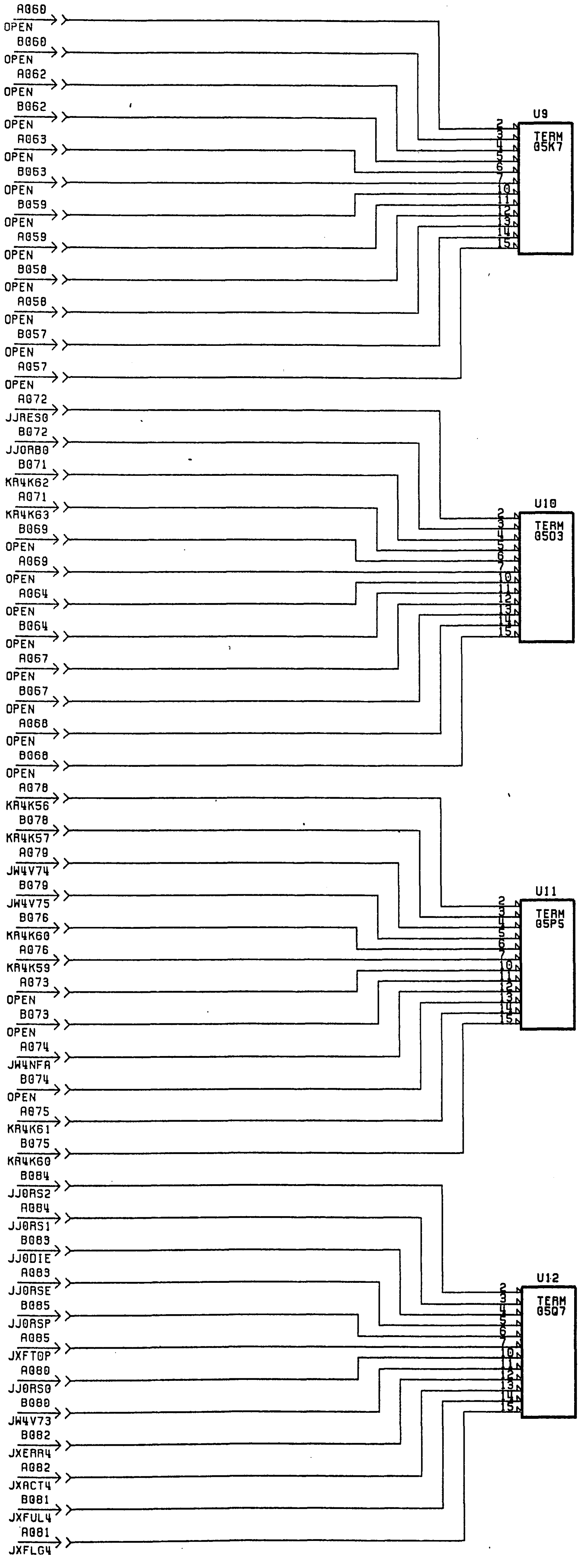
B	DWG NO. 22105610		DATE 11/01/85	REV A
N	SHEET NO. 2	60462210	PAGE KA-02	

TERMINATORS



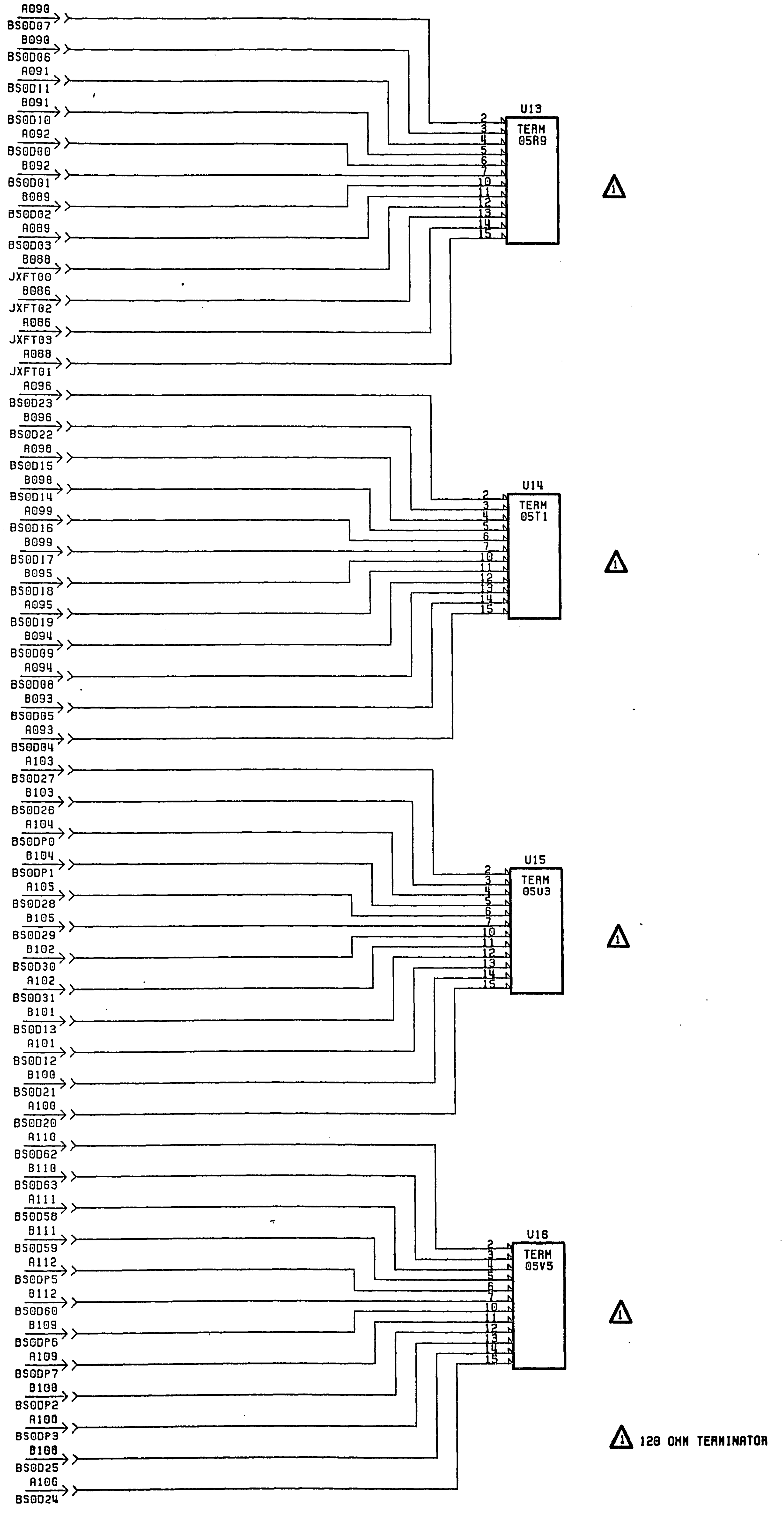
CONTROL DATA
TERMINATOR BOARD
TYPE 1KAH
B
DWG NO. 22105610
DATE 11/01/85
REV A
N SHEET NO. 3 60462210
PAGE KA-03

TERMINATORS



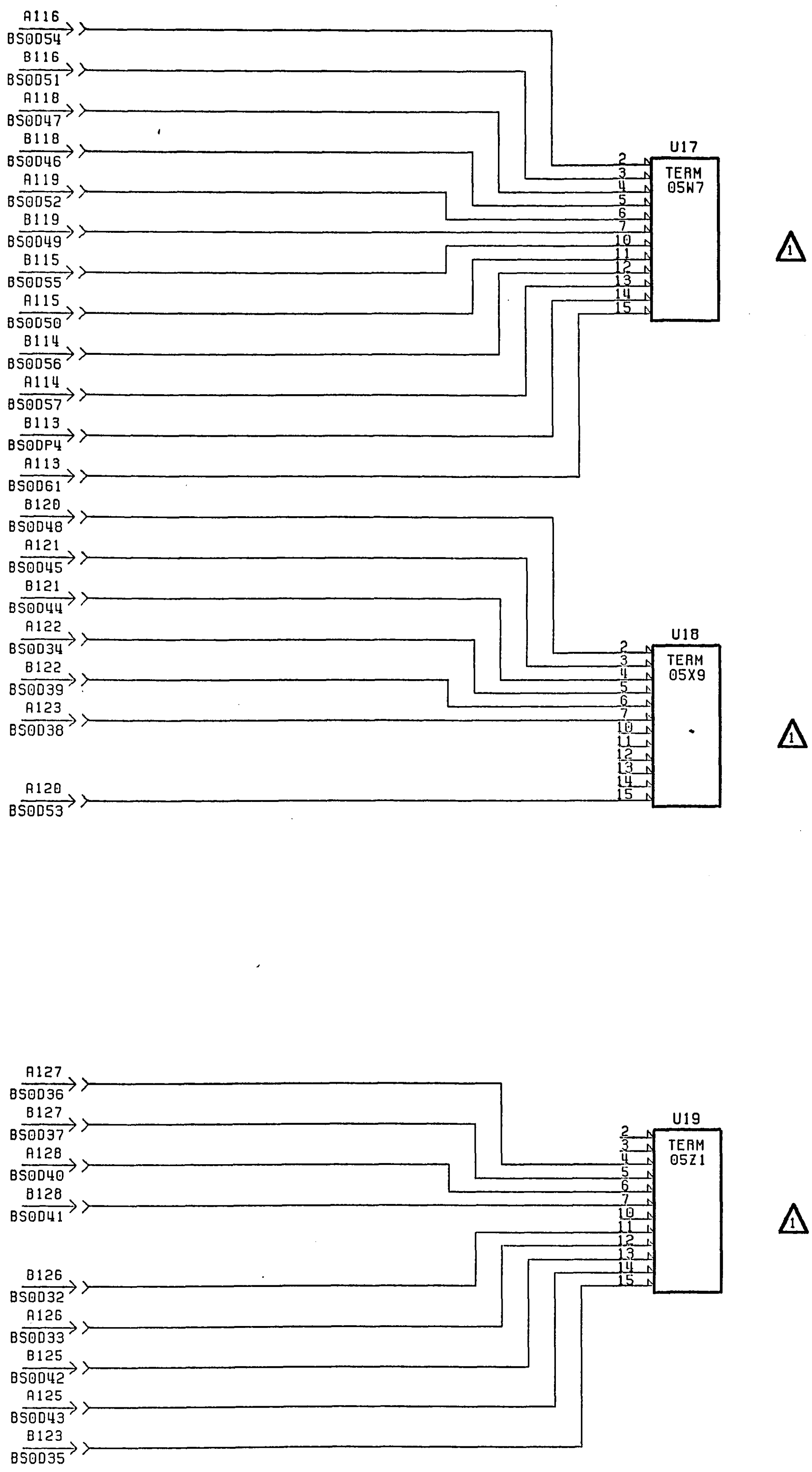
CONTROL DATA	TERMINATOR BOARD . . TYPE 1KAH	B	DWG NO. 22105810	DATE 11/01/85	REV A
	N	SHEET NO. 4	60462210	PAGE KA-04	

TERMINATORS



CONTROL DATA	TERMINATOR BOARD , , TYPE 1KAH	B	DWG NO. 22105810	DATE 06/10/88	REV B
		SHEET NO. 5	60462210	PAGE KA-05	

TERMINATORS



△1 120 OHM TERMINATOR

CONTROL DATA	TERMINATOR BOARD TYPE 1KAH	B	DWG NO. 22105610	DATE 06/10/86	REV B
		SHEET NO. 6	60462210	PAGE KA-06	

1KXH 170 DMA CHANNEL ADAPTER BAS I/F

REVISION HISTORY B/M 41655100			
DATE	REV	DESCRIPTION OF CHANGE	INIT
10/15/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	DAZ
10/19/87	B	ECO #48862 PAGES 5,8,9,13 & 15	SLP
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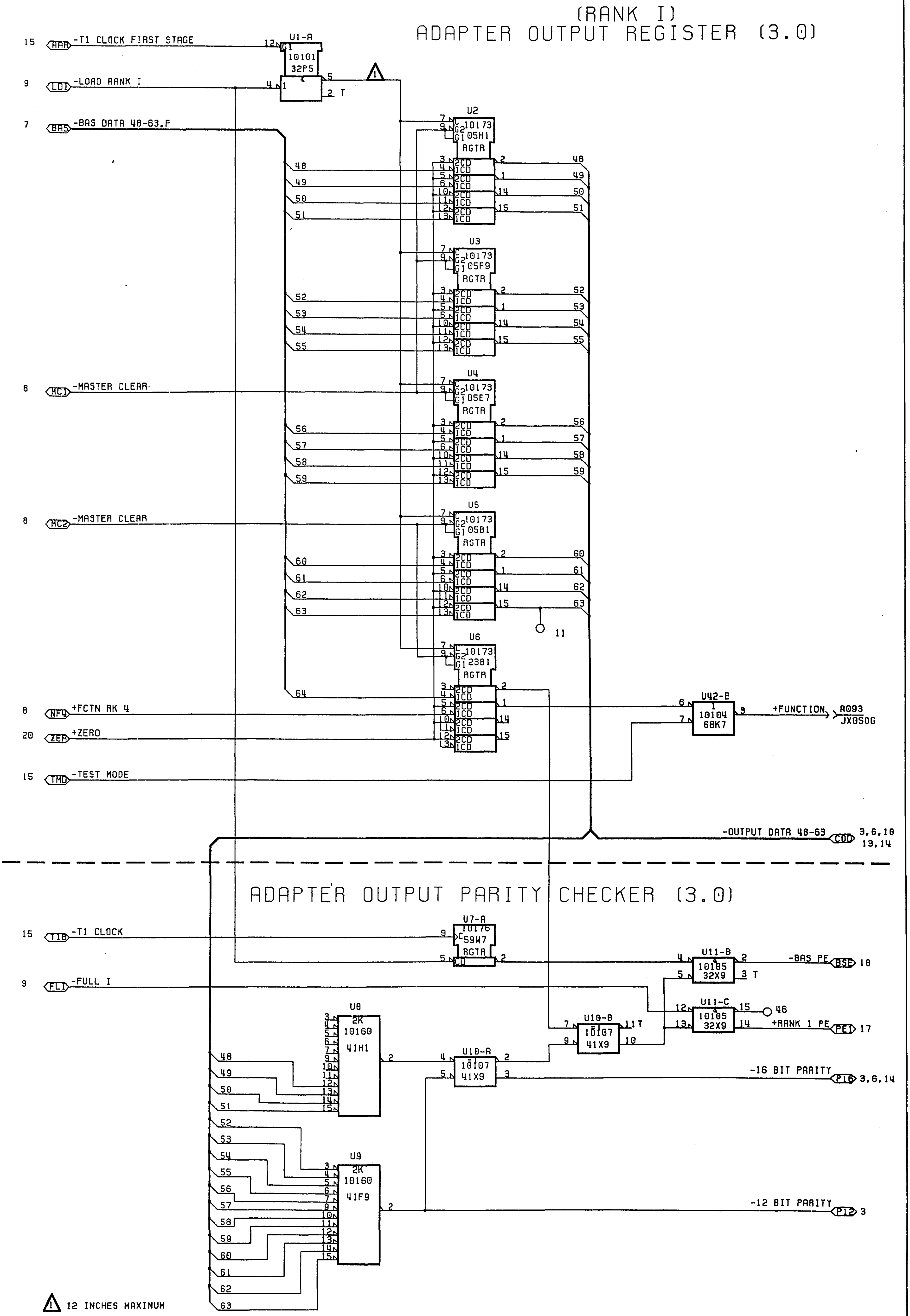
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D11,D14,D17,D20,D23
C11,C14,C17,C20,C23

DWN	L H JOHNSON	08/29/86
CHKD	S L PJESCICH	10/22/86
ENG	D A ZAHALAN	10/22/86
PUBS	N J ANDERSON	10/23/86
APP	D A ZAHALAN	10/22/86

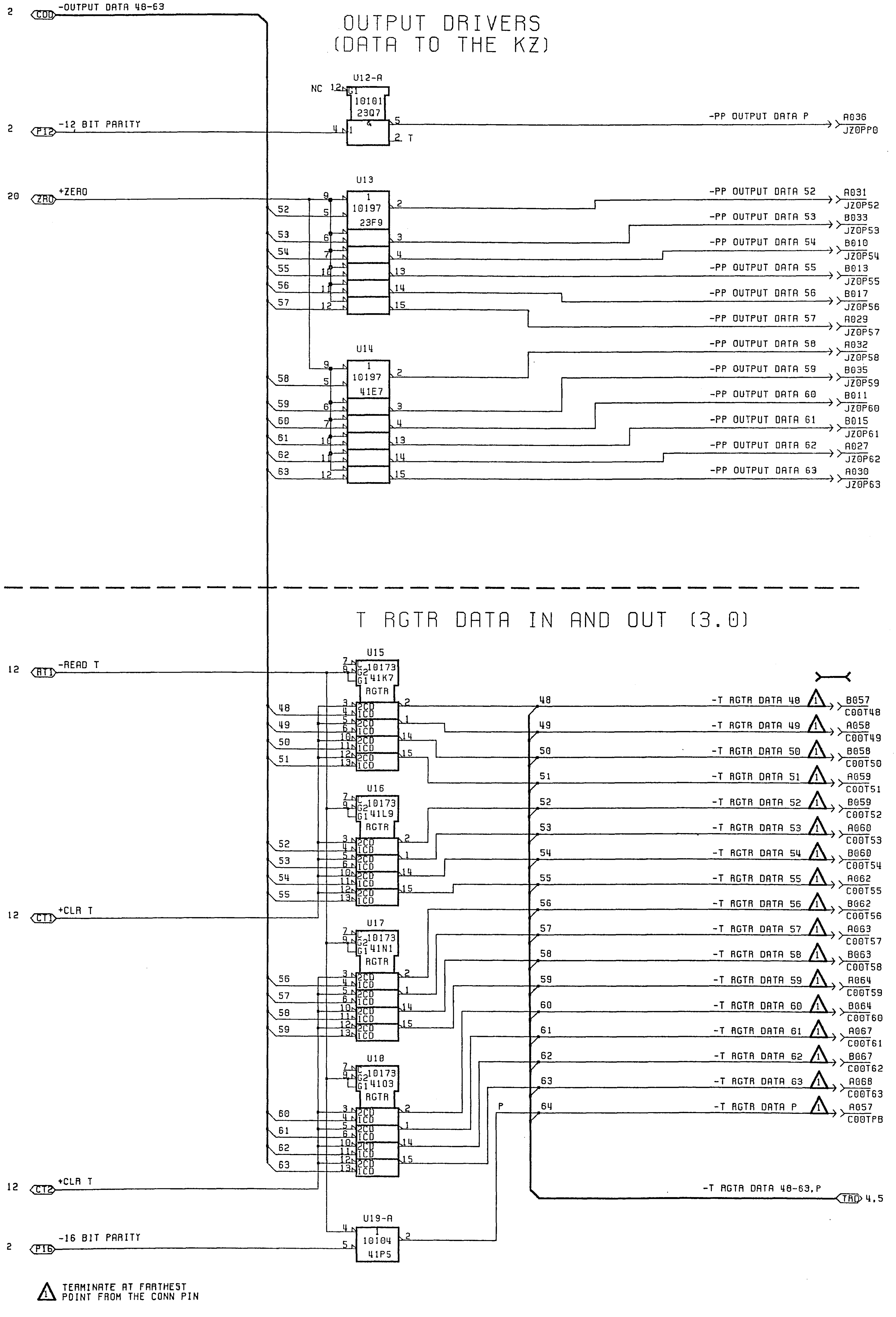
CONTROL DATA	REVISION HISTORY 170 DMA CHAN ADAPTER BAS I/F TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV B
		N SHEET NO. 1	60462210	PAGE KX-01	



CONTROL DATA

170 DMA CHAN ADAPTER BAS I/F
ADAPTER OUTPUT REGISTER
AND OUTPUT PARITY CHECKER
TYPE 1KXH

B	DWG NO. 22132519	DATE 10/15/86	REV A
SHEET NO. 2	60462210	PAGE KX-02	

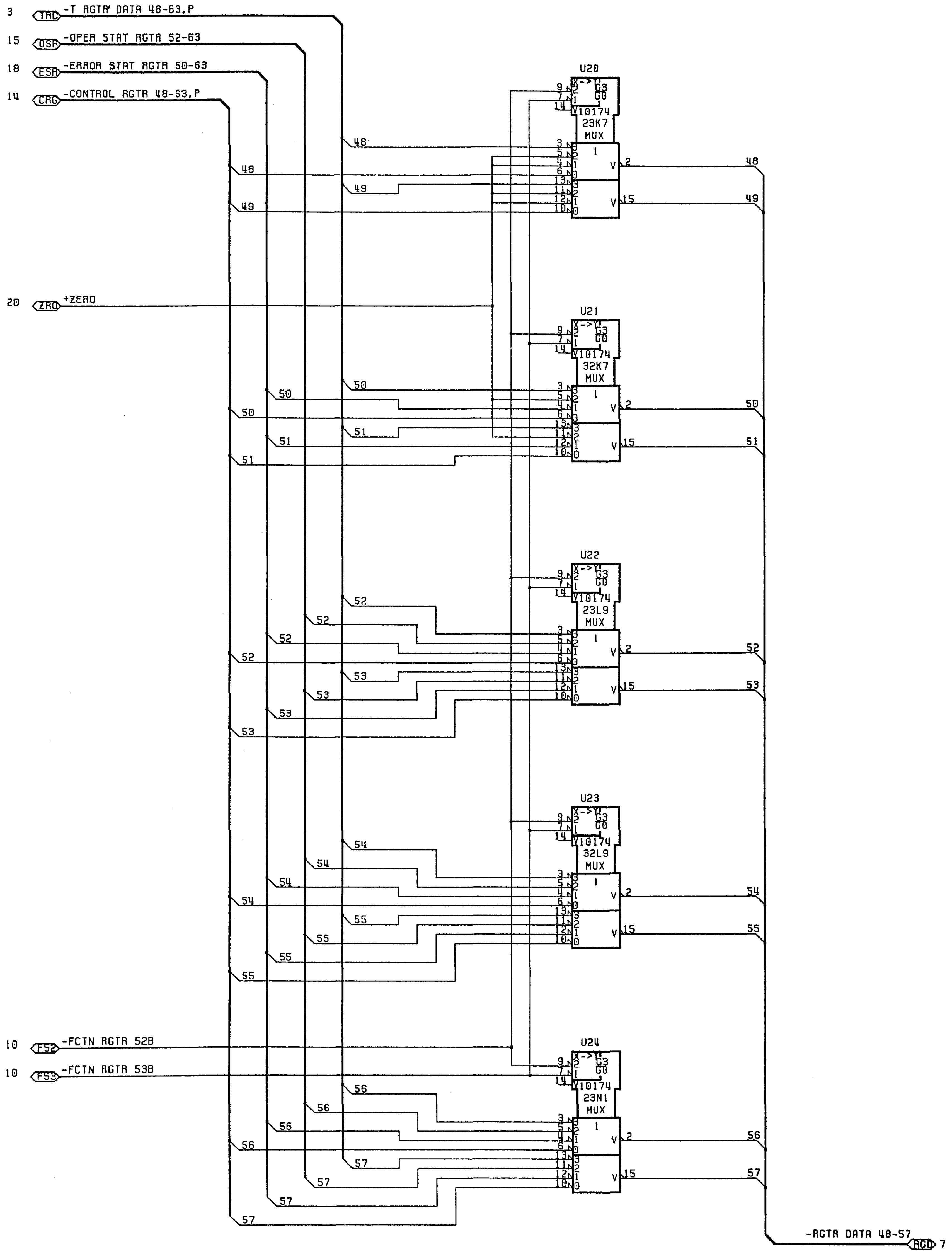

OUTPUT DRIVERS
(DATA TO THE KZ)
2 COD -OUTPUT DATA 48-63
2 P12 -12 BIT PARITY
20 ZRO +ZERO
U12-A
NC 12 G1
10101
23Q7
&
4 1
5
2 T
-PP OUTPUT DATA P A036 JZOPPO
U13
1
10197
23F9
U14
1
10197
41E7
9
5
6
7
10
11
12
2
3
4
13
14
15
52
53
54
55
56
57
58
59
60
61
62
63
-PP OUTPUT DATA 52 A031 JZOP52
-PP OUTPUT DATA 53 B033 JZOP53
-PP OUTPUT DATA 54 B010 JZOP54
-PP OUTPUT DATA 55 B013 JZOP55
-PP OUTPUT DATA 56 B017 JZOP56
-PP OUTPUT DATA 57 A029 JZOP57
-PP OUTPUT DATA 58 A032 JZOP58
-PP OUTPUT DATA 59 B035 JZOP59
-PP OUTPUT DATA 60 B011 JZOP60
-PP OUTPUT DATA 61 B015 JZOP61
-PP OUTPUT DATA 62 A027 JZOP62
-PP OUTPUT DATA 63 A030 JZOP63
T RGTR DATA IN AND OUT (3.0)
12 RT1 -READ T
12 CT1 +CLR T
12 CT2 +CLR T
2 P16 -16 BIT PARITY
U15
10173
41K7
RGTR
U16
10173
41L9
RGTR
U17
10173
41N1
RGTR
U18
10173
41Q3
RGTR
C
G2
G1
2CD
1CD
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
P
-T RGTR DATA 48 B057 C0OT48
-T RGTR DATA 49 A058 C0OT49
-T RGTR DATA 50 B058 C0OT50
-T RGTR DATA 51 A059 C0OT51
-T RGTR DATA 52 B059 C0OT52
-T RGTR DATA 53 A060 C0OT53
-T RGTR DATA 54 B060 C0OT54
-T RGTR DATA 55 A062 C0OT55
-T RGTR DATA 56 B062 C0OT56
-T RGTR DATA 57 A063 C0OT57
-T RGTR DATA 58 B063 C0OT58
-T RGTR DATA 59 A064 C0OT59
-T RGTR DATA 60 B064 C0OT60
-T RGTR DATA 61 A067 C0OT61
-T RGTR DATA 62 B067 C0OT62
-T RGTR DATA 63 A068 C0OT63
-T RGTR DATA P A057 C0OTPB
-T RGTR DATA 48-63,P TRD 4,5
U19-A
1
10104
41P5
4
5
2
1 TERMINATE AT FARTHEST POINT FROM THE CONN PIN

CONTROL DATA

170 DMA CHAN ADAPTER BAS I/F
OUTPUT DRIVERS AND
T RGTR DATA IN AND OUT
TYPE 1KXH

B	DWG NO. 22132519		DATE 10/15/86	REV A
SHEET NO. 3		60462210	PAGE KX-03	

REGISTER SELECT MUX
BITS 48-57 (3.1)

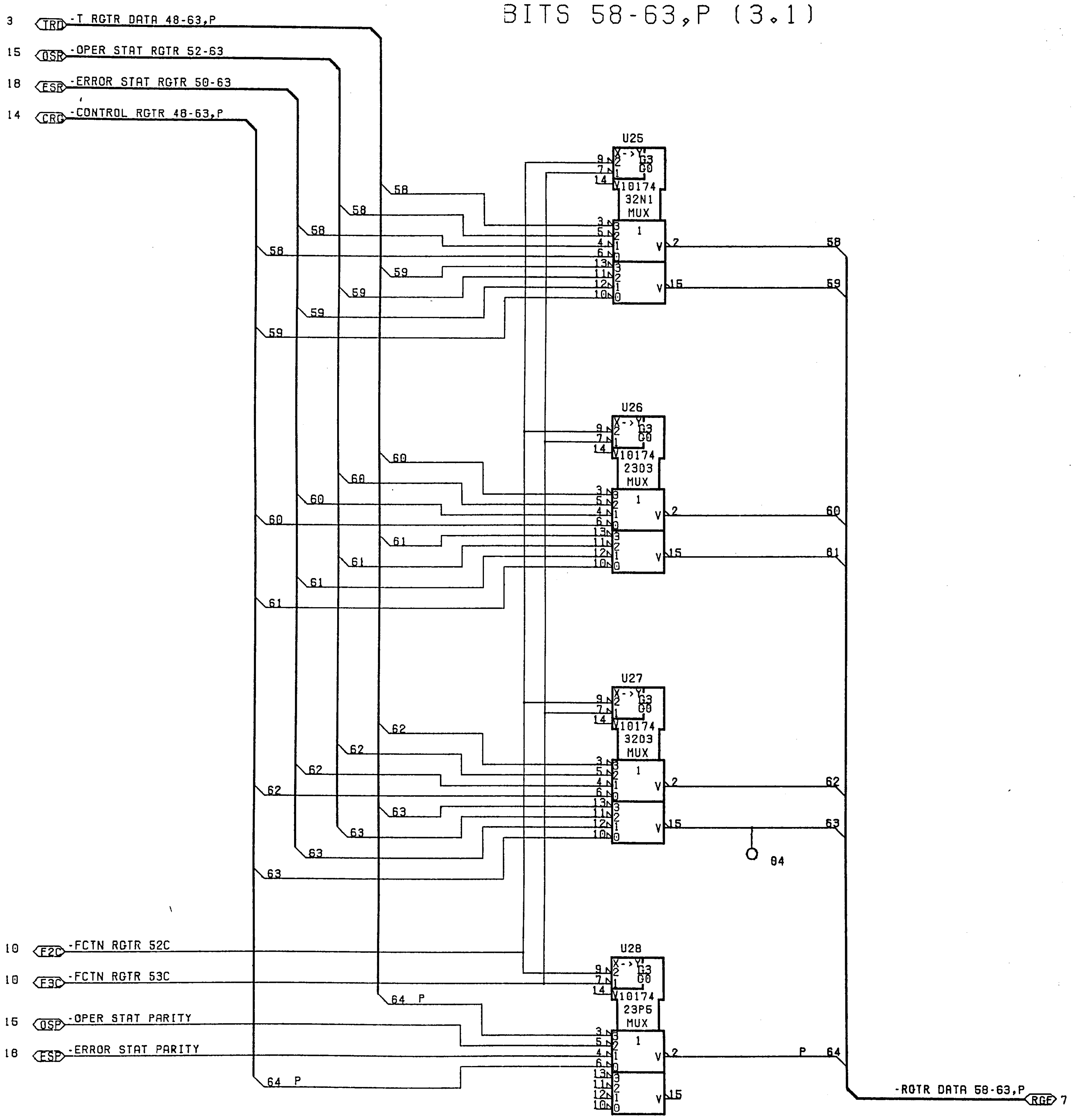


CONTROL DATA

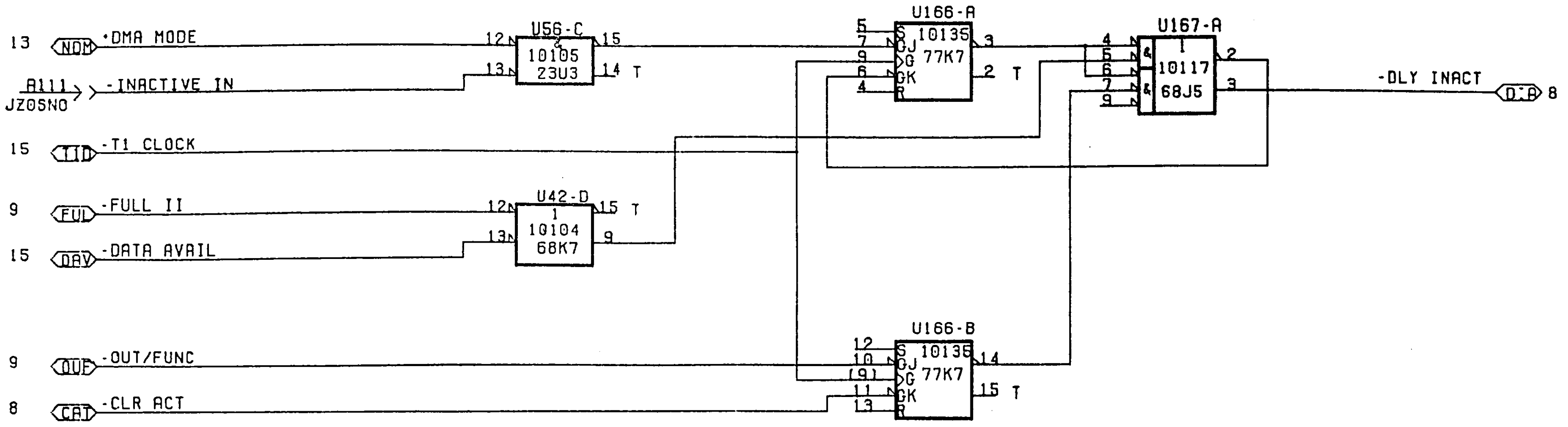
170 DMA CHAN ADAPTER BAS I/F
REGISTER SELECT MUX
BITS 48-57
TYPE 1KXH

B	DWG NO. 22132519		DATE 10/15/86		REV A
SHEET NO. 4	60462210		PAGE KX-04		

REGISTER SELECT MUX
BITS 58-63,P (3.1)

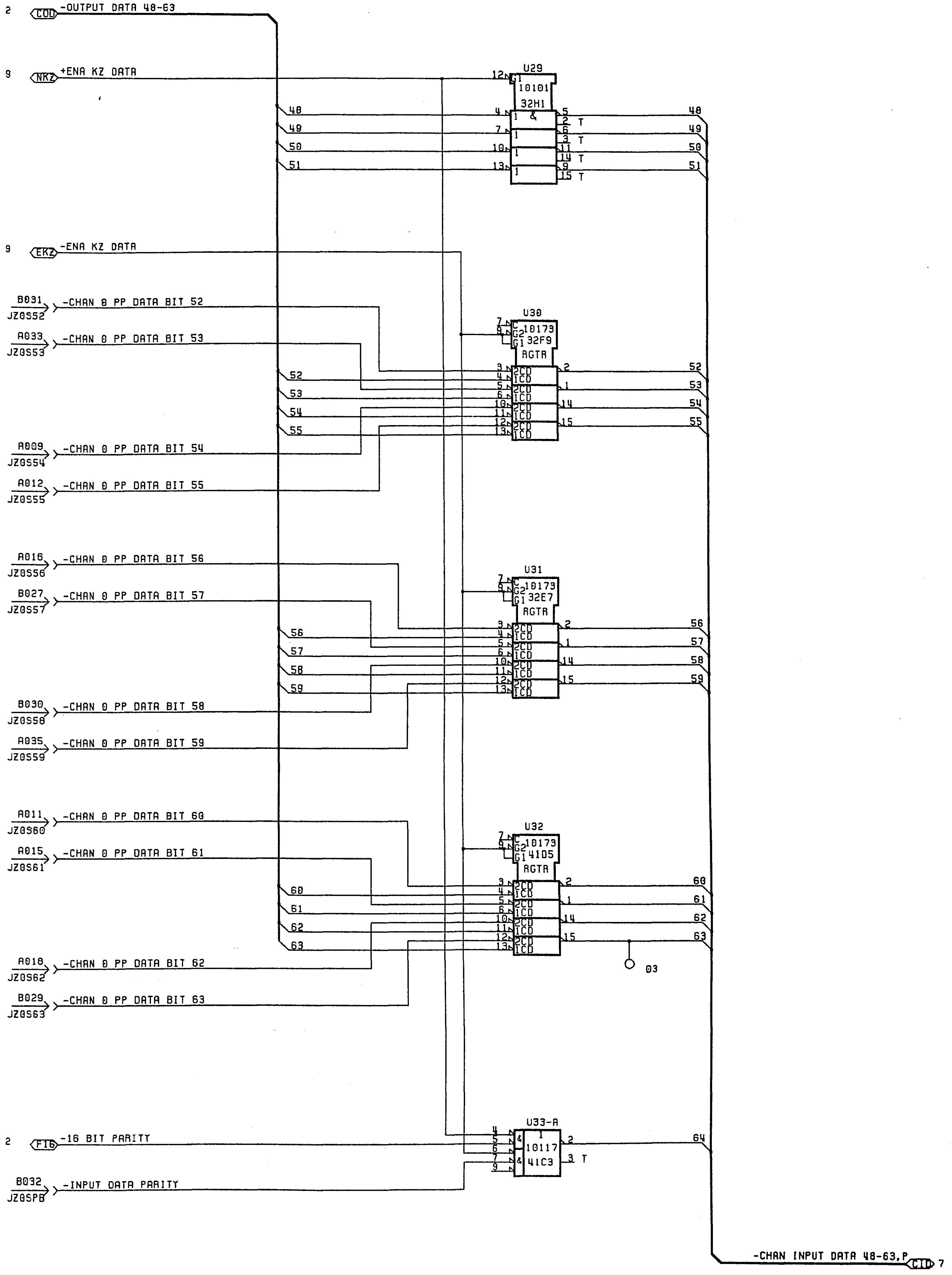


INACTIVE IN DELAY NETWORK



CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F REGISTER SELECT MUX BITS 58-63,P TYPE 1KXH	B	DWG NO. 22132519	DATE 10/19/87	REV B
	N	SHEET NO. 5	60462210	PAGE KX-05	

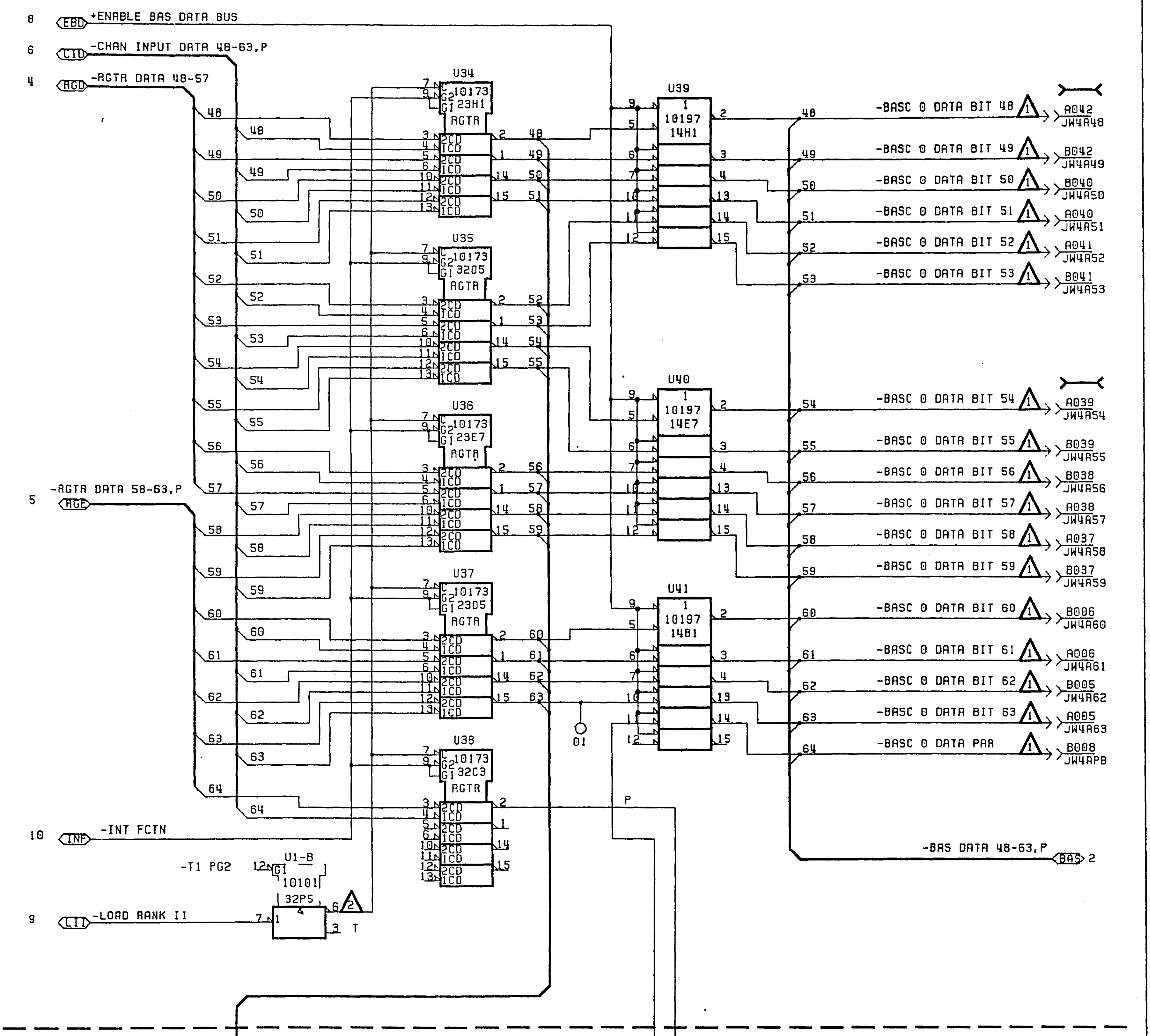
EXTERNAL INPUT DATA MUX (3.1)


2 COD -OUTPUT DATA 48-63
9 NKZ +ENA KZ DATA
9 EKZ -ENA KZ DATA
B031 JZ0S52 -CHAN 0 PP DATA BIT 52
A033 JZ0S53 -CHAN 0 PP DATA BIT 53
A009 JZ0S54 -CHAN 0 PP DATA BIT 54
A012 JZ0S55 -CHAN 0 PP DATA BIT 55
A016 JZ0S56 -CHAN 0 PP DATA BIT 56
B027 JZ0S57 -CHAN 0 PP DATA BIT 57
B030 JZ0S58 -CHAN 0 PP DATA BIT 58
A035 JZ0S59 -CHAN 0 PP DATA BIT 59
A011 JZ0S60 -CHAN 0 PP DATA BIT 60
A015 JZ0S61 -CHAN 0 PP DATA BIT 61
A018 JZ0S62 -CHAN 0 PP DATA BIT 62
B029 JZ0S63 -CHAN 0 PP DATA BIT 63
2 F16 -16 BIT PARITY
B032 JZ0SP0 -INPUT DATA PARITY
U29 10101 32H1
U30 10173 32F9 RGTR
U31 10173 32E7 RGTR
U32 10173 41D5 RGTR
U33-A 10117 41C3
03
-CHAN INPUT DATA 48-63,P CID 7

CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F EXTERNAL DATA INPUT MUX TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV A
		SHEET NO. 6	60462210	PAGE KX-06	

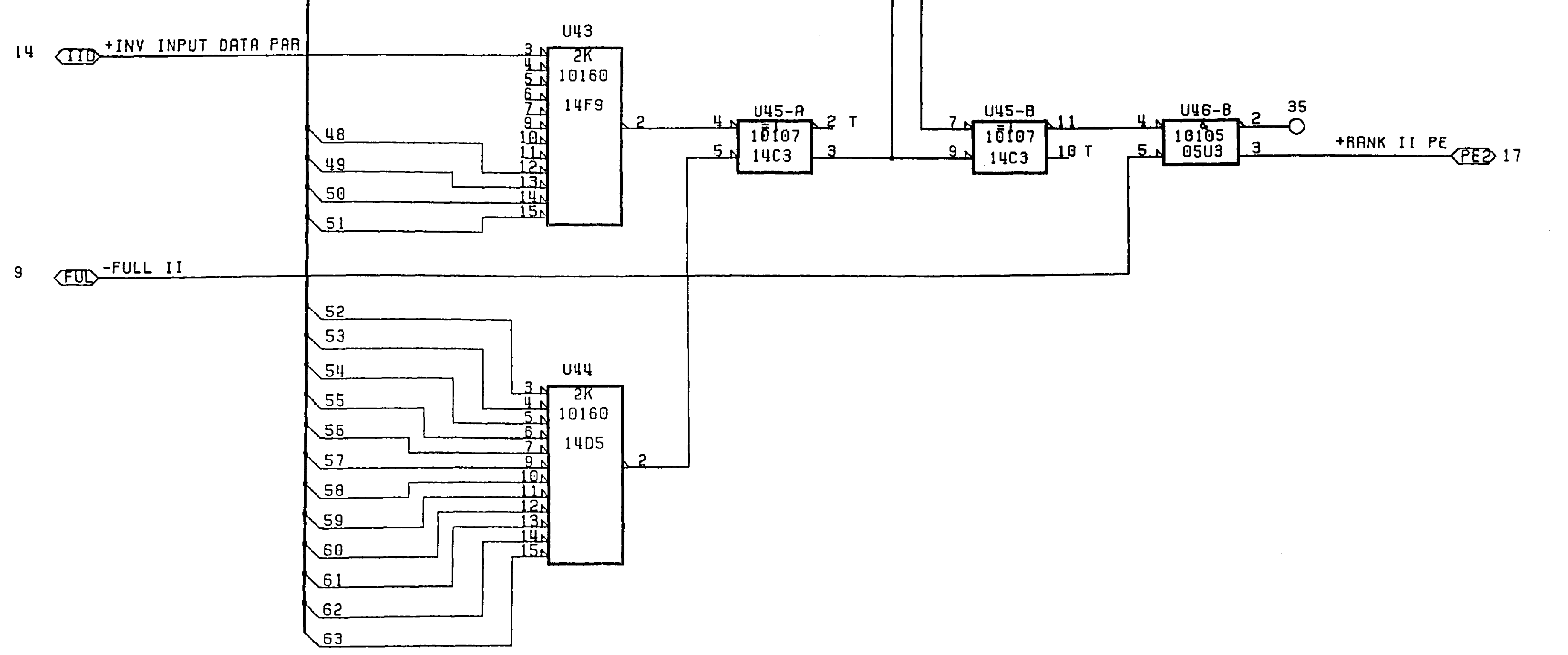
(RANK II)

ADAPTER INPUT REGISTER (3.1)



8 EBD +ENABLE BAS DATA BUS
6 CID -CHAN INPUT DATA 48-63,P
4 AGD -AGTR DATA 48-57
5 AGE -AGTR DATA 58-63,P
10 INF -INT FCTN
-T1 PG2
9 LIT -LOAD RANK II
U1-B 10101 32P5
U34 10173 23H1 RGTR
U35 10173 32D5 RGTR
U36 10173 23E7 RGTR
U37 10173 23D5 RGTR
U38 10173 32C3 RGTR
U39 1 10197 14H1
U40 1 10197 14E7
U41 1 10197 14B1
01
P
T
-BASC 0 DATA BIT 48 A042 JW4A48
-BASC 0 DATA BIT 49 B042 JW4A49
-BASC 0 DATA BIT 50 B040 JW4A50
-BASC 0 DATA BIT 51 A040 JW4A51
-BASC 0 DATA BIT 52 A041 JW4A52
-BASC 0 DATA BIT 53 B041 JW4A53
-BASC 0 DATA BIT 54 A039 JW4A54
-BASC 0 DATA BIT 55 B039 JW4A55
-BASC 0 DATA BIT 56 B038 JW4A56
-BASC 0 DATA BIT 57 A038 JW4A57
-BASC 0 DATA BIT 58 A037 JW4A58
-BASC 0 DATA BIT 59 B037 JW4A59
-BASC 0 DATA BIT 60 B006 JW4A60
-BASC 0 DATA BIT 61 A006 JW4A61
-BASC 0 DATA BIT 62 B005 JW4A62
-BASC 0 DATA BIT 63 A005 JW4A63
-BASC 0 DATA PAR B008 JW4APB
-BAS DATA 48-63,P BAS 2

ADAPTER INPUT PARITY CHECKER (3.1)

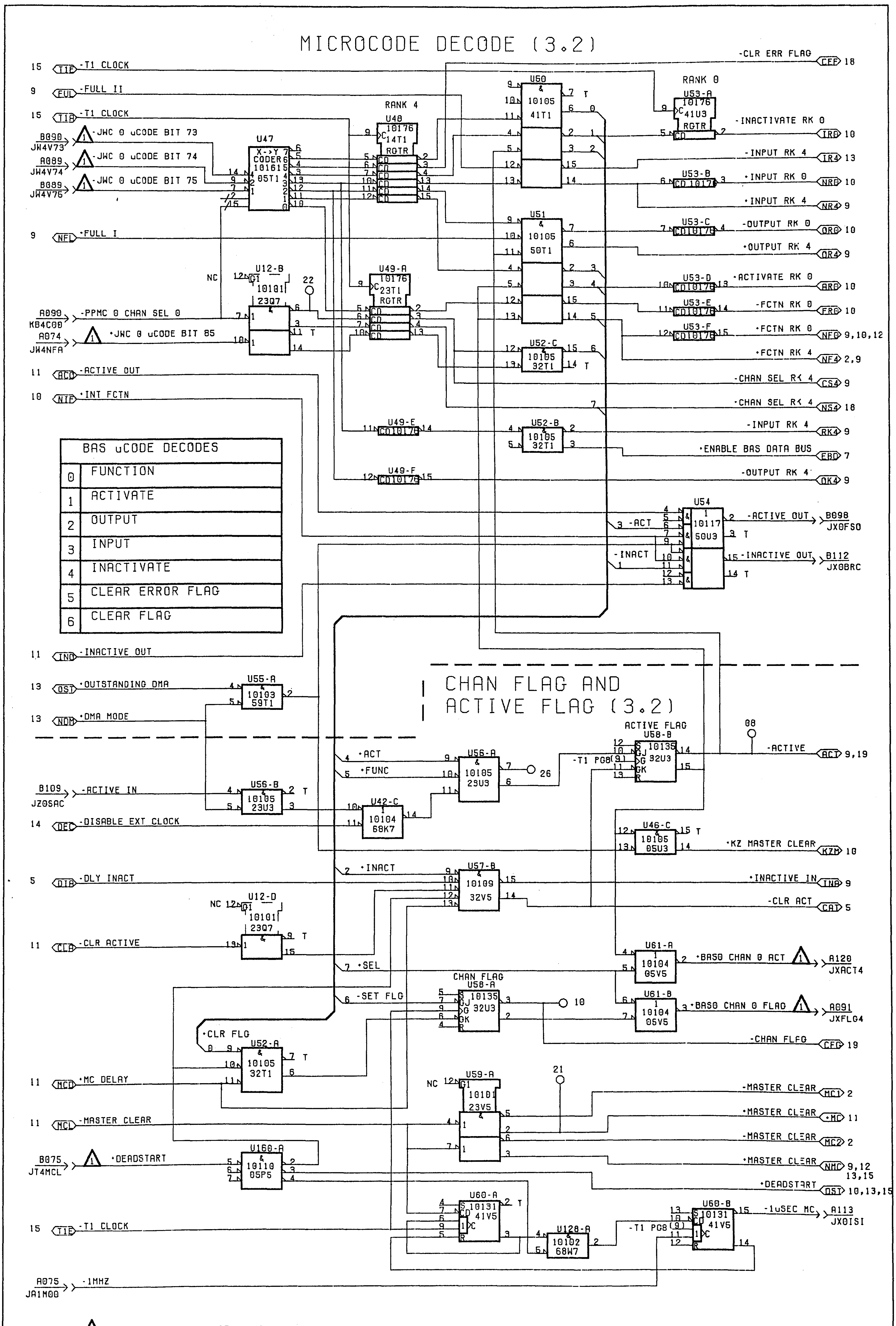


1 3 INCHES MAXIMUM AND NOT TERMINATED

2 12 INCHES MAXIMUM

CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F ADAPTER INPUT REGISTER AND INPUT PARITY CHECKER TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV A
		N	SHEET NO. 7	60462210	PAGE KX-07

MICROCODE DECODE (3.2)

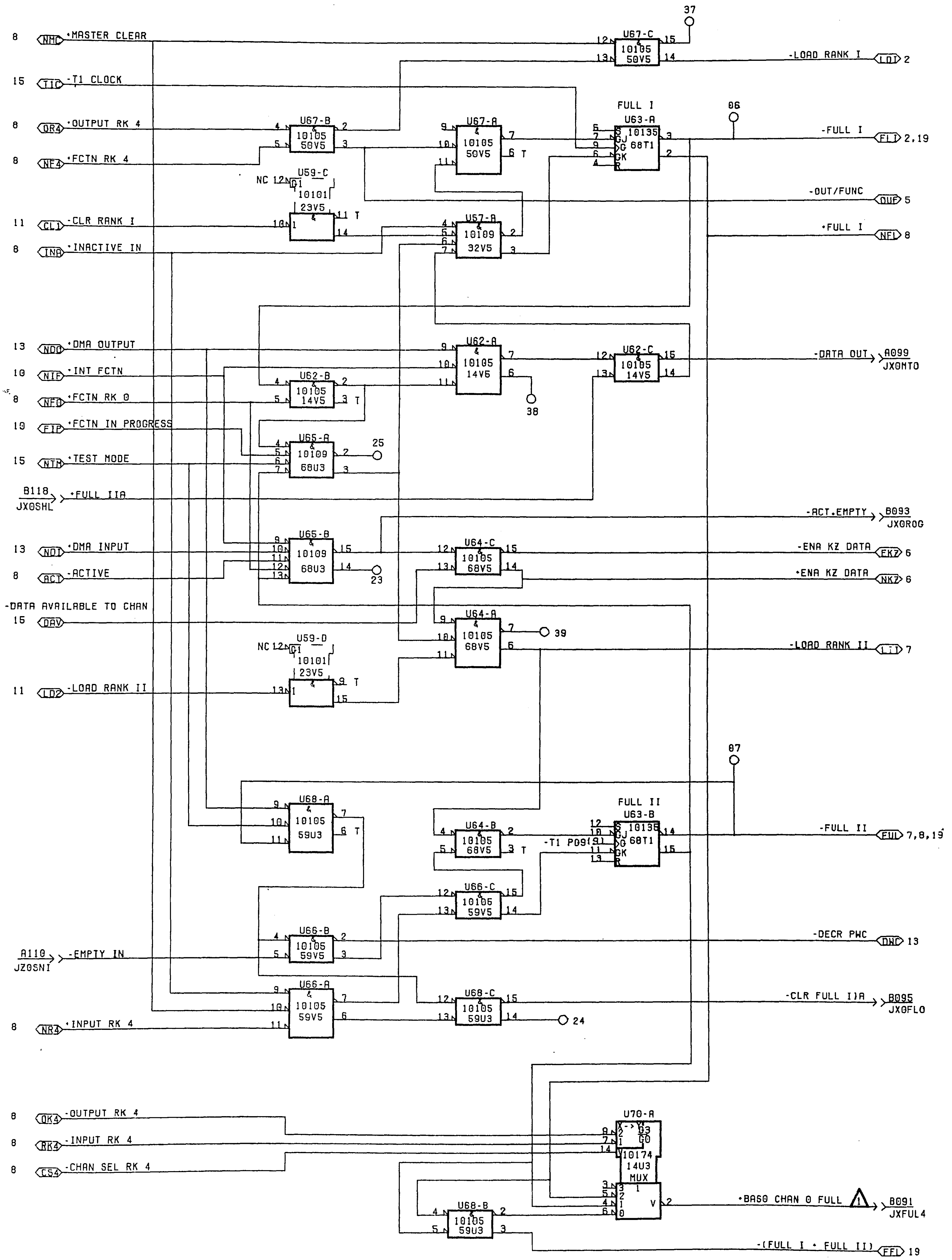


	BAS uCODE DECODES
0	FUNCTION
1	ACTIVATE
2	OUTPUT
3	INPUT
4	INACTIVATE
5	CLEAR ERROR FLAG
6	CLEAR FLAG

1 3" MAX LENGTH AND NOT TERMINATED

CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F BAS MICROCODE DECODE CHAN FLAG AND ACTIVE FLAG TYPE 1KXH	B	DWG NO. 22132519	DATE 10/19/87	REV B
		N	SHEET NO. 8	60462210	PAGE KX-08

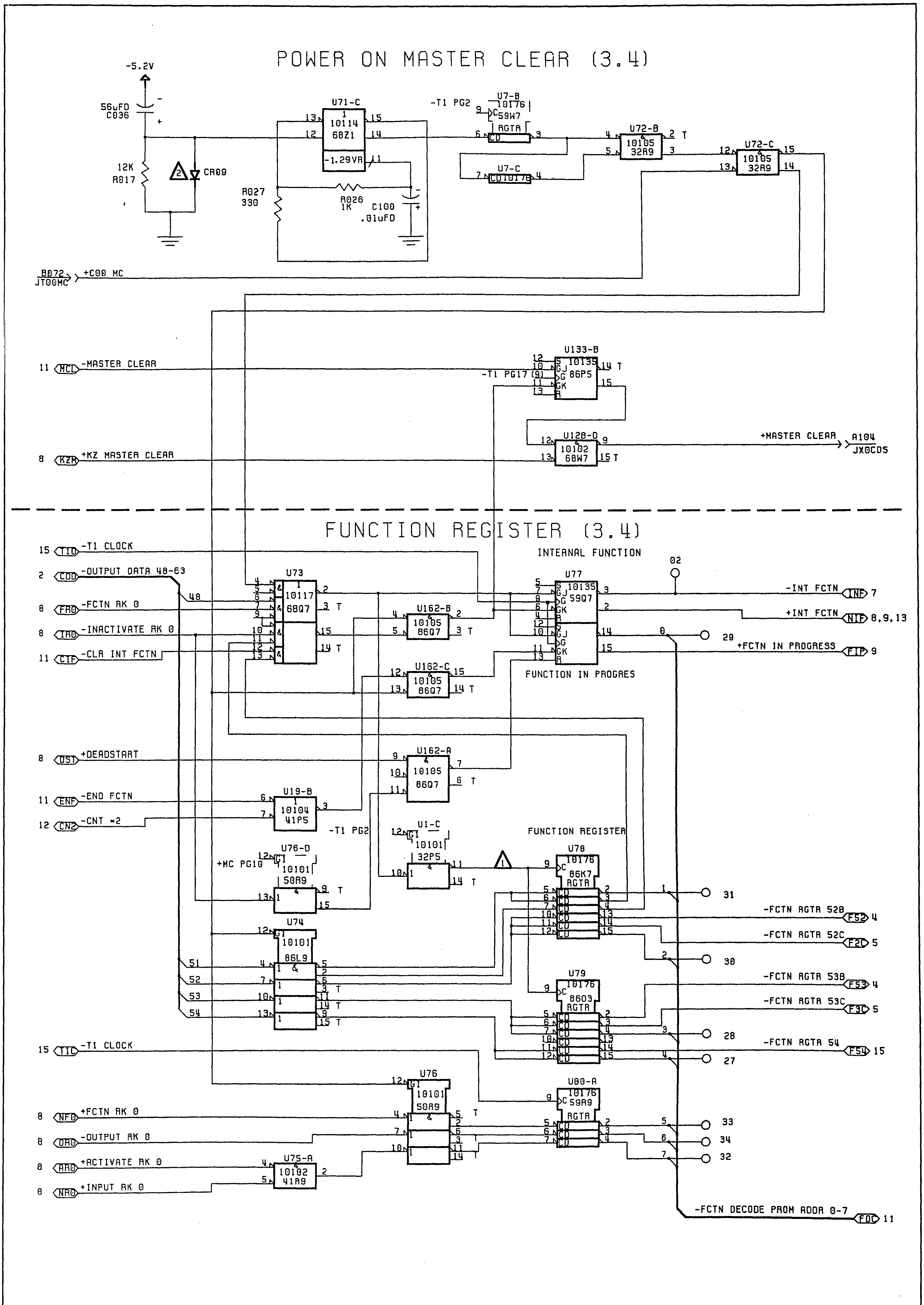
ADAPTER FULL FLAGS (3.3)



⚠ 3" MAX LENGTH AND NOT TERMINATED

CONTROL DATA
170 DMA CHAN ADAPTER BAS I/F
ADAPTER FULL FLAGS
TYPE 1KXH

B	
DWG NO.	22132519
DATE	10/19/87
REV	A
SHEET NO.	9
	60462210
PAGE	KX-09



1. 12 INCHES MAXIMUM

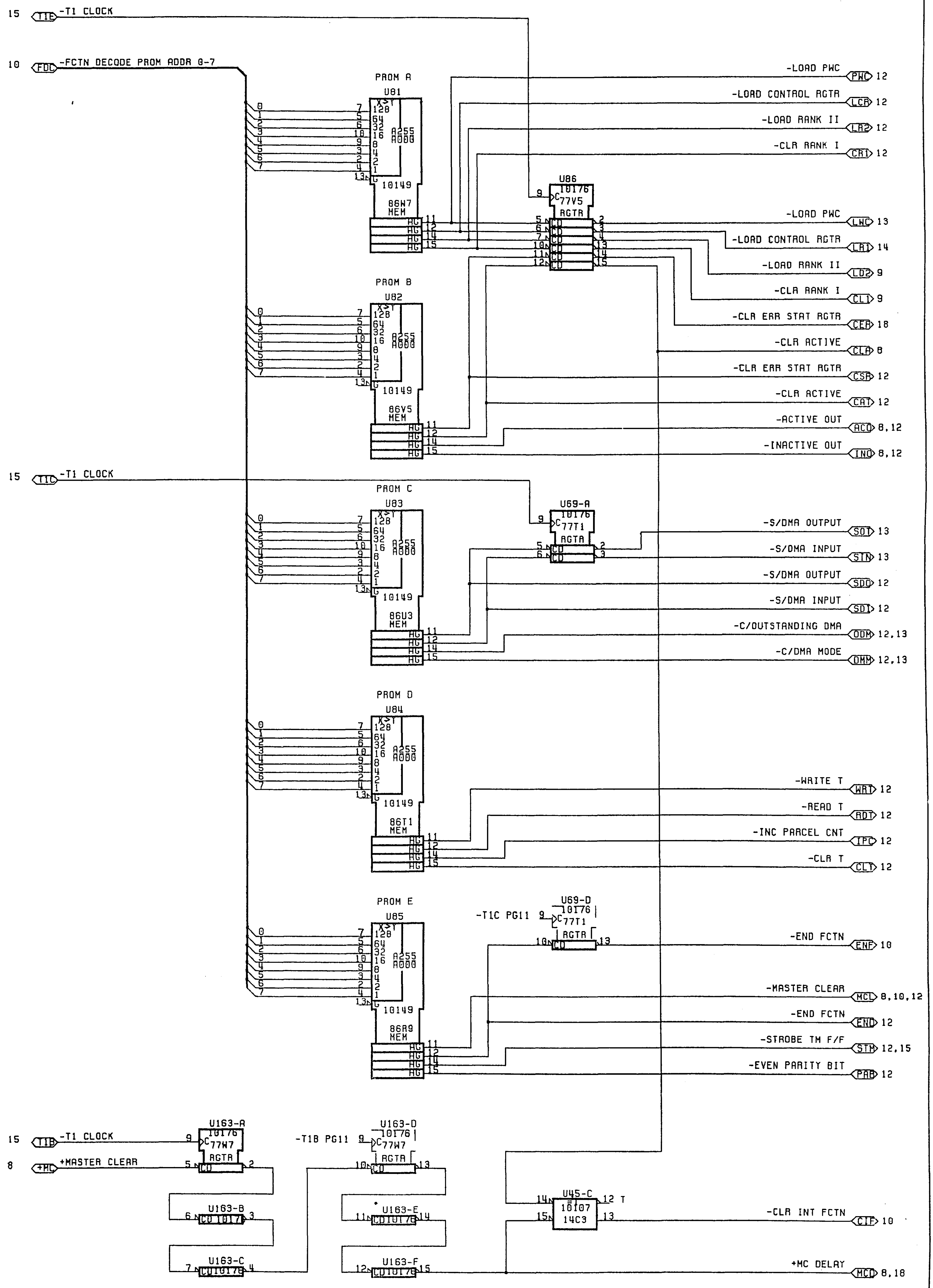
2. SCHOTTKY DIODE PN 12081500

CONTROL DATA

170 DMA CHAN ADAPTER BAS I/F
FUNCTION REGISTER
POWER ON MASTER CLEAR
TYPE 1KXH

B	DWG NO. 22132519	DATE 10/15/86	REV A
N	SHEET NO. 10	60462210	PAGE KX-10

FUNCTION DECODE PROMS A-E (3.4)



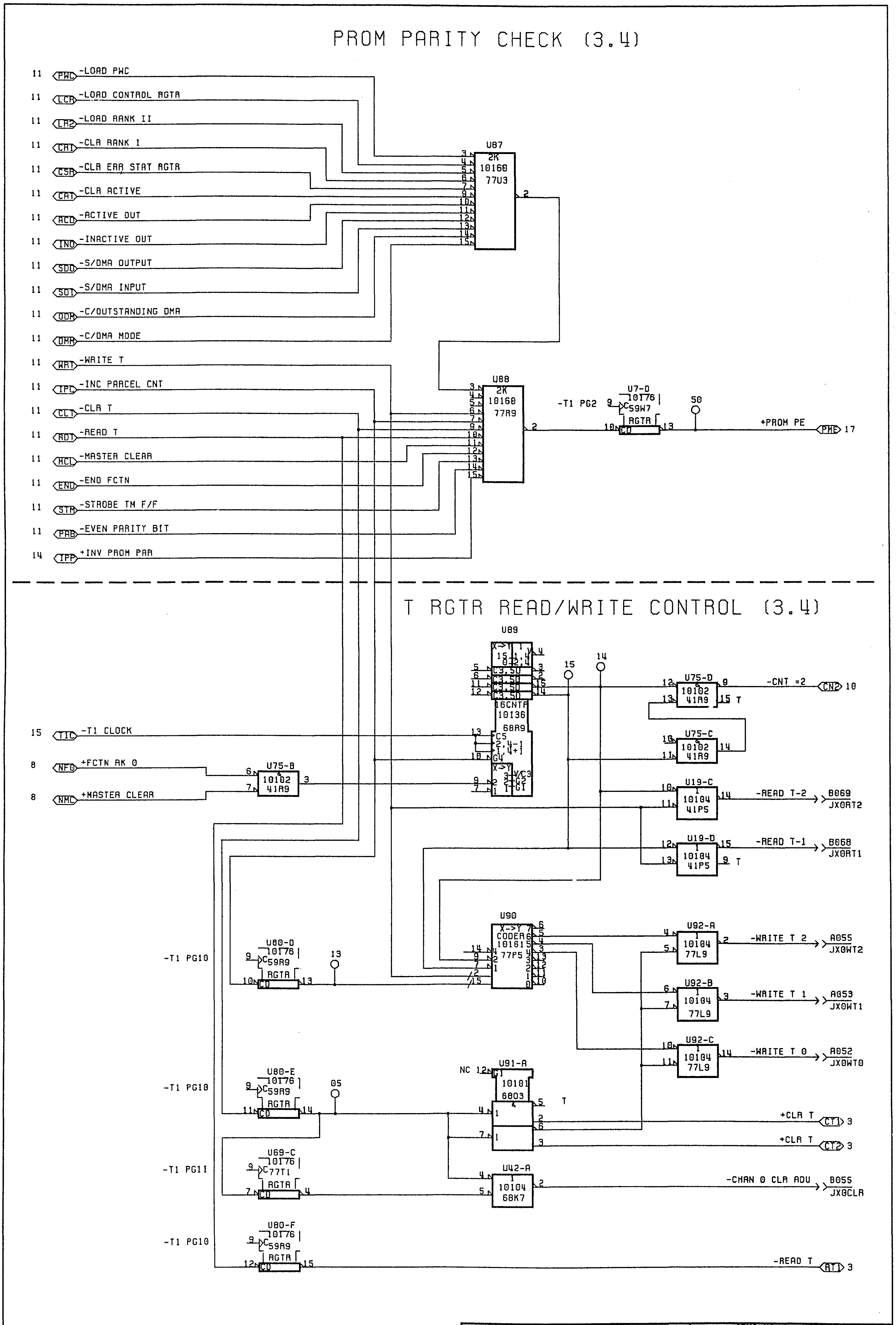
CONTROL DATA

170 DMA CHAN ADAPTER BAS I/F
FUNCTION DECODE PROMS A-E
TYPE 1KXH

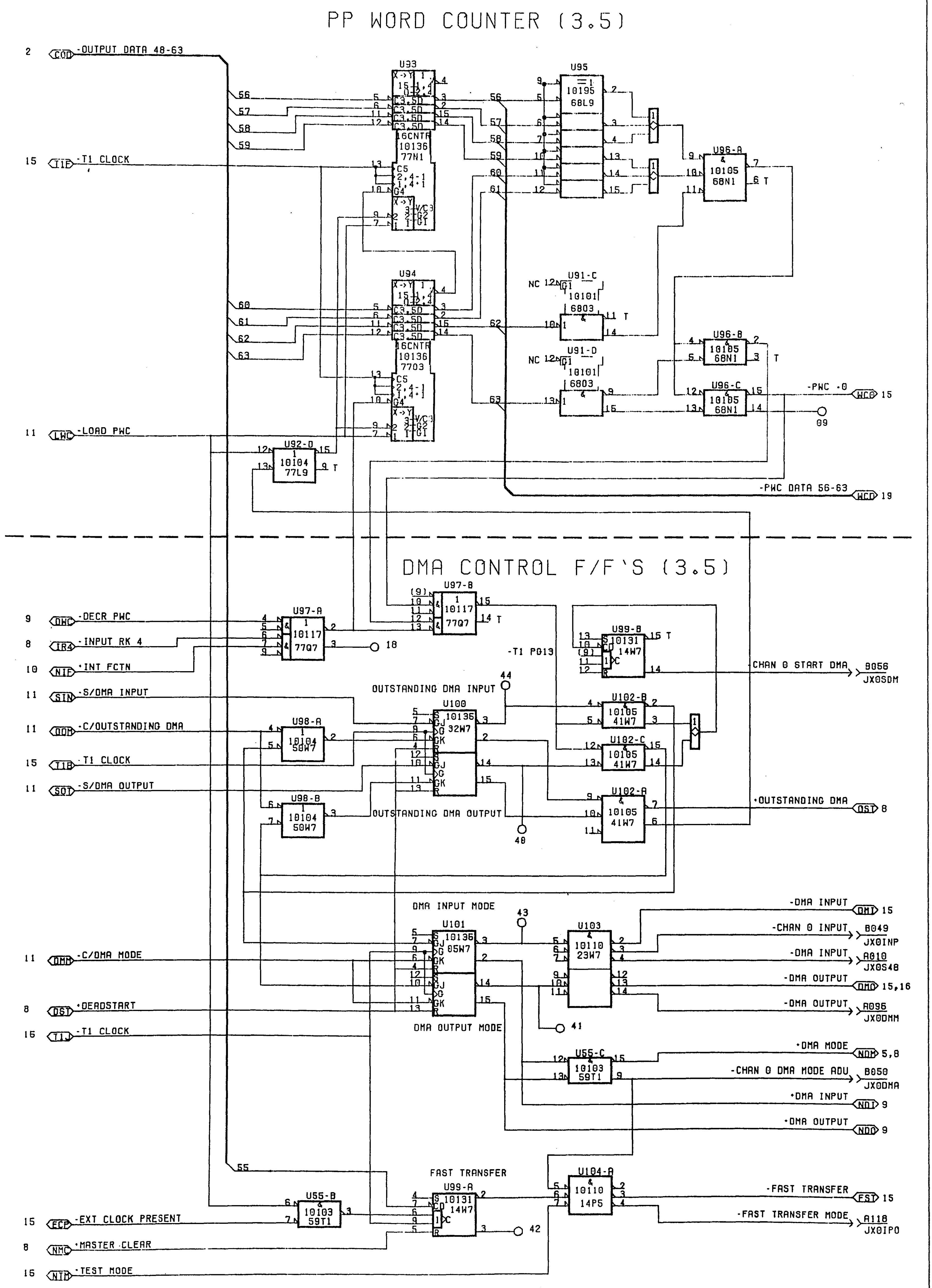
B
DWG NO. 22132519
DATE 10/15/86
REV A
SHEET NO. 11
60462210
PAGE KX-11

PROM PARITY CHECK (3.4)

T RGTR READ/WRITE CONTROL (3.4)



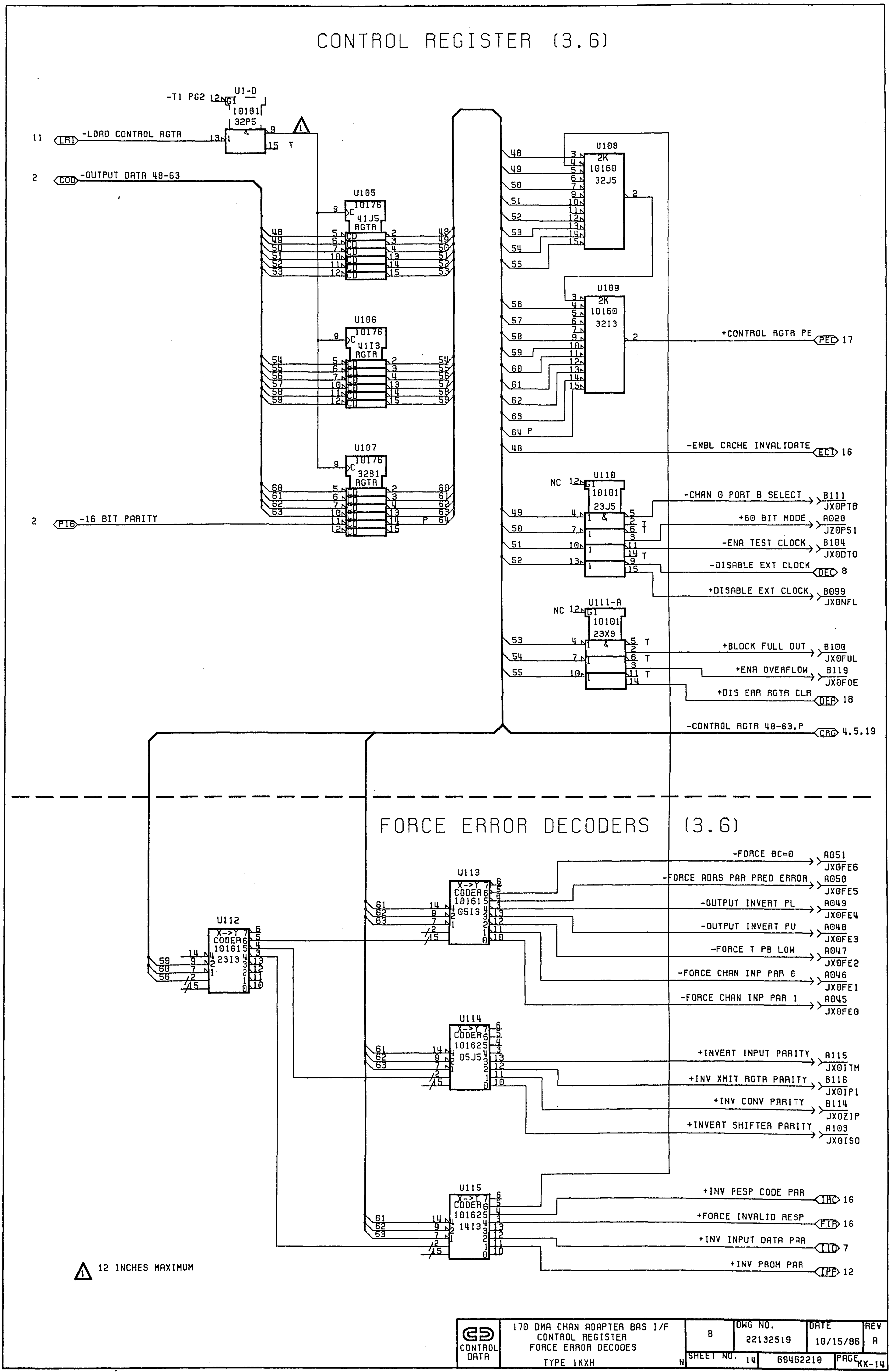
CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F PROM PARITY CHECK T RGTR READ/WRITE CONTROL TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV A
		N	SHEET NO. 12	60462210	PAGE KX-12



CONTROL DATA

170 DMA CHAN ADAPTER BRG I/F
DMA CONTROL F/F'S AND
PP WORD COUNTER
TYPE 1KXH

	DWG NO.	DATE	REV
B	22132519	10/19/87	B
SHEET NO. 13	60462210	PAGE KX-13	

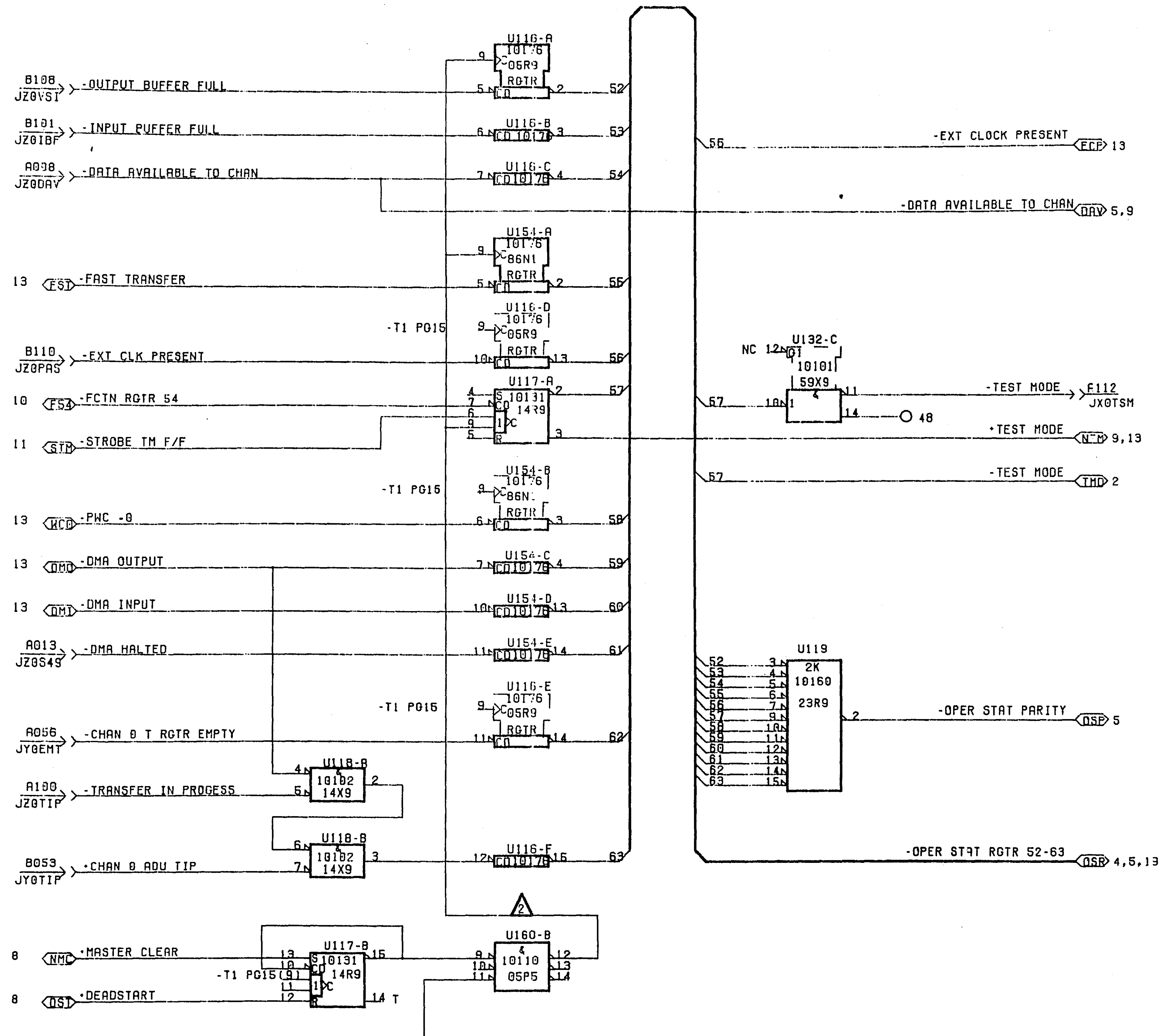

CONTROL REGISTER (3.6)
-T1 PG2
U1-D
10101
32P5
11 LRI -LOAD CONTROL RGTR
2 COD -OUTPUT DATA 48-63
2 P16 -16 BIT PARITY
U105 10176 41J5 RGTR
U106 10176 41I3 RGTR
U107 10176 32B1 RGTR
U108 2K 10160 32J5
U109 2K 10160 32I3
+CONTROL RGTR PE PEC 17
-ENBL CACHE INVALIDATE ECI 16
U110 10101 23J5
NC
-CHAN 0 PORT B SELECT B111 JX0PTB
+60 BIT MODE A028 JZ0P51
-ENA TEST CLOCK B104 JX0DT0
-DISABLE EXT CLOCK DEC 8
+DISABLE EXT CLOCK B099 JX0NFL
U111-A 10101 23X9
+BLOCK FULL OUT B100 JX0FUL
+ENA OVERFLOW B119 JX0F0E
+DIS ERR RGTR CLR DER 18
-CONTROL RGTR 48-63,P CRG 4,5,19
FORCE ERROR DECODERS (3.6)
U112 X->Y CODER 101615 23I3
U113 X->Y CODER 101615 05I3
U114 X->Y CODER 101625 05J5
U115 X->Y CODER 101625 14I3
-FORCE BC=0 A051 JX0FE6
-FORCE ADRS PAR PRED ERROR A050 JX0FE5
-OUTPUT INVERT PL A049 JX0FE4
-OUTPUT INVERT PU A048 JX0FE3
-FORCE T PB LOW A047 JX0FE2
-FORCE CHAN INP PAR 0 A046 JX0FE1
-FORCE CHAN INP PAR 1 A045 JX0FE0
+INVERT INPUT PARITY A115 JX0ITM
+INV XMIT RGTR PARITY B116 JX0IP1
+INV CONV PARITY B114 JX0ZIP
+INVERT SHIFTER PARITY A103 JX0IS0
+INV RESP CODE PAR IRC 16
+FORCE INVALID RESP FIR 16
+INV INPUT DATA PAR IID 7
+INV PROM PAR IPP 12
12 INCHES MAXIMUM

CONTROL DATA

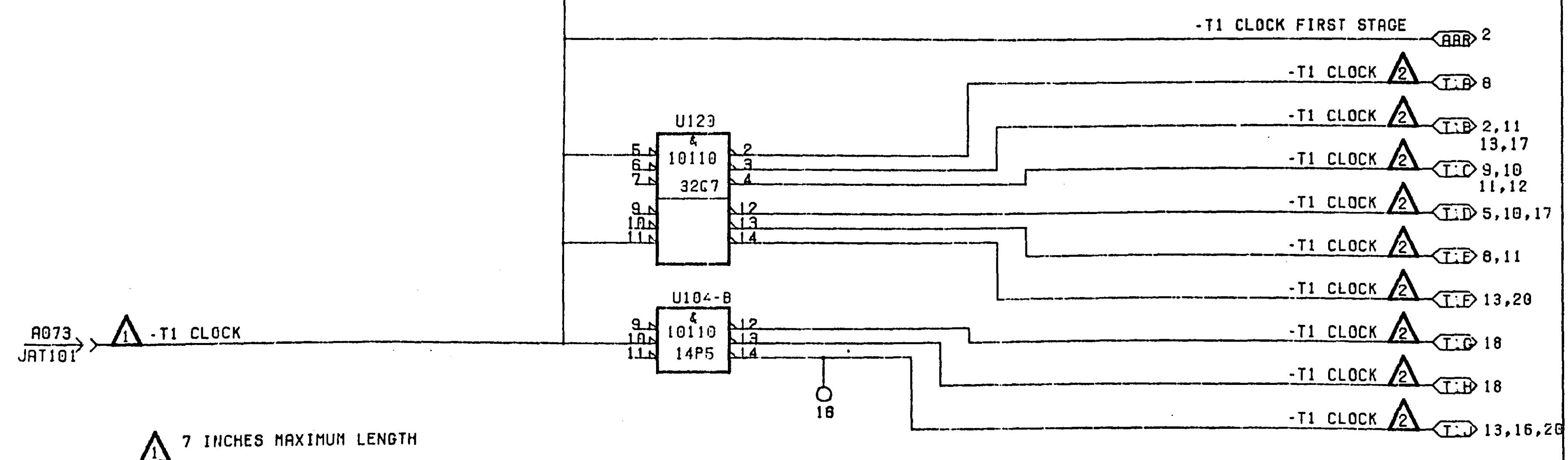
170 DMA CHAN ADAPTER BAS I/F
CONTROL REGISTER
FORCE ERROR DECODES
TYPE 1KXH

B	DWG NO. 22132519	DATE 10/15/86	REV A
SHEET NO. 14	60462210	PAGE KX-14	

OPERATIONAL STATUS NETWORK (3.5)



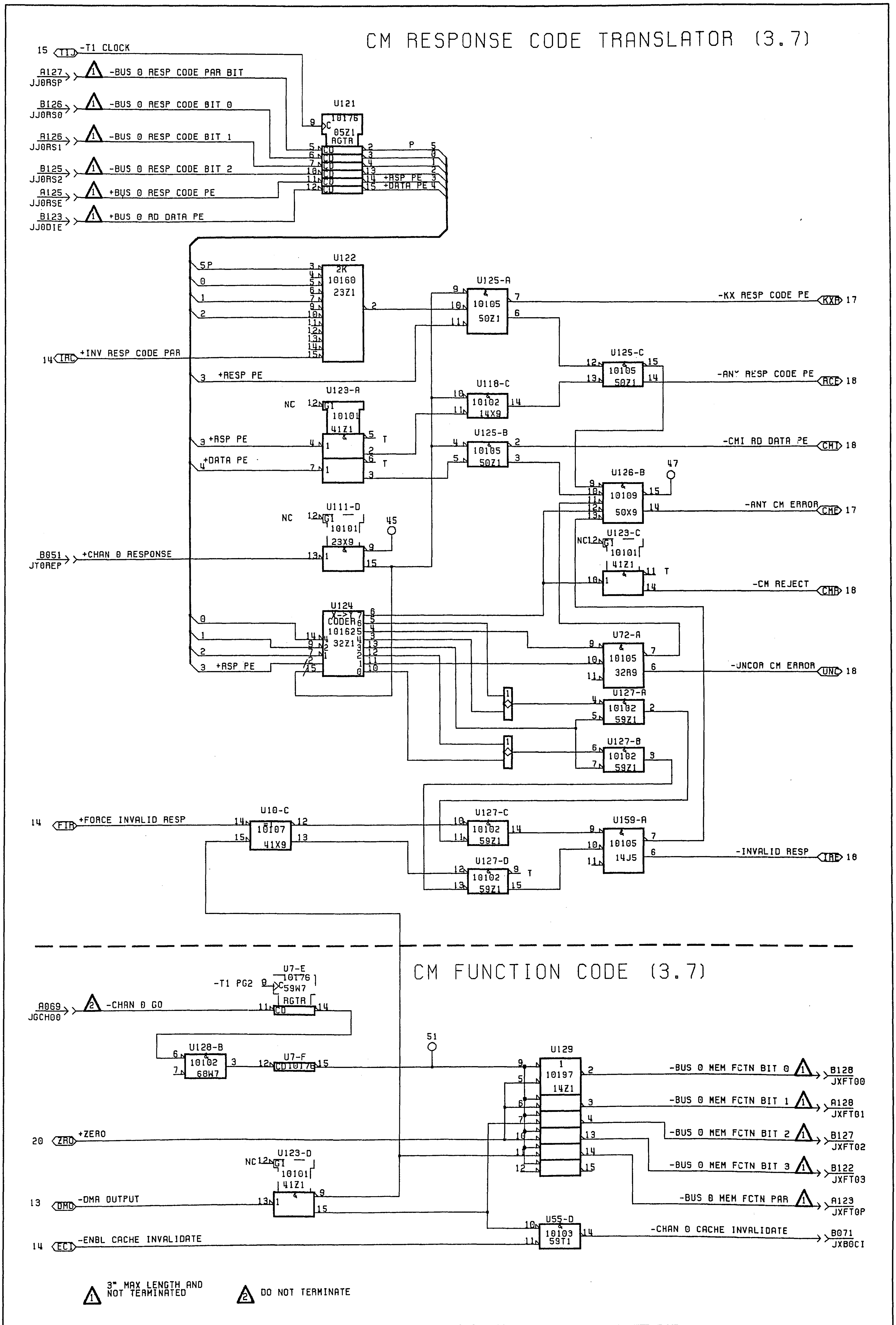
T1 CLOCK FANOUT



△1 7 INCHES MAXIMUM LENGTH

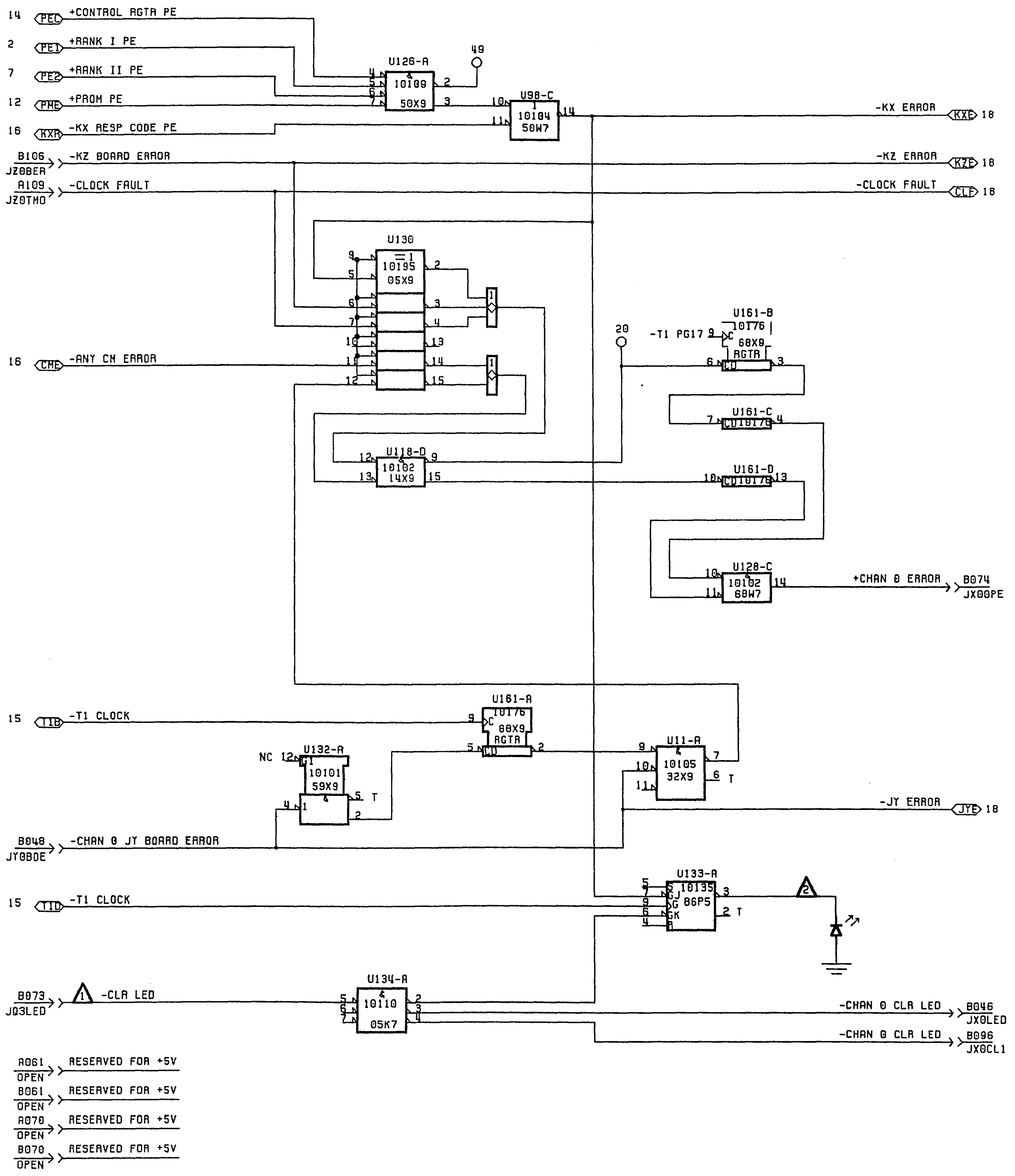
△2 12 INCHES MAXIMUM LENGTH

CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F OPERATIONAL STATUS NETWORK T1 CLOCK FANOUTS TYPE 1KXH	B	DWG NO. 22132519	DATE 10/19/87	REV B
		SHEET NO. 15	60462210	PAGE KX-15	



CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F CM RESPONSE CODE TRANSLATOR CM FUNCTION CODE TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV A
		N	SHEET NO. 16	60462210	PAGE KX-16

ERROR STATUS NETWORK (3.7)



1. 3" MAX LENGTH AND NOT TERMINATED

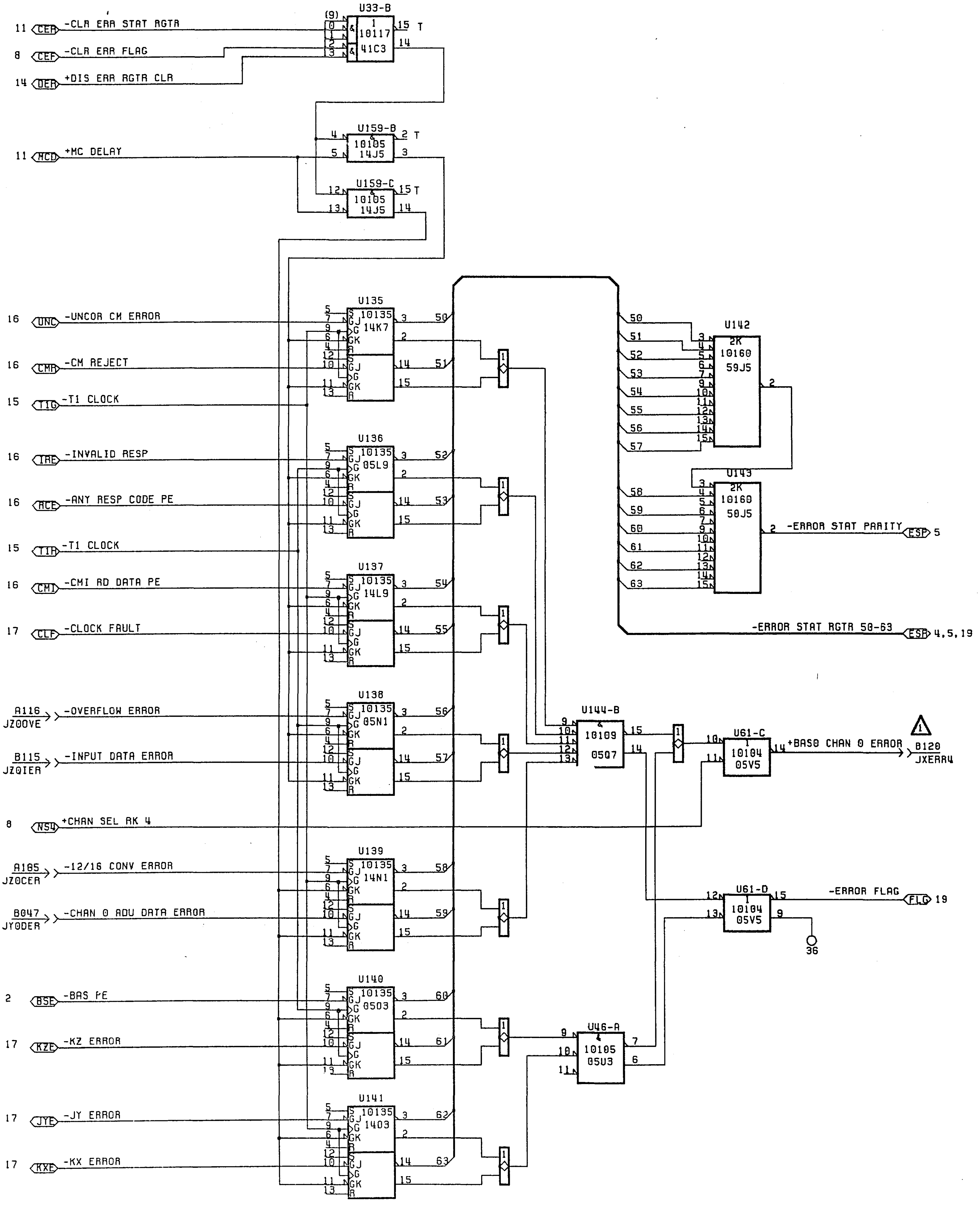
2. TERMINATE

CONTROL DATA

170 DMA CHAN ADAPTER BAS I/F
ERROR STATUS NETWORK
TYPE 1KXH

	DWG NO.	DATE	REV
B	22132519	10/15/86	A
SHEET NO. 17	60462210	PAGE KX-17	

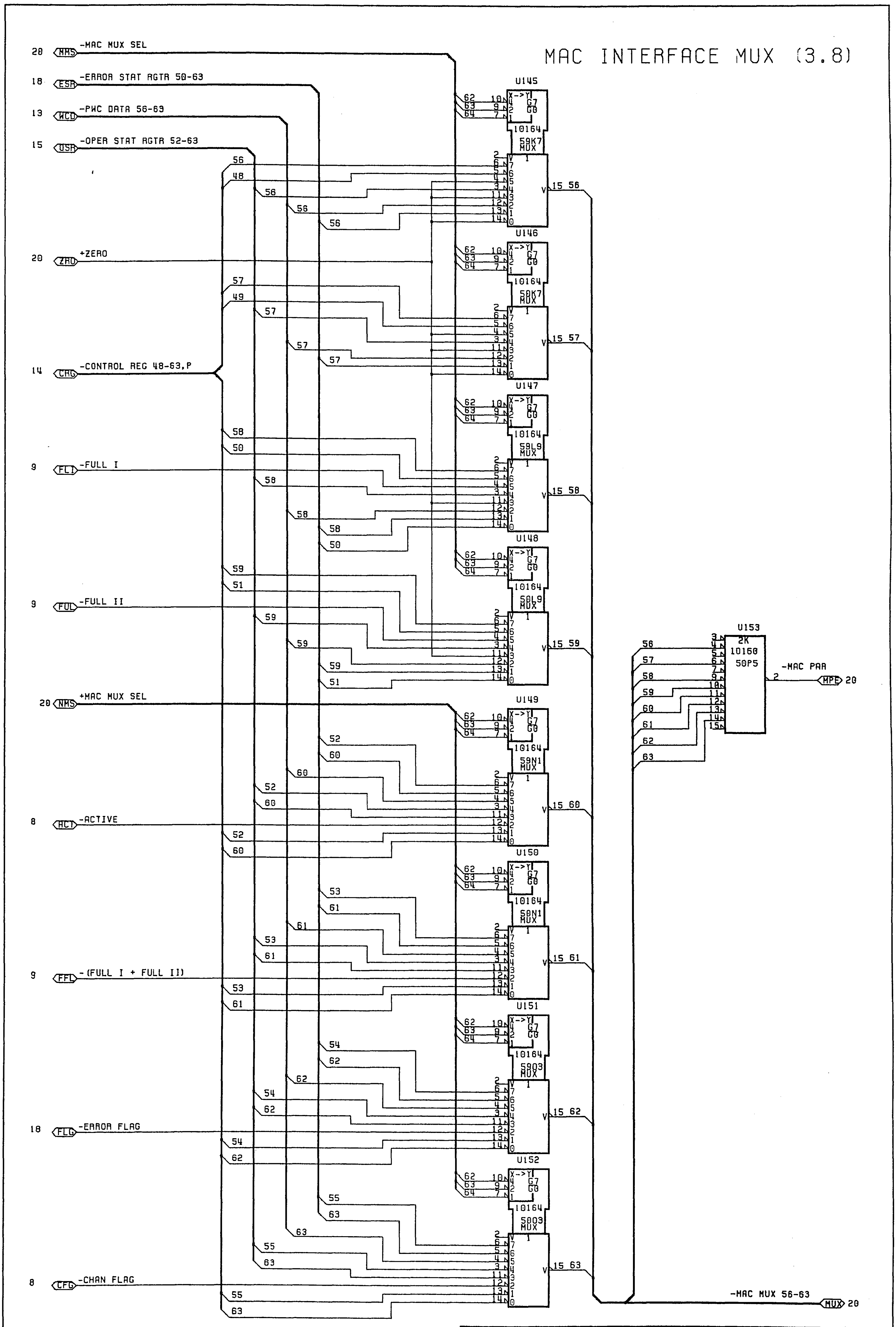
ERROR STATUS REGISTER (3.7)



⚠ 3" MAX LENGTH AND NOT TERMINATED

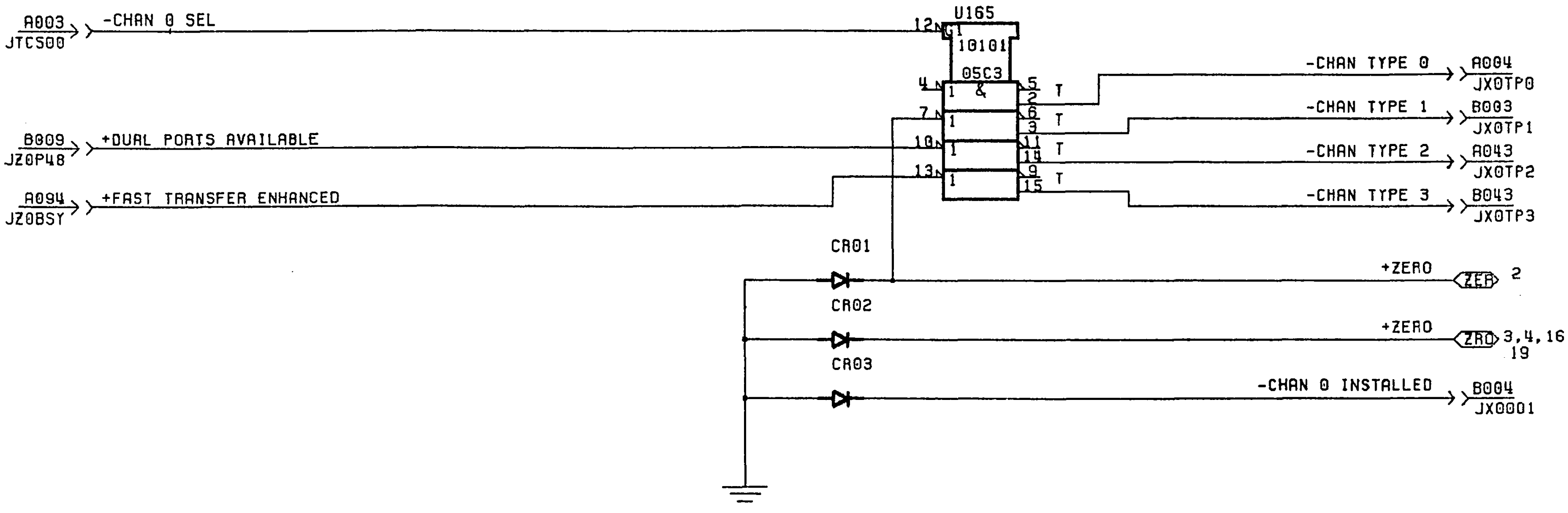
CONTROL DATA
170 DMA CHAN ADAPTER BAS I/F
ERROR STATUS REGISTER
TYPE 1KXH
B
DWG NO. 22132519
DATE 10/15/86
REV A
SHEET NO. 18 60462210
PAGE KX-18

MAC INTERFACE MUX (3.8)

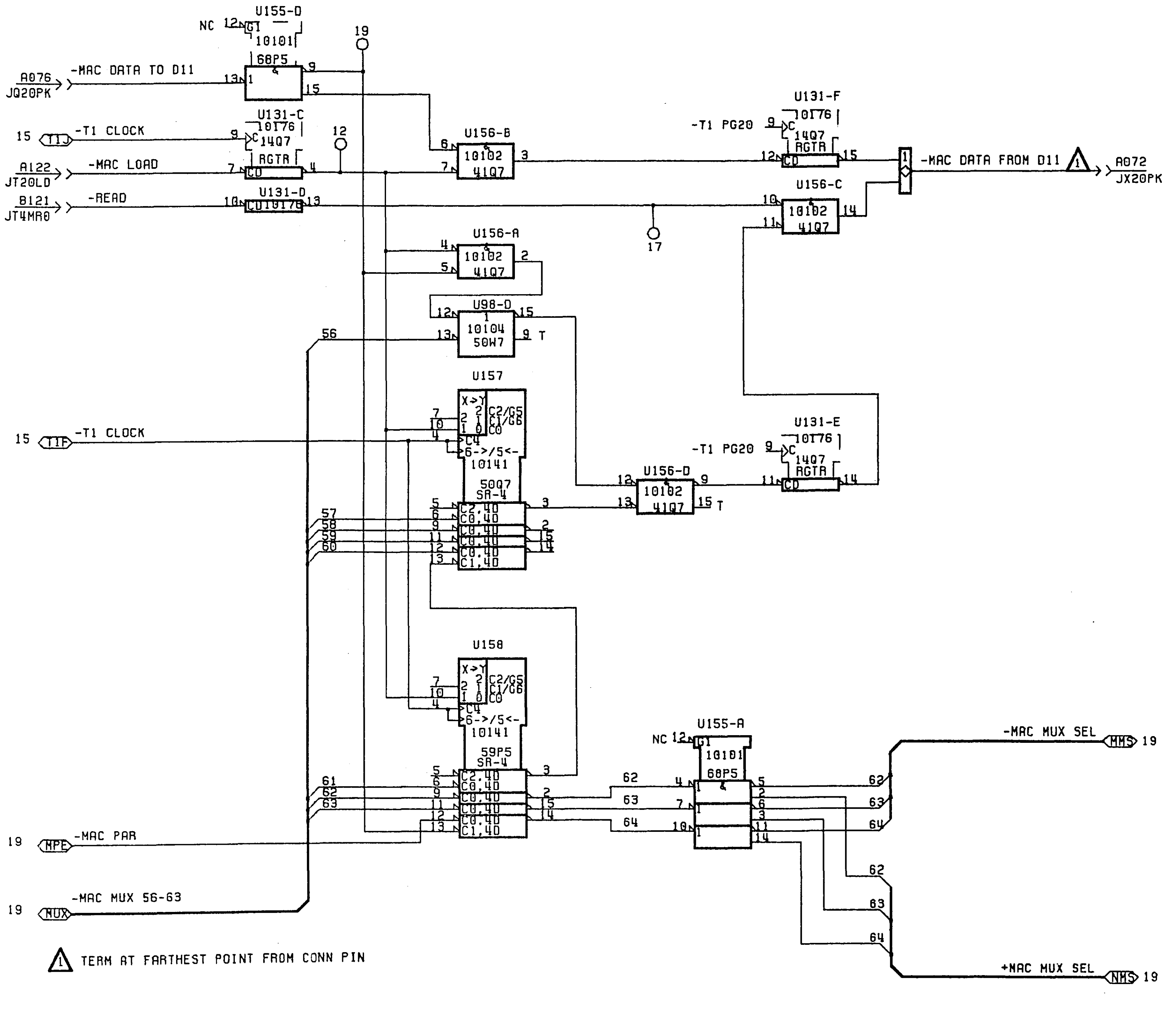


CONTROL DATA	170 DMA CHAN ADAPTER BAS I/F MAC INTERFACE MUX TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV A
		N	SHEET NO. 19	60462210	PAGE KX-19

CHANNEL TYPE IDENTIFIER (3.8)



MAC INTERFACE (3.8)



⚠1 TERM AT FARTHEST POINT FROM CONN PIN

CONTROL DATA

170 DMA CHAN ADAPTER BAS I/F
MAC INTERFACE
CHANNEL TYPE IDENTIFIER
TYPE 1KXH

B
DWG NO. 22132519
DATE 10/15/86
REV A
N
SHEET NO. 20 60462210
PAGE KX-20

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	07	-RANK II BIT 63	27	10	-FCTN CODE BIT 54
02	10	-INTERNAL FUNCTION	28	10	-FCTN CODE BIT 53
03	06	-CHAN INPUT BIT 63	29	10	-FCTN IN PROGRESS
04	05	-RGTR MUX BIT 63	30	10	-FCTN CODE BIT 52
05	12	-CLEAR T RGTR	31	10	-FCTN CODE BIT 51
06	09	-FULL I FLAG	32	10	-ACT OR INPUT RNK I
07	09	-FULL II FLAG	33	10	-FUNCTION RANK I
08	08	-ACTIVE FLAG	34	10	-OUTPUT RANK I
09	13	+PP WORD CNT = ZERO	35	07	-RANK II PE
10	08	-CHAN FLAG	36	18	+ERROR FLAG
11	02	-ADAPTER OUT BIT 63	37	09	+LOAD RANK I
12	20	-MAC LOAD	38	09	+DATA OUT
13	12	-INCT PARCEL CNT	39	09	+LOAD RANK II
14	12	-T COUNTER BIT 0	40	13	-OUTSTD DMA OUTPUT
15	12	-T COUNTER BIT 1	41	13	-DMA OUTPUT MODE
16	15	-T1 CLOCK	42	13	+FAST TRANSFER
17	20	-MAC READ	43	13	-DMA INPUT MODE
18	13	+DECR PP WORD CNTR	44	13	-OUTSTD DMA INPUT
19	20	-MAC DATA IN	45	16	-CHAN RESPONSE
20	17	-CHAN ERROR	46	02	-RANK I PE
21	08	+MASTER CLEAR	47	16	+ANY CM ERROR
22	08	-PPM CHAN SELECT	48	15	+TEST MODE
23	09	+ACTIVE AND EMPTY	49	17	+NON CM KX ERROR
24	09	+CLEAR FULL IIA	50	12	+PROM PE
25	09	-RANK I TO RANK II	51	16	+CHAN GO
26	08	+SET ACTIVE			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065, B065,A066,B066,A077,B077,A097,B097,A107, B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 (NU)
TERM	NONE
UNUSED	A008,B012,B016,A017,B018,A019,B019,A020,B020, A021,B021,A022,B022,A023,B023,A025,B025,A026, B026,B028,B036,B045,B052,A071,B076,A078,B078, A079,B079,A080,B080,A081,B081,A082,B082,A083 B083,A084,B084,A085,B085,A086,B086,A088,B088, A092,B092,B094,A095,A101,A102,B102,B103,B105, A106,A108,B113,A114,A119,A121

CONTROL DATA	CIO CHANNEL BOARD BAS I/F TESTPOINTS AND SIGNAL NAMES AND CONNECTOR PINS TYPE 1KXH	B	DWG NO. 22132519	DATE 10/15/86	REV A
		N	SHEET NO. 21	60462210	PAGE KX-21

1KZH CIO CHANNEL 170 DMA I/F

REVISION HISTORY B/M 41655300

DATE	REV	DESCRIPTION OF CHANGE	INIT
10/15/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	LHJ
12/16/86	B	ECO #48394 PAGE 4	SLP
03/10/87	C	ECO #48628 PAGES 2, 18, & 21	SLP
10/19/87	D	ECO #48862 PAGE 16 & 18	SLP

DWN	L H JOHNSON	10/23/86
CHKD	S L PJESCICH	10/23/86
ENG	D A ZAHALAN	10/23/86
PUBS	N ANDERSON	10/23/86
APP	D A ZAHALAN	10/23/86

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

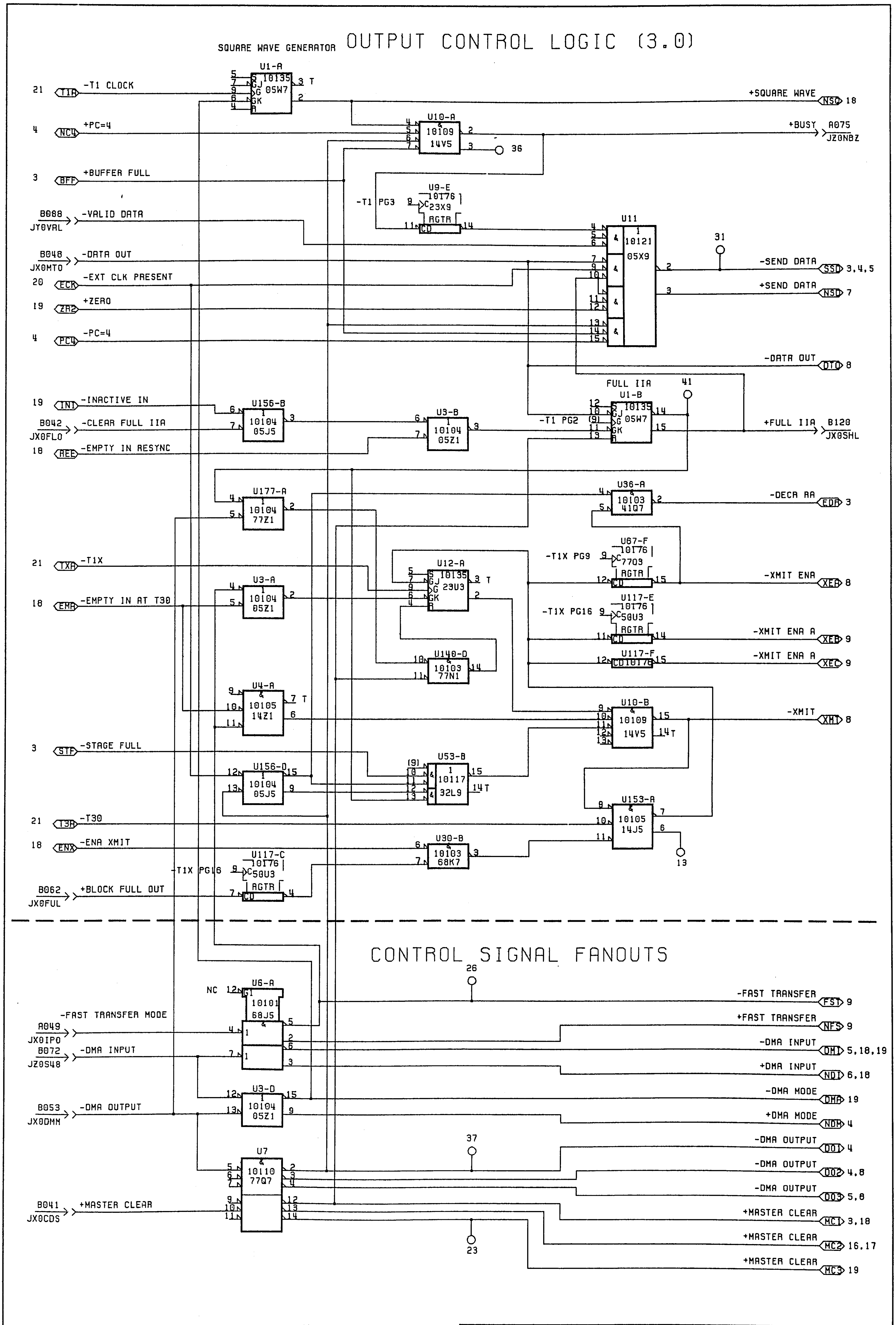
LOC: D09, D12, D15, D18, D21
C09, C12, C15, C18, C21

CONTROL DATA

REVISION HISTORY

TYPE 1KZH

B	DWG NO. 22132520	DATE 10/19/87	REV D
SHEET NO. 1	60462210	PAGE KZ-01	

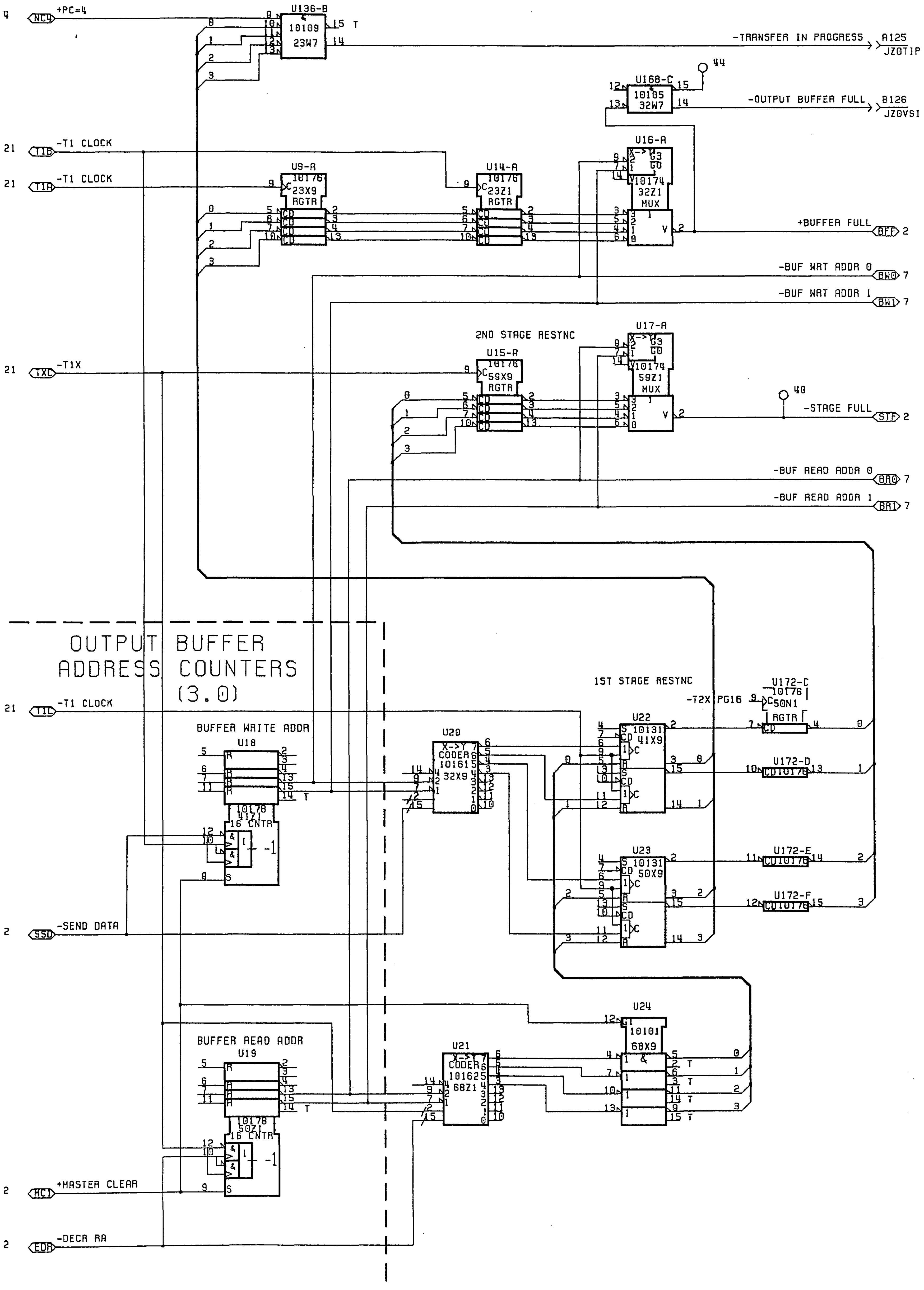


CONTROL DATA

170 DMA CHAN EXT I/F
OUTPUT CONTROL LOGIC
AND CONTROL SIGNAL FANOUTS
TYPE 1KZH

B	DWG NO. 22132520	DATE 03/10/87	REV C
SHEET NO. 2	60462210	PAGE KZ-02	

OUTPUT RESYNC NETWORK (3.0)

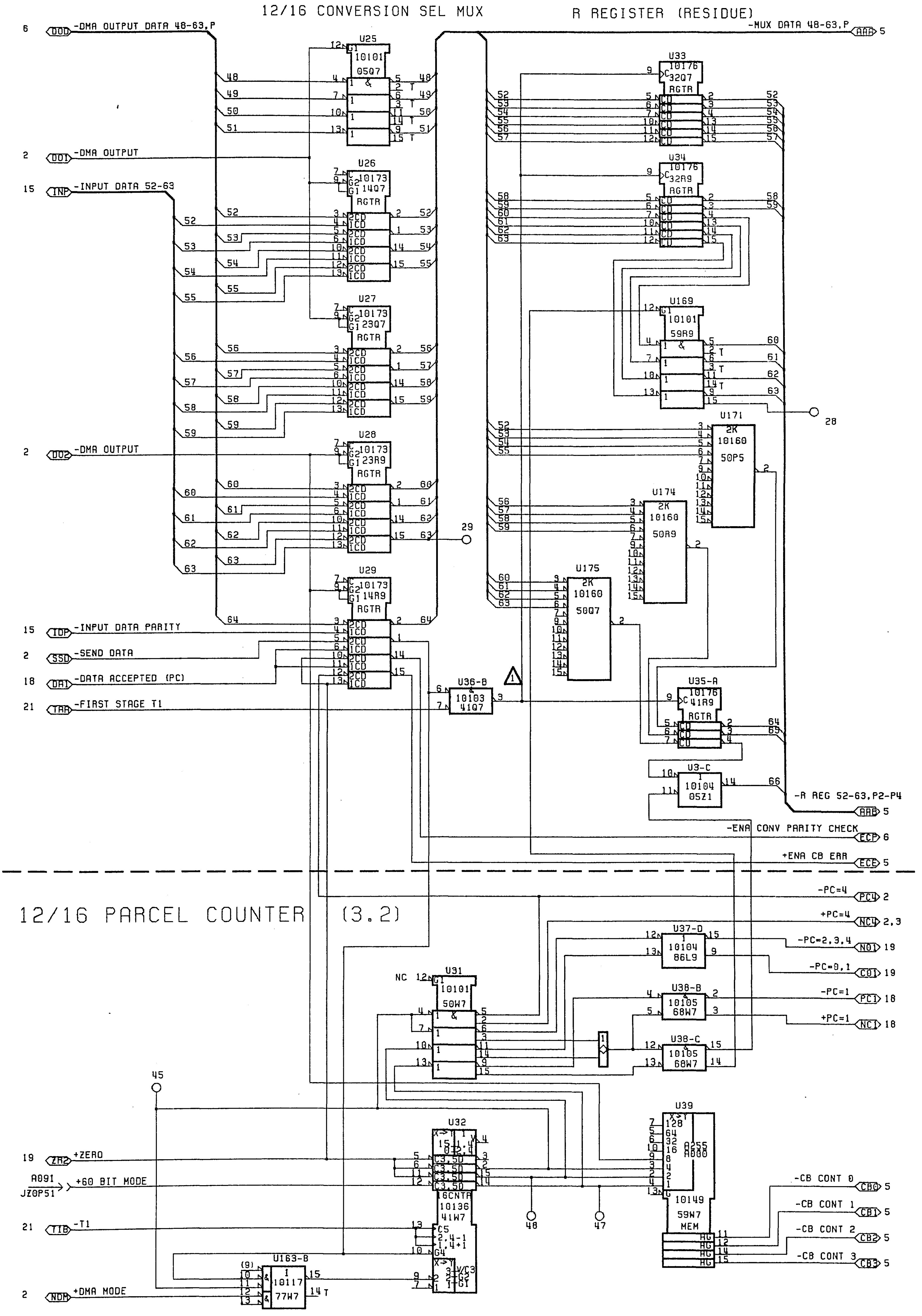


CONTROL DATA

170 DMA CHAN EXT I/F
OUTPUT RESYNC NETWORK
AND ADDRESS COUNTERS
TYPE 1KZH

	DWG NO.	DATE	REV
B	22132520	10/15/86	A
SHEET NO. 3	60462210	PAGE KZ-03	

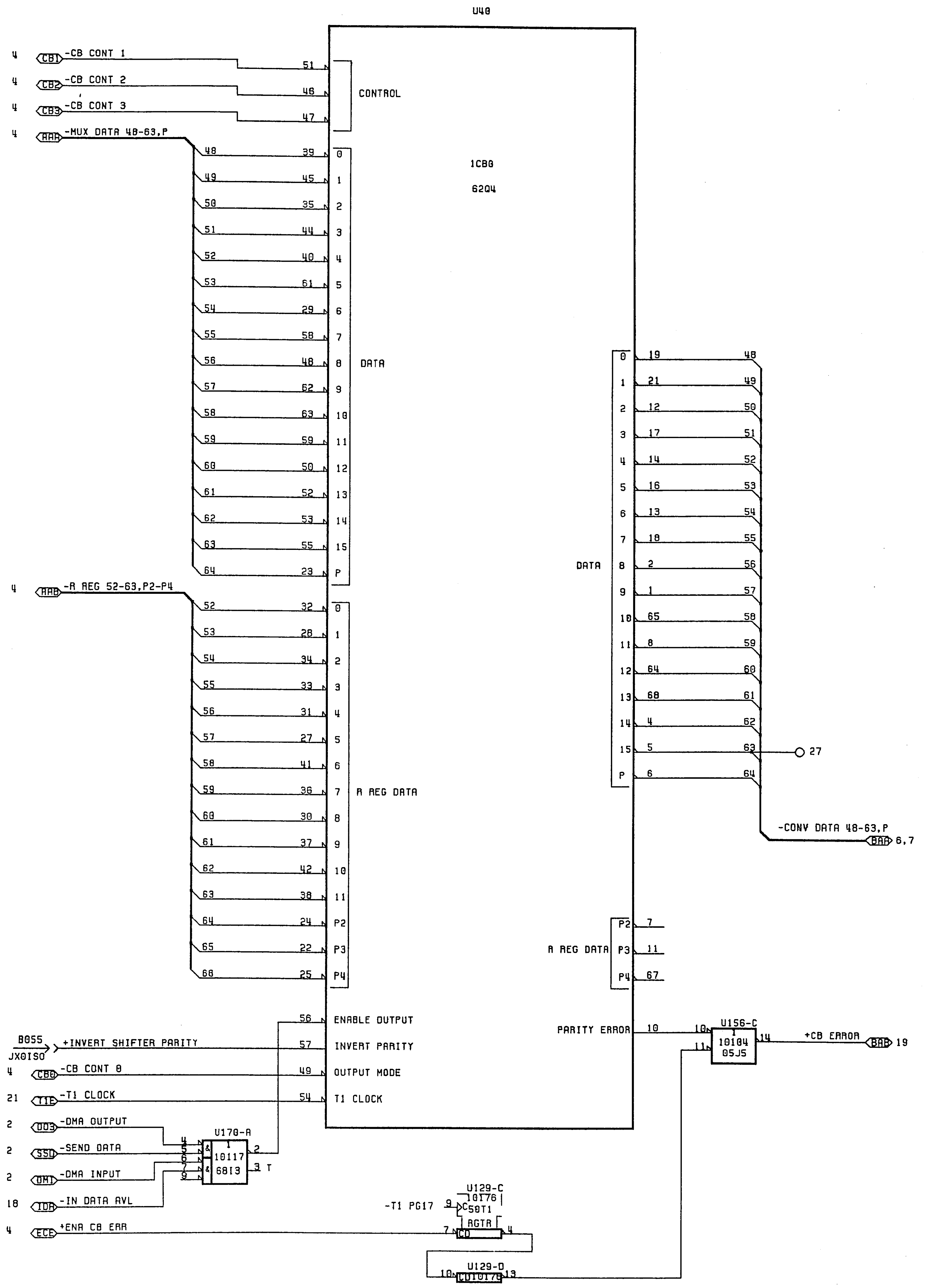
12/16 CONVERTER INPUT (3.2)



⚠ 12 INCHES MAXIMUM

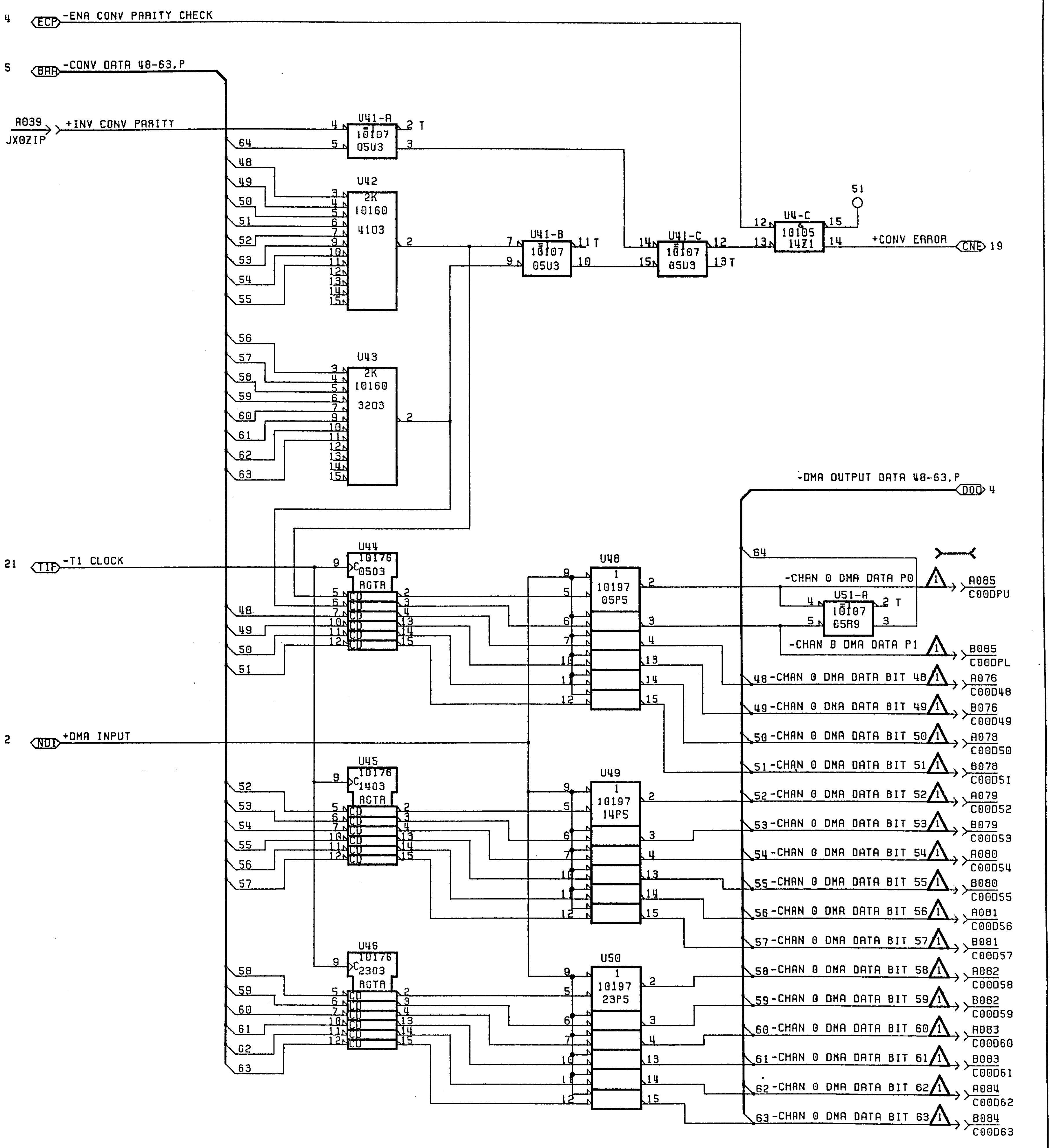
CONTROL DATA	170 DMA CHAN EXT I/F 12/16 CONVERTER INPUT 12/16 PARCEL COUNTER TYPE 1KZH	B	DWG NO. 22132520	DATE 12/16/86	REV B
		N	SHEET NO. 04	60462210	PAGE KZ-04

12/16 CONVERSION SHIFTER (3.2)



CONTROL DATA	170 DMA CHAN EXT I/F 12/16 CONVERSION SHIFTER TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
			SHEET NO. 05	60462210	PAGE KZ-05

DMA INPUT DATA PARITY CHECKER (3.2)

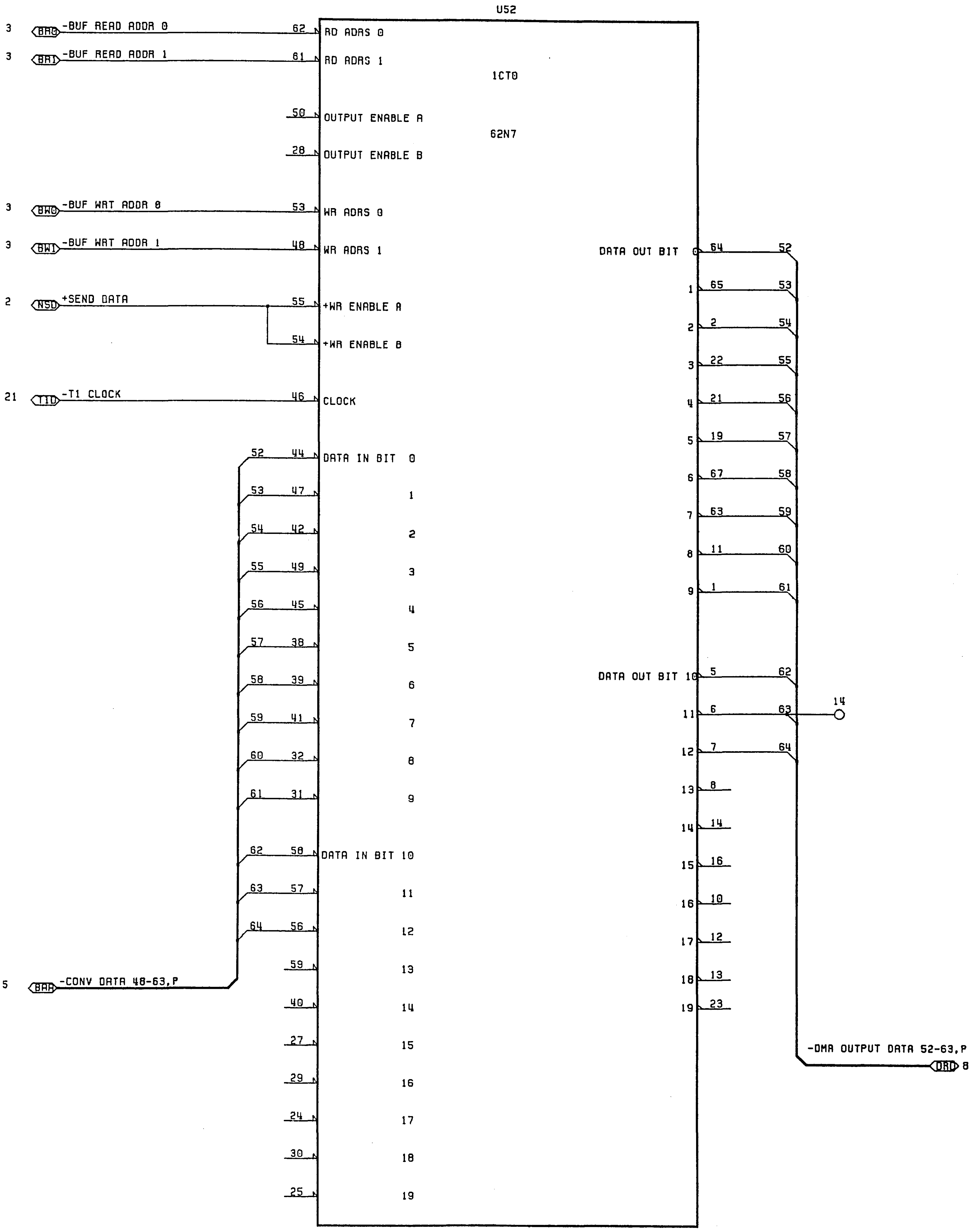


4 ECP -ENA CONV PARITY CHECK
5 BAR -CONV DATA 48-63.P
A039 +INV CONV PARITY
JX0ZIP
U41-A 10107 05U3
U42 2K 10160 4103
U43 2K 10160 3203
U41-B 10107 05U3
U41-C 10107 05U3
U4-C 10105 1471
51
+CONV ERROR CNE 19
-DMA OUTPUT DATA 48-63.P DOO 4
21 T1F -T1 CLOCK
U44 10176 0503 AGTR
U45 10176 1403 AGTR
U46 10176 2303 AGTR
2 NDI +DMA INPUT
U48 1 10197 05P5
U49 1 10197 14P5
U50 1 10197 23P5
U51-A 10107 05R9
-CHAN 0 DMA DATA P0 A085 C00DPU
-CHAN 0 DMA DATA P1 B085 C00DPL
-CHAN 0 DMA DATA BIT 48 A076 C00D48
-CHAN 0 DMA DATA BIT 49 B076 C00D49
-CHAN 0 DMA DATA BIT 50 A078 C00D50
-CHAN 0 DMA DATA BIT 51 B078 C00D51
-CHAN 0 DMA DATA BIT 52 A079 C00D52
-CHAN 0 DMA DATA BIT 53 B079 C00D53
-CHAN 0 DMA DATA BIT 54 A080 C00D54
-CHAN 0 DMA DATA BIT 55 B080 C00D55
-CHAN 0 DMA DATA BIT 56 A081 C00D56
-CHAN 0 DMA DATA BIT 57 B081 C00D57
-CHAN 0 DMA DATA BIT 58 A082 C00D58
-CHAN 0 DMA DATA BIT 59 B082 C00D59
-CHAN 0 DMA DATA BIT 60 A083 C00D60
-CHAN 0 DMA DATA BIT 61 B083 C00D61
-CHAN 0 DMA DATA BIT 62 A084 C00D62
-CHAN 0 DMA DATA BIT 63 B084 C00D63

⚠1 TERMINATE AT THE FARTHEST POINT FROM THE CONNECTOR PIN.

CONTROL DATA
170 DMA CHAN EXT I/F
DMA INPUT DATA PARITY CHECKER
TYPE 1KZH
B
DWG NO. 22132520
DATE 10/15/86
REV A
N SHEET NO. 06 60462210
PAGE KZ-06

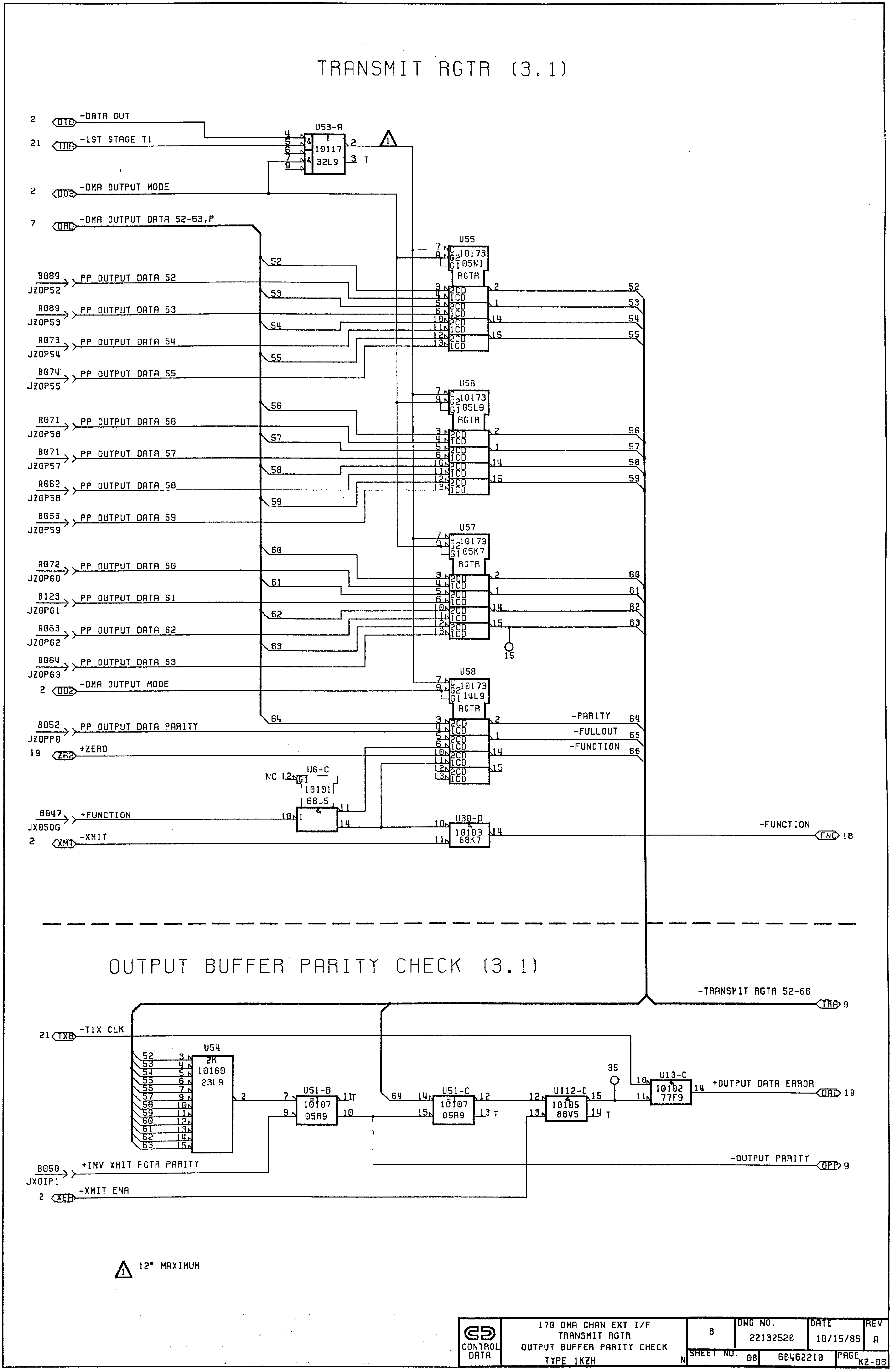
OUTPUT RESYNC BUFFER (3.1)



CONTROL DATA

170 DMA CHAN EXT I/F
OUTPUT RESYNC BUFFER
TYPE 1KZH

	DWG NO.	DATE	REV
B	22132520	10/15/86	A
SHEET NO. 07	60462210	PAGE KZ-07	


TRANSMIT RGTR (3.1)

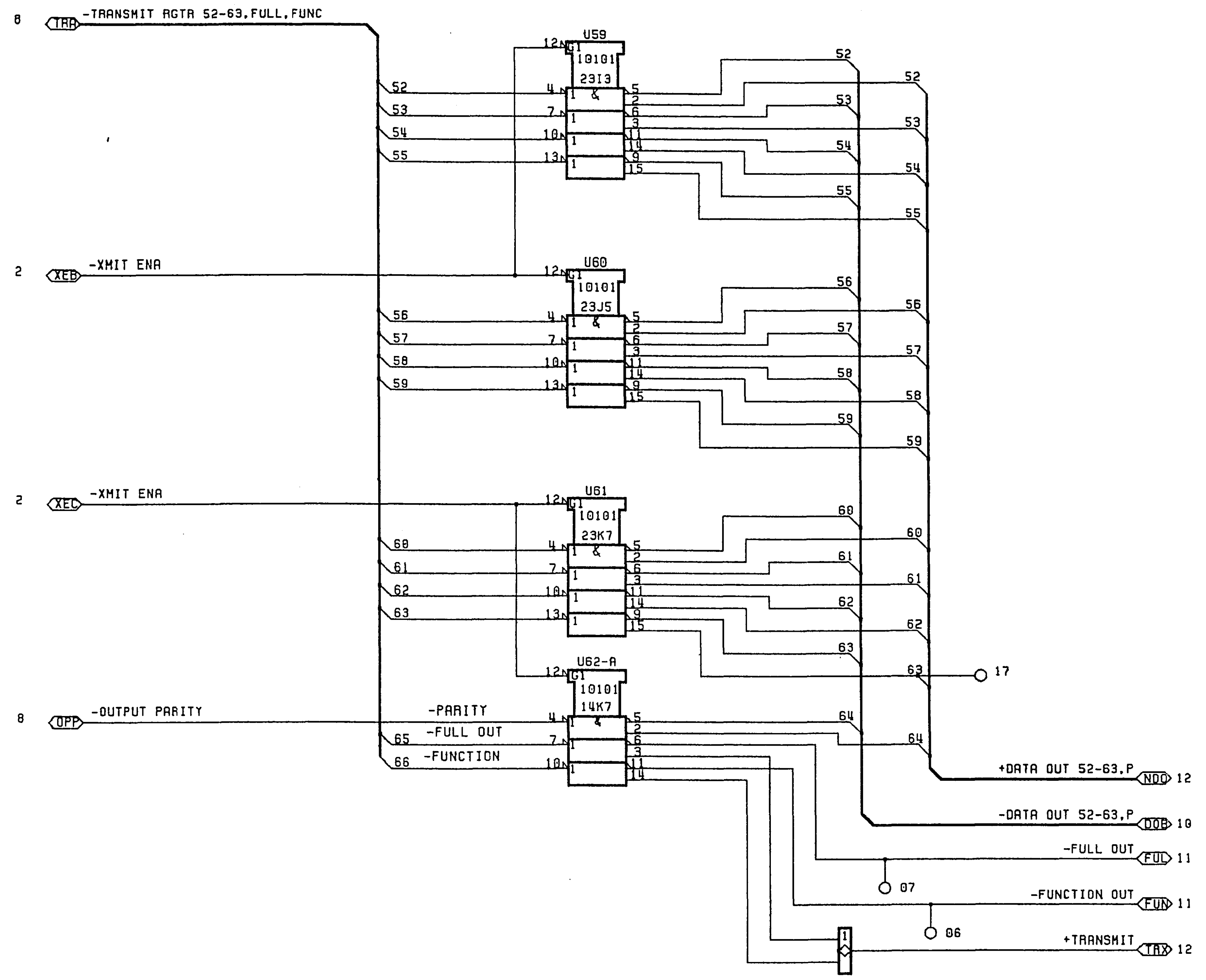
OUTPUT BUFFER PARITY CHECK (3.1)

CONTROL DATA

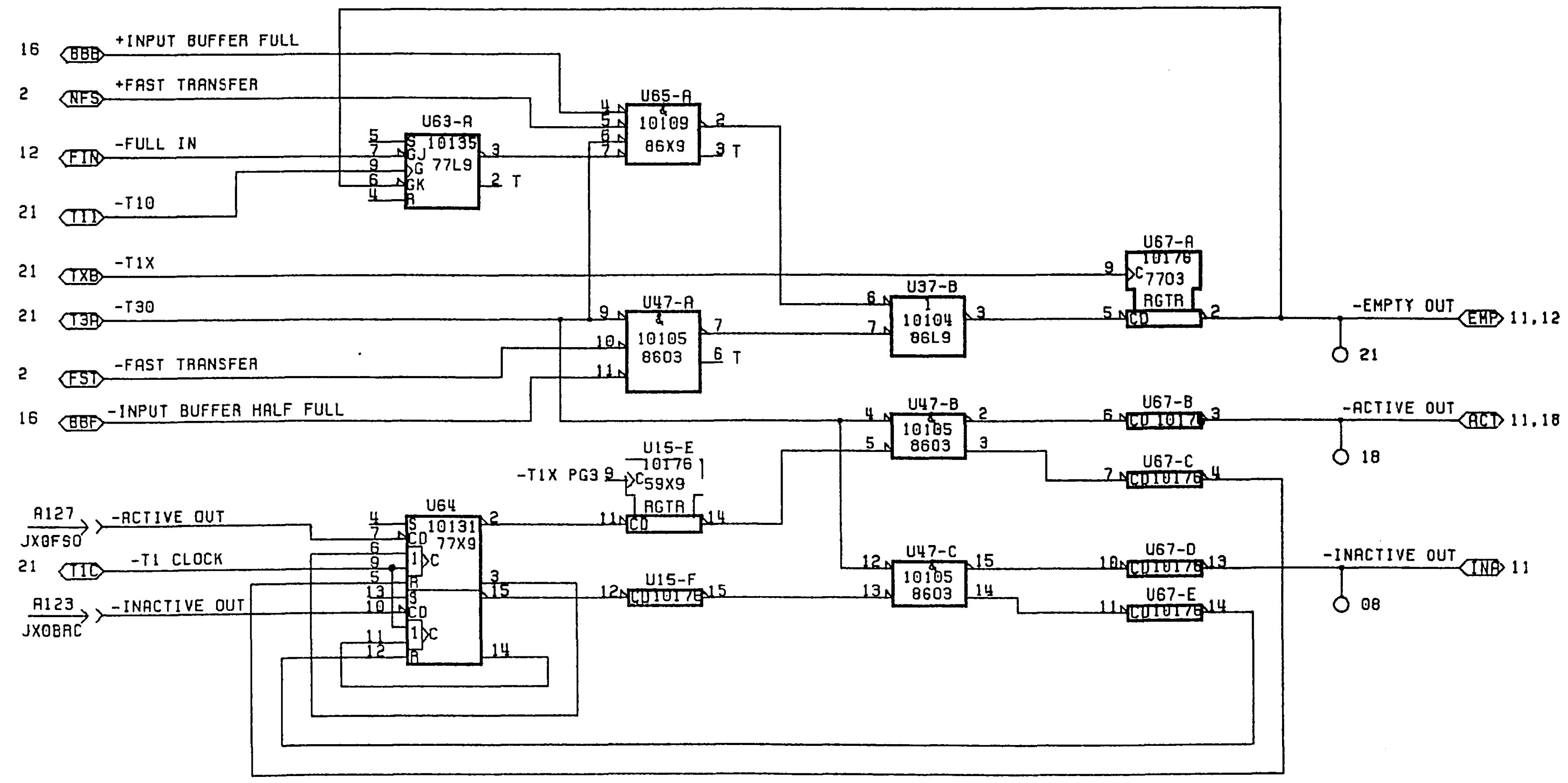
170 DMA CHAN EXT I/F
TRANSMIT RGTR
OUTPUT BUFFER PARITY CHECK
TYPE 1KZH

	DWG NO.	DATE	REV
B	22132520	10/15/86	A
SHEET NO. 08	60462210	PAGE KZ-08	

TRANSMIT ENABLES (3.1)

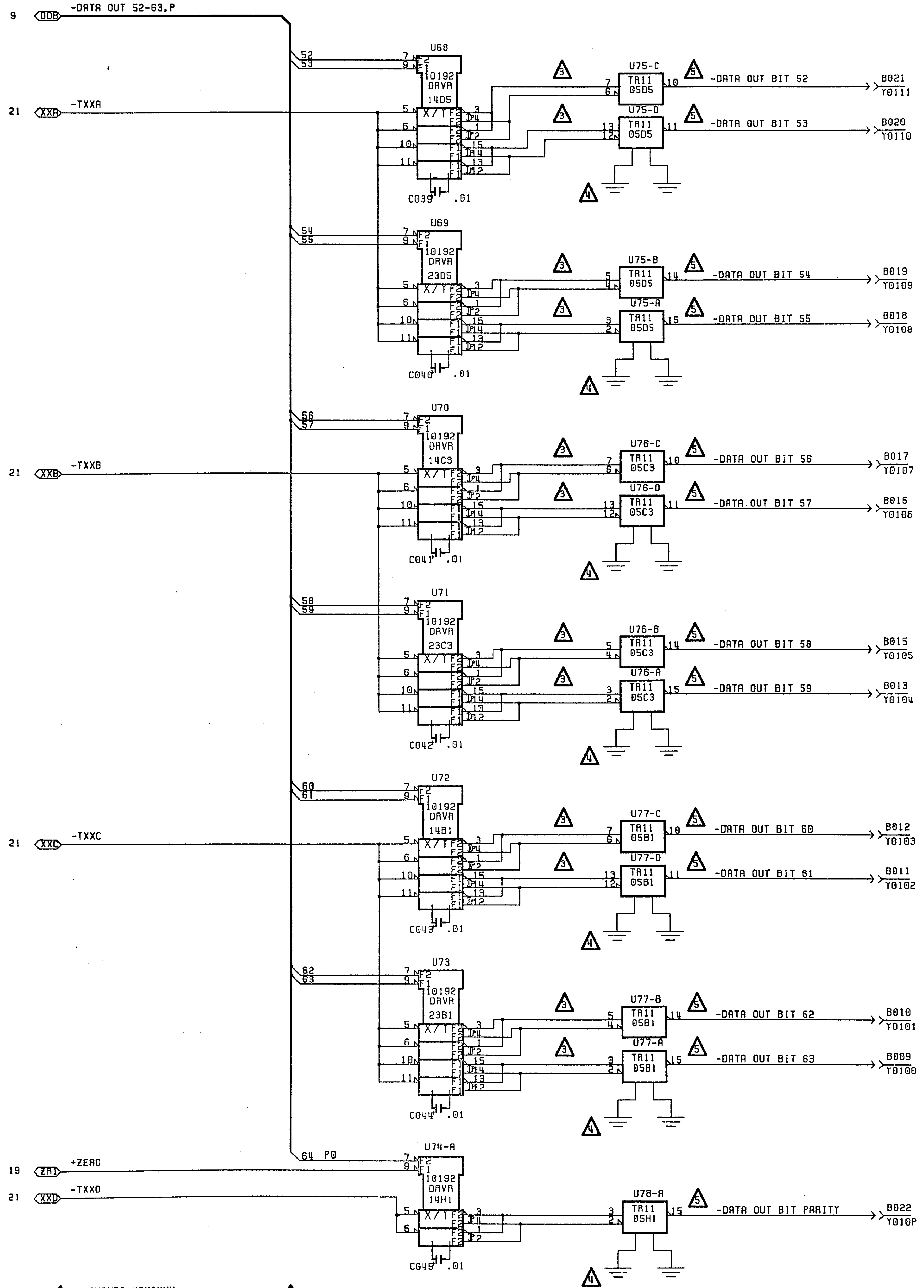


EMPTY, ACTIVE & INACTIVE OUT NETWORKS (3.1)



CONTROL DATA	170 DMA CHAN EXT I/F TRANSMIT ENABLES, EMPTY, ACTIVE, AND INACTIVE OUT NETWORKS TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
		SHEET NO. 09	60462210	PAGE KZ-09	

DATA OUT TRANSMITTERS (3.1)



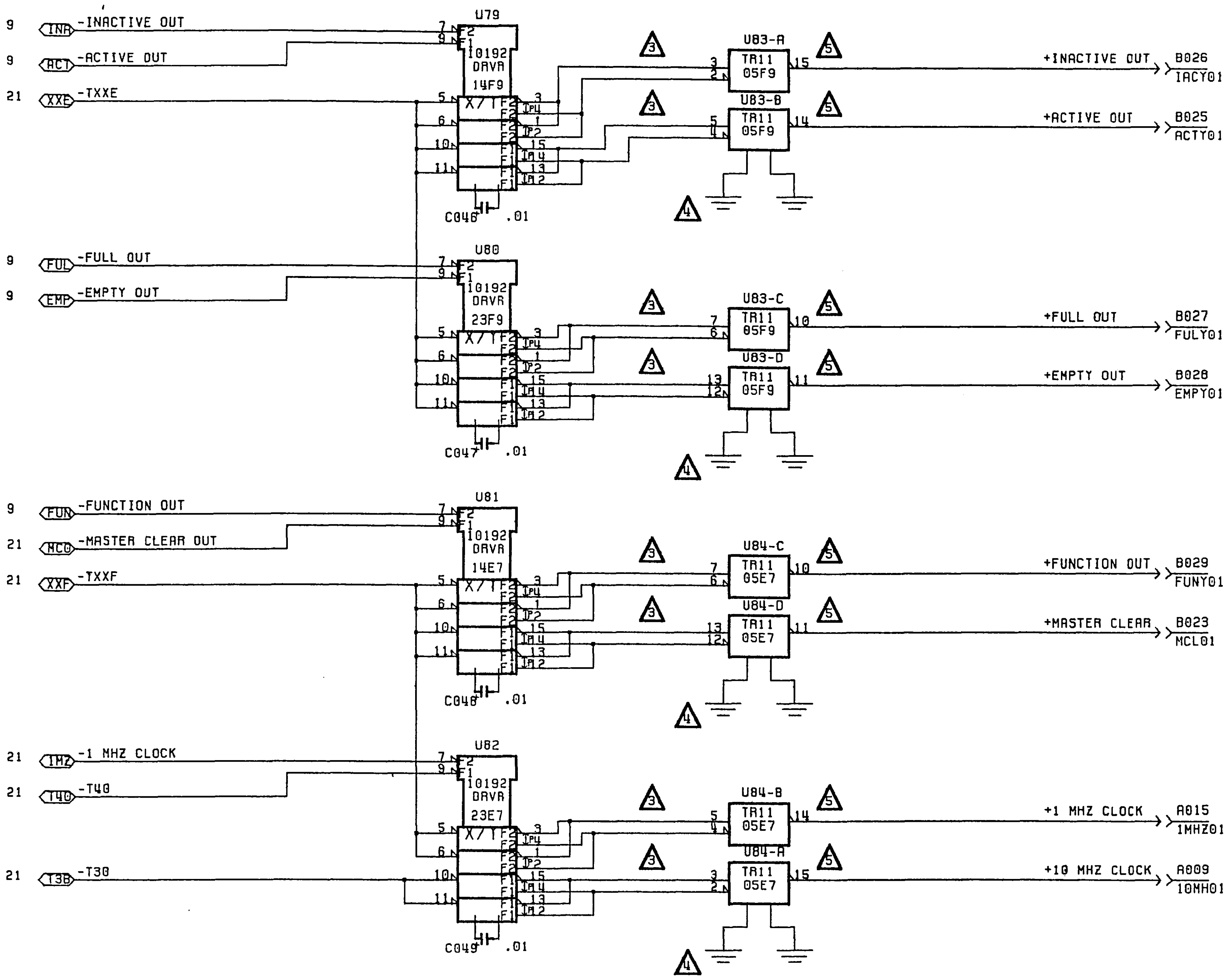
△3 3 INCHES MAXIMUM BETWEEN 10192 AND TR11 CHIPS

△5 4.5 INCHES MAXIMUM

△4 GND PINS 1 AND 8 OF THE TR11 CHIPS SHOULD BE GROUNDED AT PIN 16 OF THEIR RESPECTIVE 10192 CHIP WITH MINIMUM FOIL WIDTH OF .032 INCHES

CONTROL DATA
170 DMA CHAN EXT I/F
DATA OUT TRANSMITTERS
TYPE 1KZH
B
DWG NO. 22132520
DATE 10/15/86
REV A
N
SHEET NO. 10
60462210
PAGE KZ-10

CONTROL SIGNAL TRANSMITTERS (3.1)



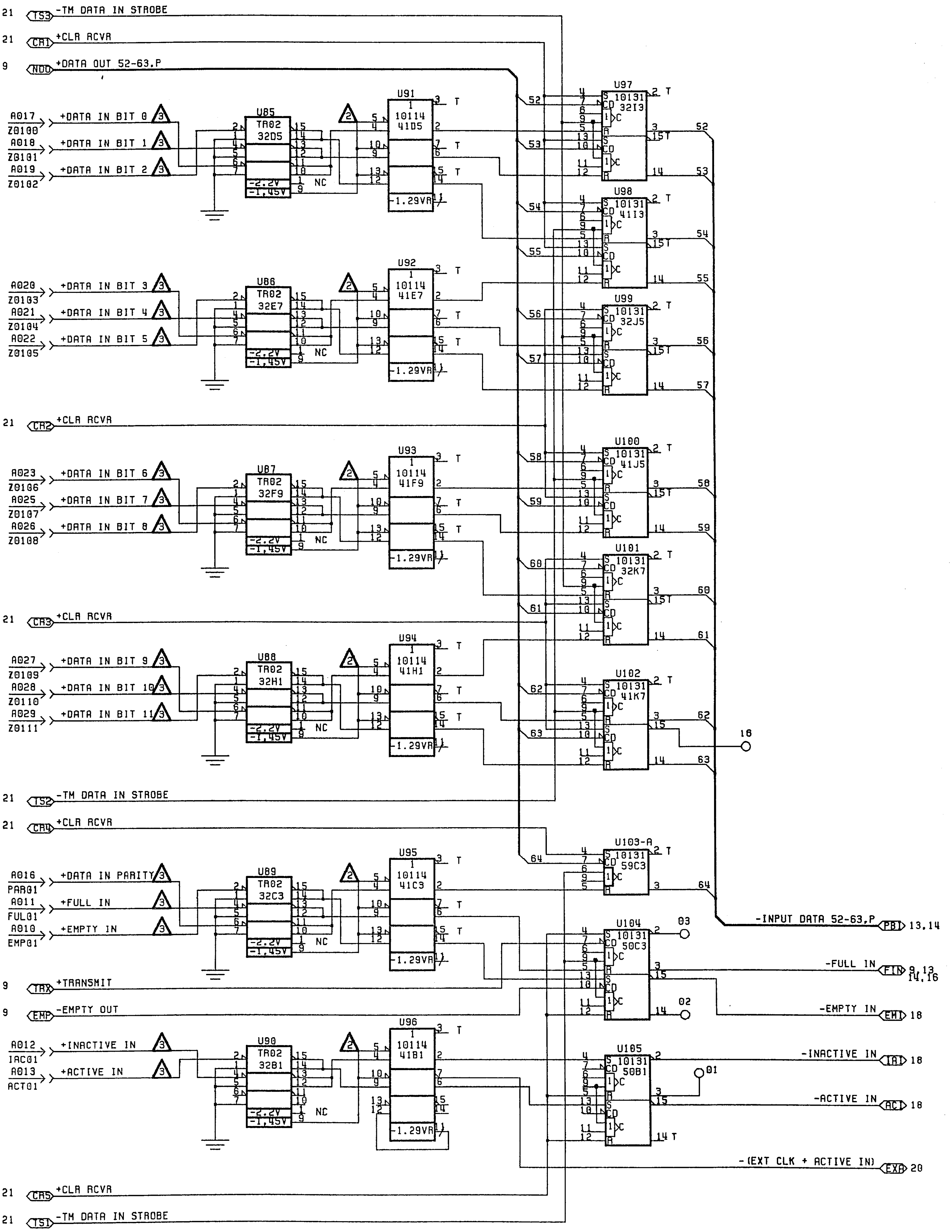
3 — 3 INCHES MAXIMUM BETWEEN 10192 AND TR11 CHIPS

4 — GND PINS 1 AND 8 OF THE TR11 CHIPS SHOULD BE GROUNDED AT PIN 16 OF THEIR RESPECTIVE 10192 CHIP WITH MINIMUM FOIL WIDTH OF .032 INCHES

5 — 4.5 INCHES MAXIMUM

CONTROL DATA	170 DMA CHAN EXT I/F CONTROL SIGNAL TRANSMITTERS TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
			SHEET NO. 11	60462210	PAGE KZ-11

INPUT RECEIVERS AND DESKEW RGTR (3.4)

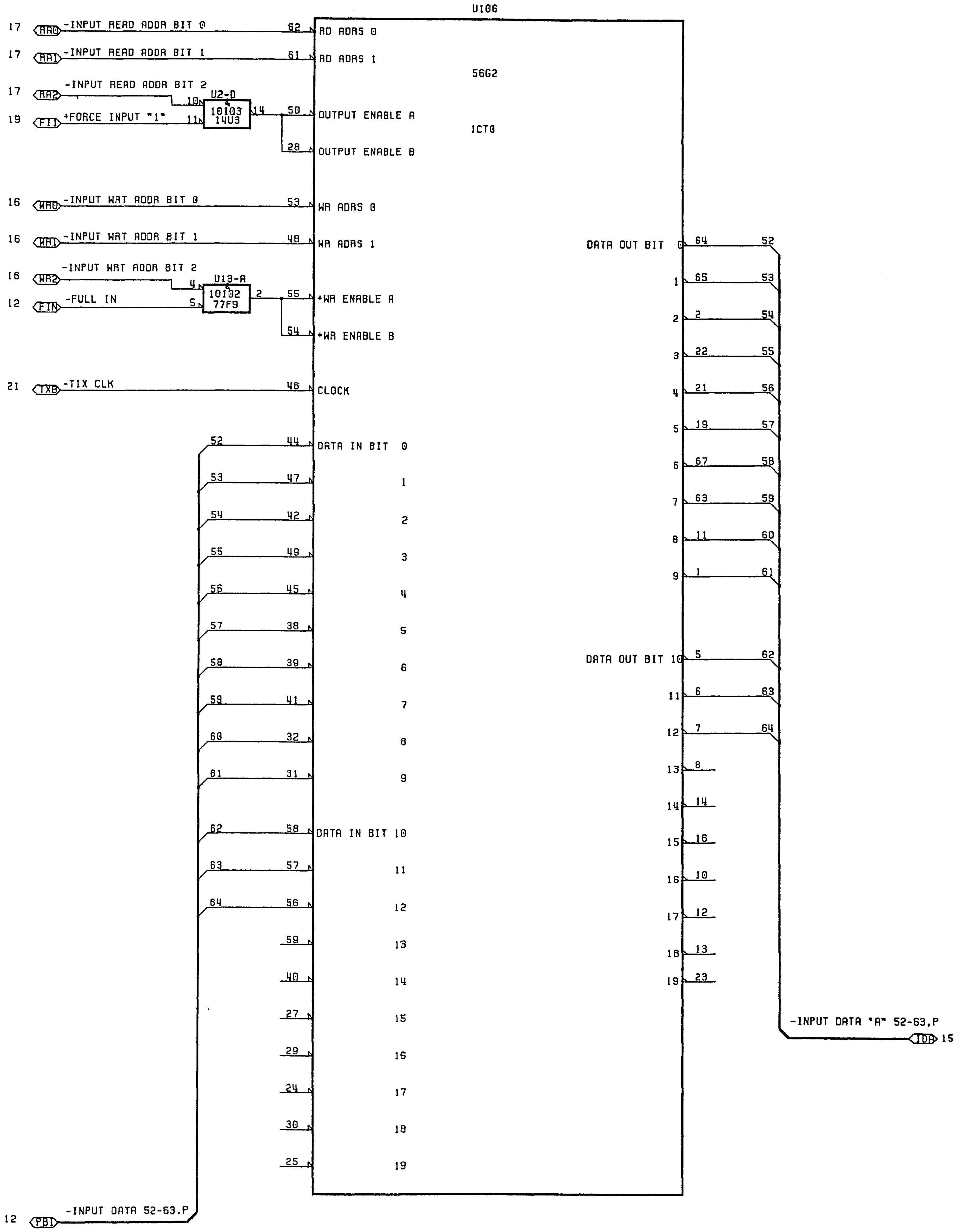


2 2 INCH MAX BETWEEN TR02 AND 10114

3 4.5 INCH MAX

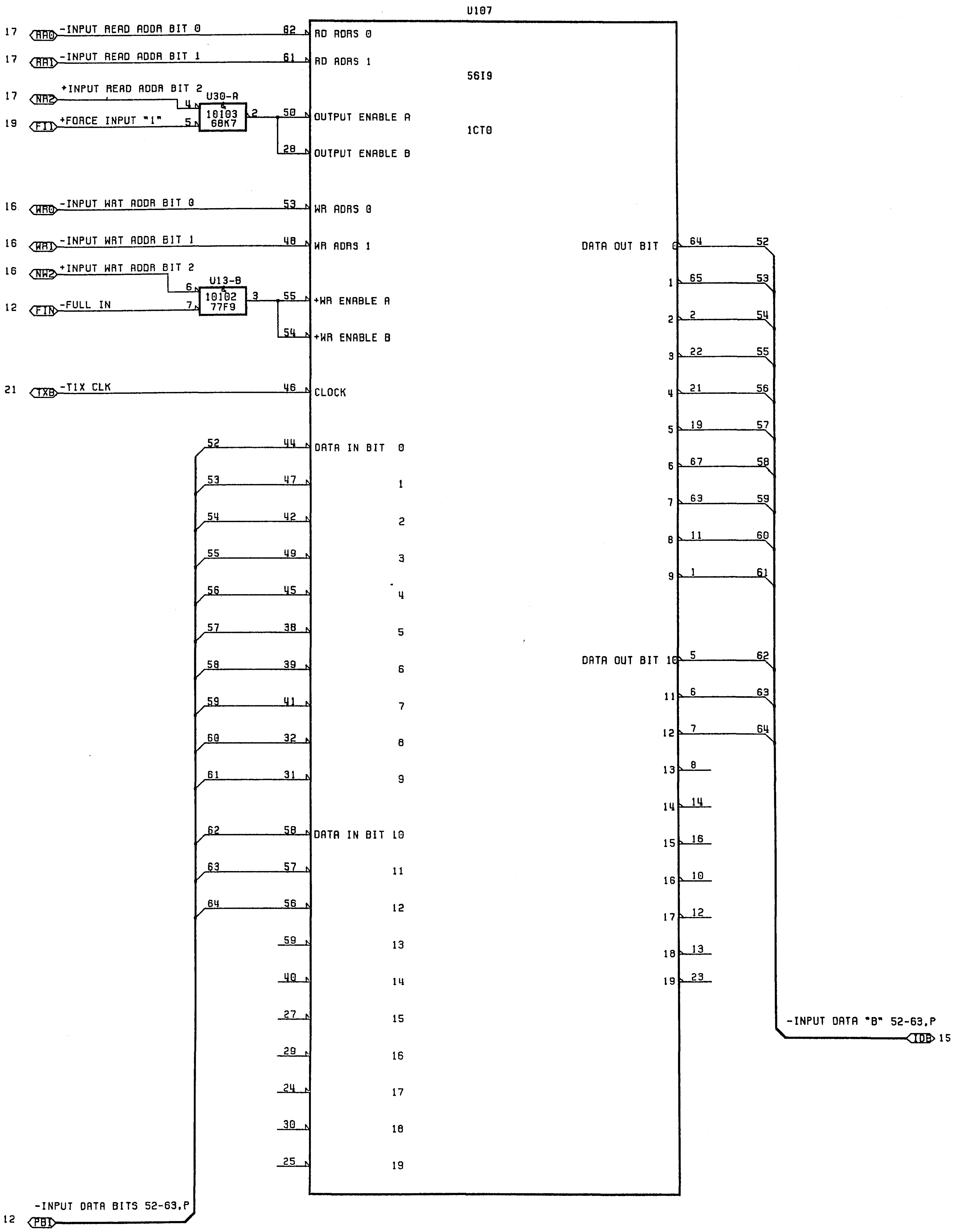
CONTROL DATA
170 DMA CHAN EXT I/F
INPUT RECEIVERS AND DESKEW RGTR
TYPE 1KZH
B
DWG NO. 22132520
DATE 10/15/86
REV A
SHEET NO. 12
60462210
PAGE KZ-12

INPUT BUFFER "CHIP A" (3.4)

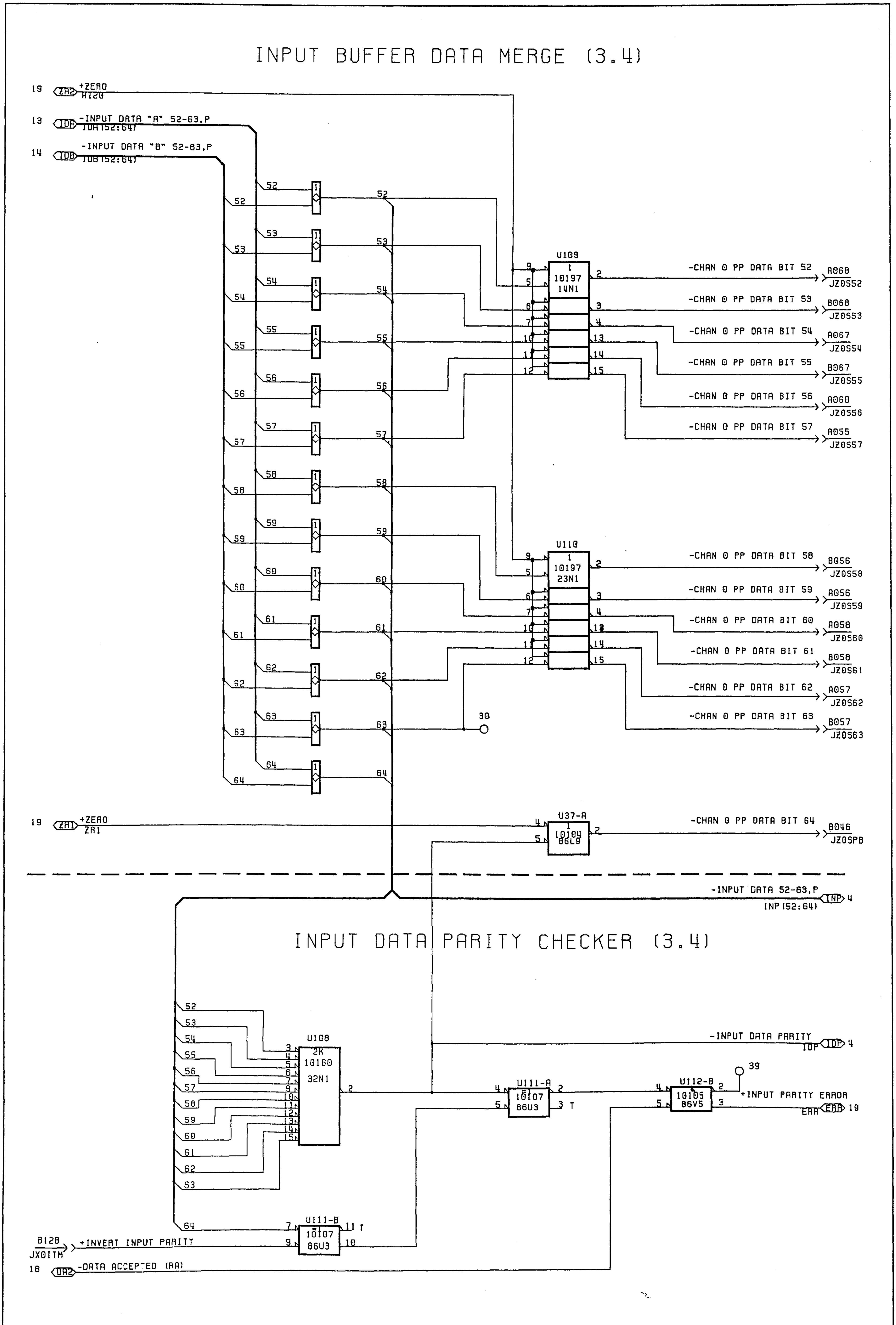


CONTROL DATA	170 DMA CHAN EXT I/F INPUT BUFFER "CHIP A" TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
		N	SHEET NO. 13	60462210	PAGE KZ-13

INPUT BUFFER "CHIP B" (3.4)



CONTROL DATA	170 DMA CHAN EXT I/F INPUT BUFFER "CHIP B" TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
		SHEET NO. 14	60462210	PAGE KZ-14	

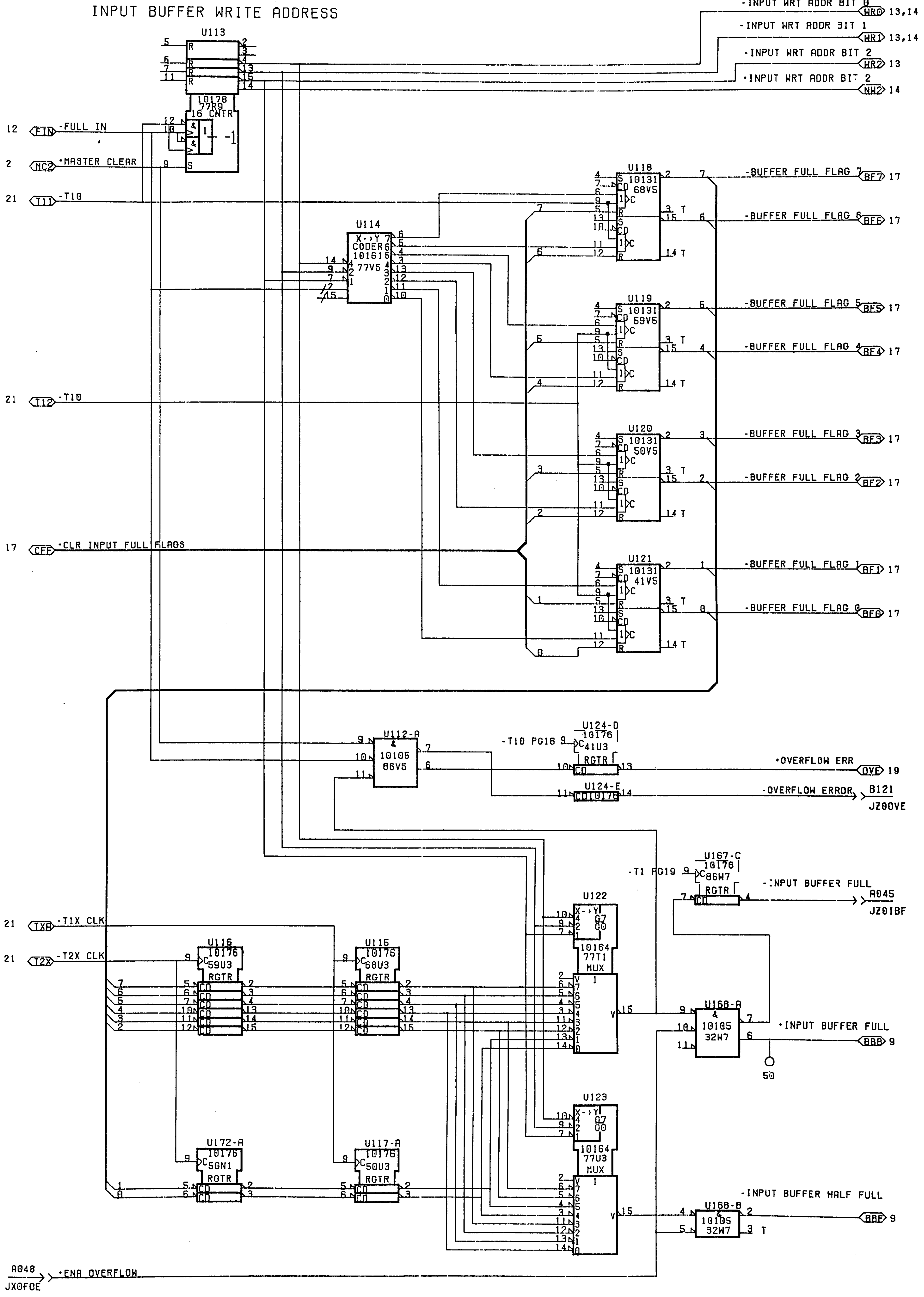

INPUT BUFFER DATA MERGE (3.4)
19 ZR2 +ZERO ZR2
13 IDA -INPUT DATA "A" 52-63,P IDA(52:64)
14 IDB -INPUT DATA "B" 52-63,P IDB(52:64)
52 53 54 55 56 57 58 59 60 61 62 63 64
U109 1 10197 14N1
-CHAN 0 PP DATA BIT 52 A068 JZ0S52
-CHAN 0 PP DATA BIT 53 B068 JZ0S53
-CHAN 0 PP DATA BIT 54 A067 JZ0S54
-CHAN 0 PP DATA BIT 55 B067 JZ0S55
-CHAN 0 PP DATA BIT 56 A060 JZ0S56
-CHAN 0 PP DATA BIT 57 A055 JZ0S57
U110 1 10197 23N1
-CHAN 0 PP DATA BIT 58 B056 JZ0S58
-CHAN 0 PP DATA BIT 59 A056 JZ0S59
-CHAN 0 PP DATA BIT 60 A058 JZ0S60
-CHAN 0 PP DATA BIT 61 B058 JZ0S61
-CHAN 0 PP DATA BIT 62 A057 JZ0S62
-CHAN 0 PP DATA BIT 63 B057 JZ0S63
30
19 ZR1 +ZERO ZR1
U37-A 1 10104 86L9
-CHAN 0 PP DATA BIT 64 B046 JZ0SPB
-INPUT DATA 52-63,P INP(52:64) INP 4
INPUT DATA PARITY CHECKER (3.4)
U108 2K 10160 32N1
-INPUT DATA PARITY IDP IDP 4
39
U111-A 10107 86U3
U112-B 10105 86V5
+INPUT PARITY ERROR ERR ERR 19
U111-B 10107 86U3
B128 JX0ITM +INVERT INPUT PARITY
18 DA2 -DATA ACCEPTED (AA)

CONTROL DATA

170 DMA CHAN EXT I/F
INPUT BUFFER DATA MERGE
INPUT DATA PARITY CHECKER
TYPE 1KZH

B	DWG NO.	DATE	REV
	22132520	10/15/86	A
SHEET NO. 15	60462210	PAGE KZ-15	

INPUT BUFFER WRITE CONTROL (3.3)


INPUT BUFFER WRITE ADDRESS
U113
10178
77R9
16 CNTR
12 FIN -FULL IN
2 MC2 •MASTER CLEAR
21 T11 -T10
21 T12 -T10
17 CFF •CLR INPUT FULL FLAGS
21 T1X -T1X CLK
21 T2X -T2X CLK
A048 JX0FOE •ENA OVERFLOW
-INPUT WRT ADDR BIT 0 WR0 13,14
-INPUT WRT ADDR BIT 1 WR1 13,14
-INPUT WRT ADDR BIT 2 WR2 13
•INPUT WRT ADDR BIT 2 NW2 14
U114
X->Y
CODER
10161
77V5
U118 10131 68V5
U119 10131 59V5
U120 10131 50V5
U121 10131 41V5
-BUFFER FULL FLAG 7 BF7 17
-BUFFER FULL FLAG 6 BF6 17
-BUFFER FULL FLAG 5 BF5 17
-BUFFER FULL FLAG 4 BF4 17
-BUFFER FULL FLAG 3 BF3 17
-BUFFER FULL FLAG 2 BF2 17
-BUFFER FULL FLAG 1 BF1 17
-BUFFER FULL FLAG 0 BF0 17
U112-A & 10105 86V5
U124-D 10176 41U3 RGTR
-T10 PG18
U124-E 10176
•OVERFLOW ERR OVE 19
-OVERFLOW ERROR B121 JZ0OVE
U167-C 10176 86W7 RGTR
-T1 PG19
-INPUT BUFFER FULL A045 JZ0IBF
U122 X->Y G7 G0 10164 77T1 MUX
U123 X->Y G7 G0 10164 77U3 MUX
U116 10176 59U3 RGTR
U115 10176 68U3 RGTR
U172-A 10176 50N1 RGTR
U117-A 10176 50U3 RGTR
U168-A & 10105 32W7
•INPUT BUFFER FULL BBB 9
50
-INPUT BUFFER HALF FULL
U168-B & 10105 32W7
BBF 9

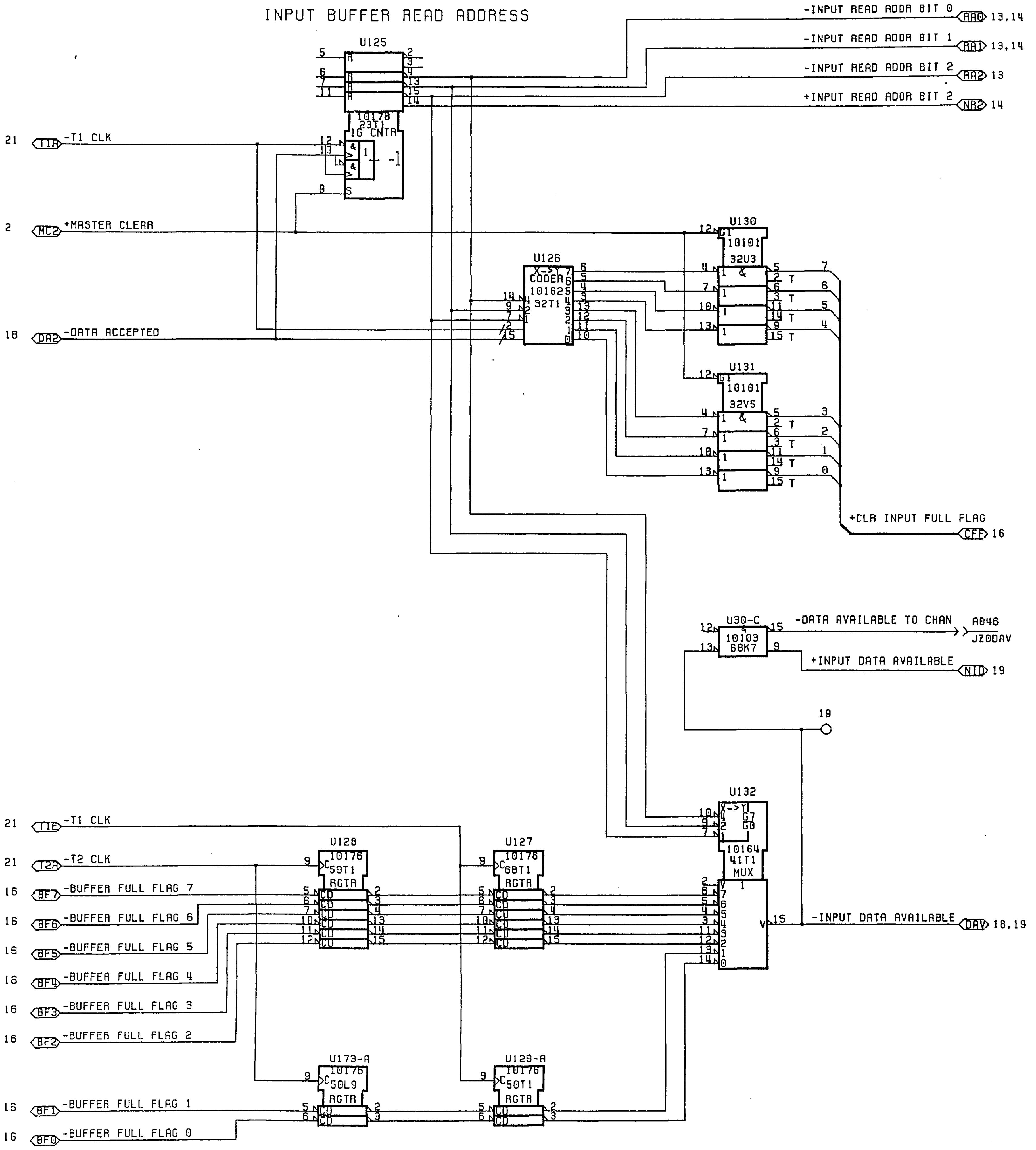
CONTROL DATA

170 DMA CHAN EXT I/F
INPUT BUFFER WRITE CONTROL
TYPE 1KZH

B

DWG NO. 22132520
DATE 10/19/87
REV D
SHEET NO. 16
60462210
PAGE KZ-16

INPUT BUFFER READ CONTROL (3.3)



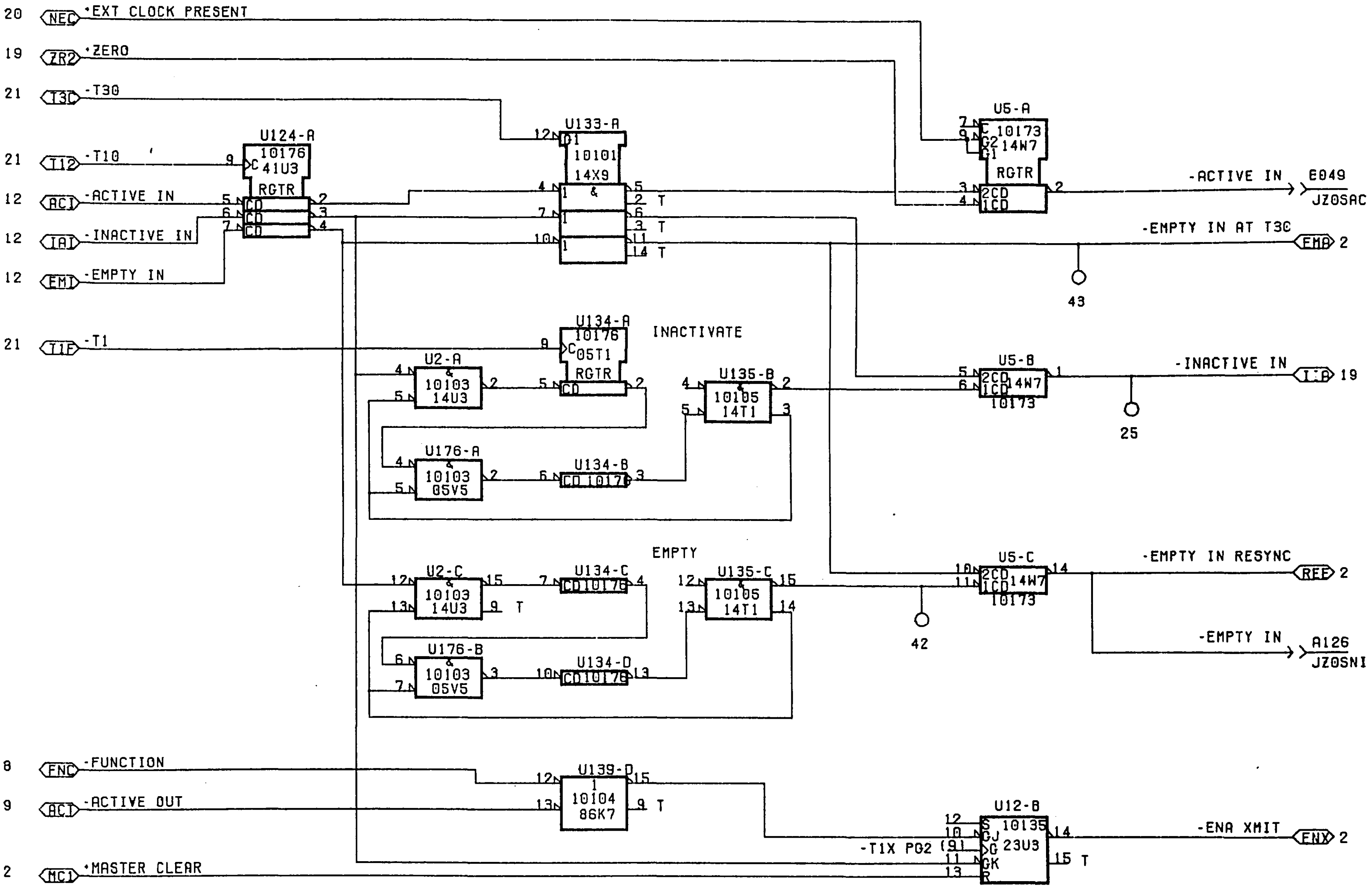
INPUT BUFFER READ ADDRESS
U125
10178
23T1
16 CNTR
21 -T1 CLK T1A
2 +MASTER CLEAR MC2
18 -DATA ACCEPTED DA2
-INPUT READ ADDR BIT 0 RA0 13,14
-INPUT READ ADDR BIT 1 RA1 13,14
-INPUT READ ADDR BIT 2 RA2 13
+INPUT READ ADDR BIT 2 NR2 14
U126
X->Y
CODER
10162
32T1
U130
10101
32U3
U131
10101
32V5
+CLR INPUT FULL FLAG CFF 16
U30-C
10103
60K7
-DATA AVAILABLE TO CHAN A046 JZ0DAV
+INPUT DATA AVAILABLE NID 19
19
U132
X->Y
G7
G0
10164
41T1
MUX
-INPUT DATA AVAILABLE DAV 18,19
21 -T1 CLK T1E
21 -T2 CLK T2A
16 -BUFFER FULL FLAG 7 BF7
16 -BUFFER FULL FLAG 6 BF6
16 -BUFFER FULL FLAG 5 BF5
16 -BUFFER FULL FLAG 4 BF4
16 -BUFFER FULL FLAG 3 BF3
16 -BUFFER FULL FLAG 2 BF2
16 -BUFFER FULL FLAG 1 BF1
16 -BUFFER FULL FLAG 0 BF0
U128
10176
59T1
RGTR
U127
10176
60T1
RGTR
U173-A
10176
50L9
RGTR
U129-A
10176
50T1
RGTR

CONTROL DATA

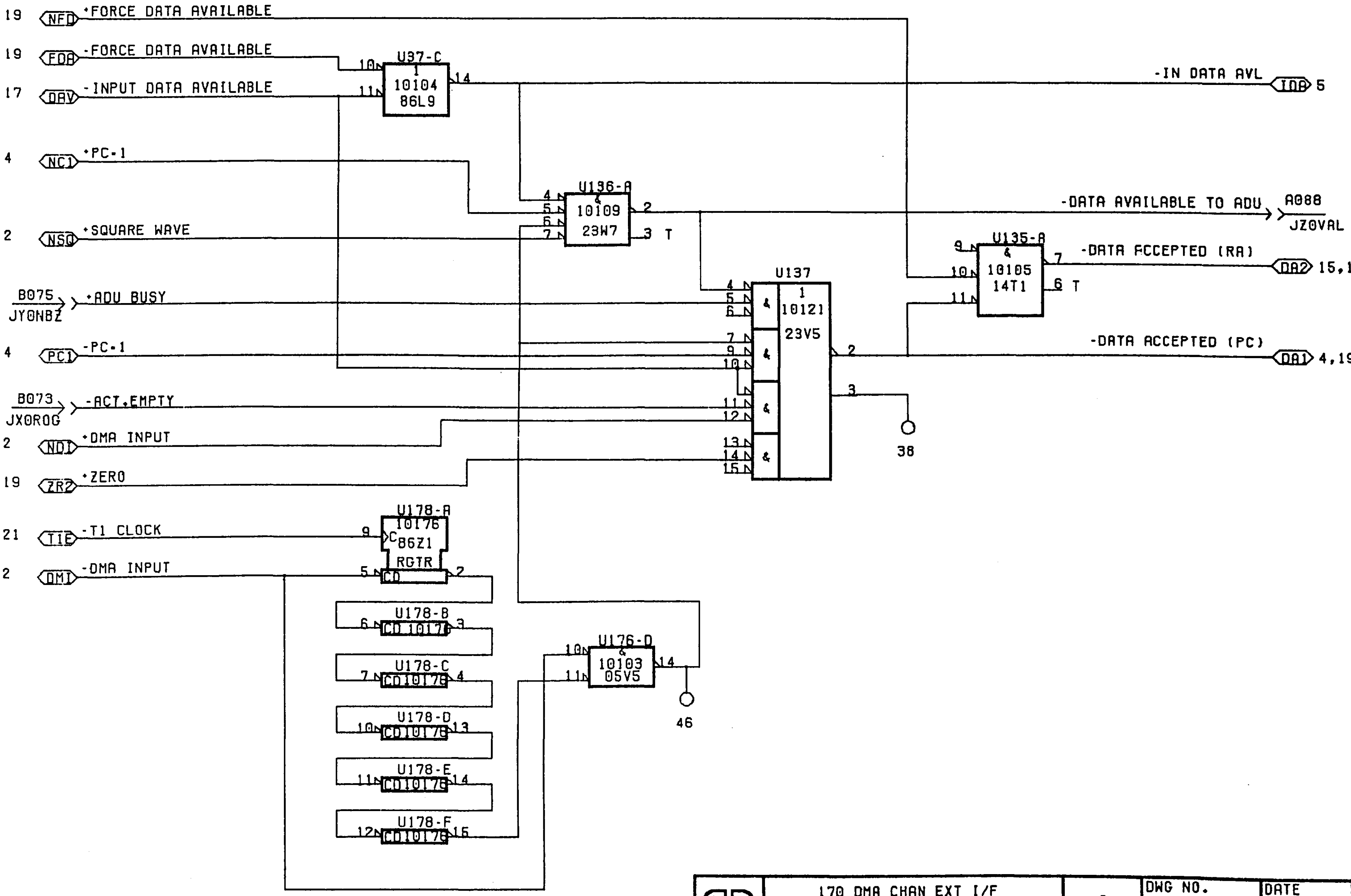
170 DMA CHAN EXT I/F
INPUT BUFFER READ CONTROL
TYPE 1KZH

B	DWG NO. 22132520	DATE 10/15/86	REV A
SHEET NO. 17	60462210	PAGE KZ-17	

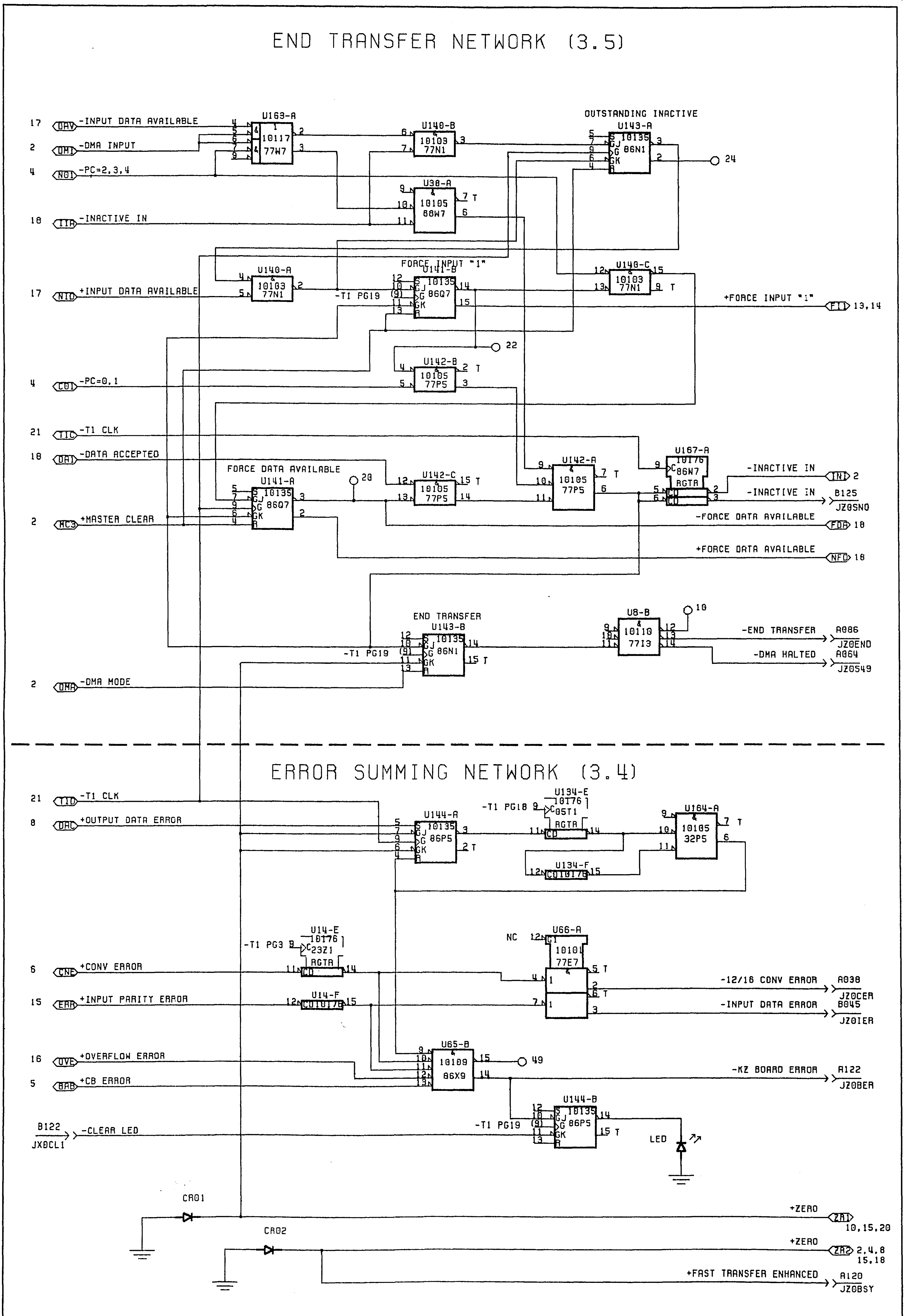
CONTROL IN RESYNC (3.5)



DATA ACCEPT NETWORK (3.2)



CONTROL DATA	170 DMA CHAN EXT I/F INPUT CONTROL SIGNAL RESYNC DATA ACCEPT NETWORK TYPE 1KZH	B	DWG NO. 22132520	DATE 10/19/87	REV D
		SHEET NO. 18	60462210	PAGE KZ-18	

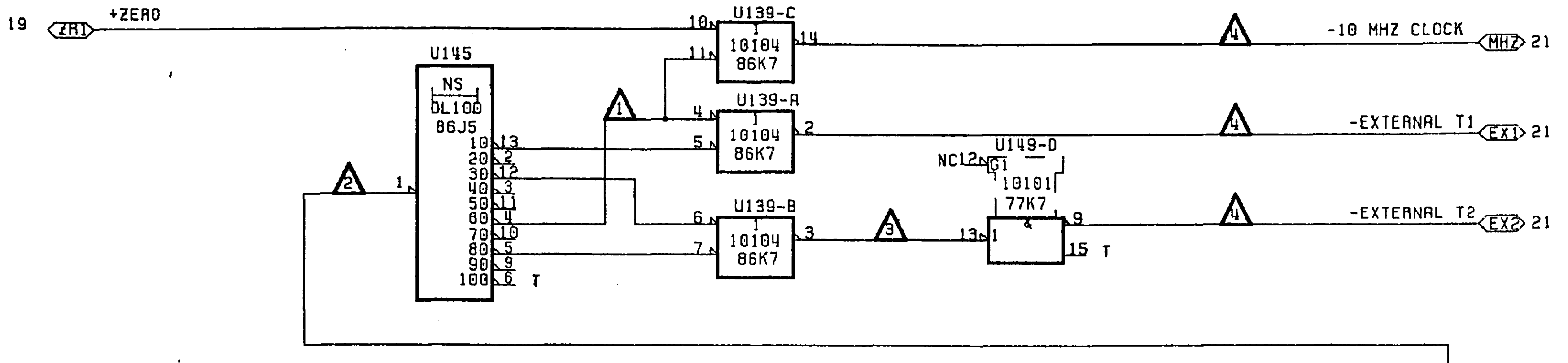


CONTROL DATA

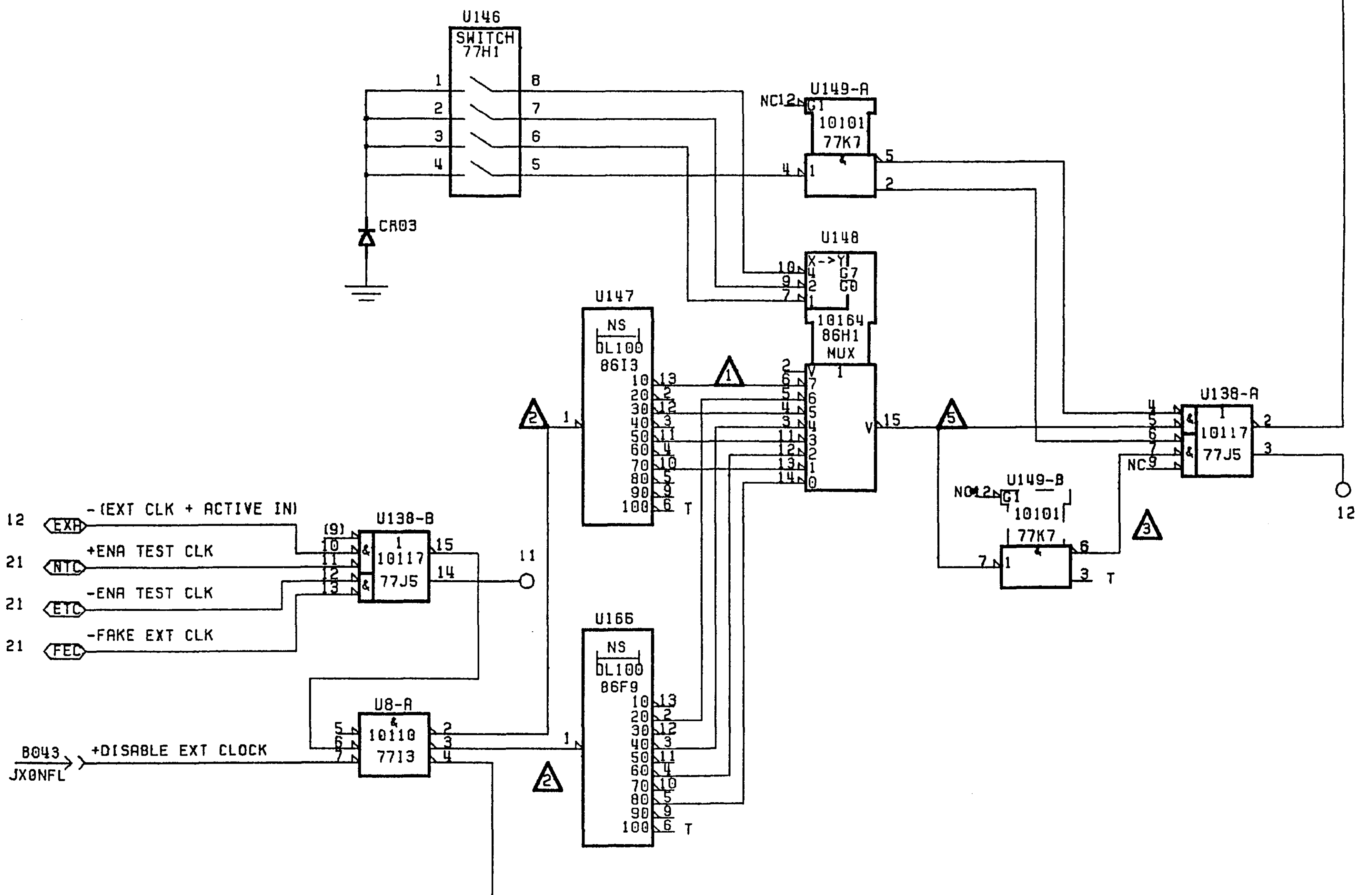
170 DMA CHAN EXT I/F
END TRANSFER NETWORK
ERROR SUMMING NETWORK
TYPE 1KZH

B	DWG NO. 22132520	DATE 10/15/86	REV A
SHEET NO. 19	60462210	PAGE KZ-19	

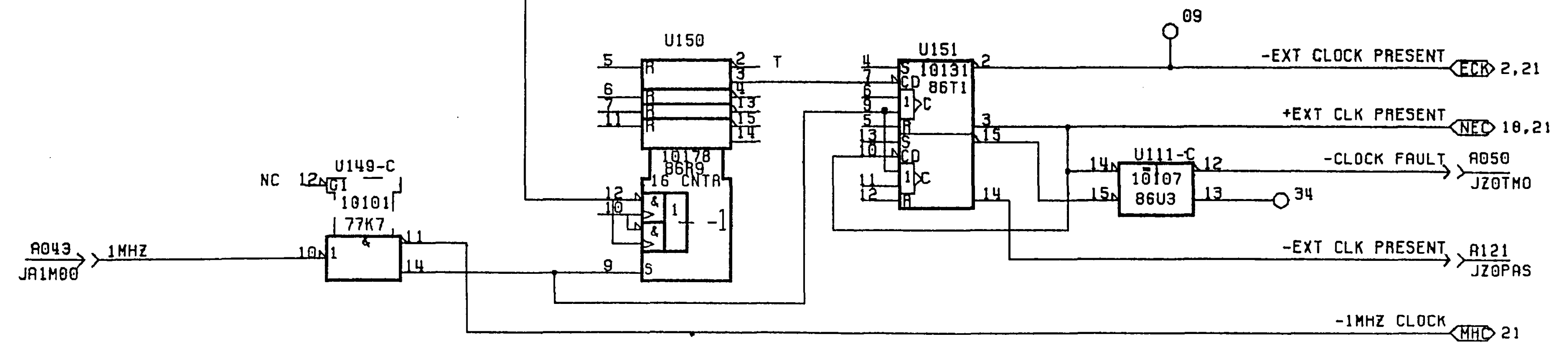
EXTERNAL CLOCK T1/T2 FORMATION (3.6)



EXTERNAL CLOCK TUNING NETWORK (3.6)



EXTERNAL CLOCK DETECTION NETWORK (3.6)



△1 ALL LINES FROM DL100 SHOULD BE .750 INCHES MAXIMUM AND NOT TERMINATED

△2 NOT TERMINATED

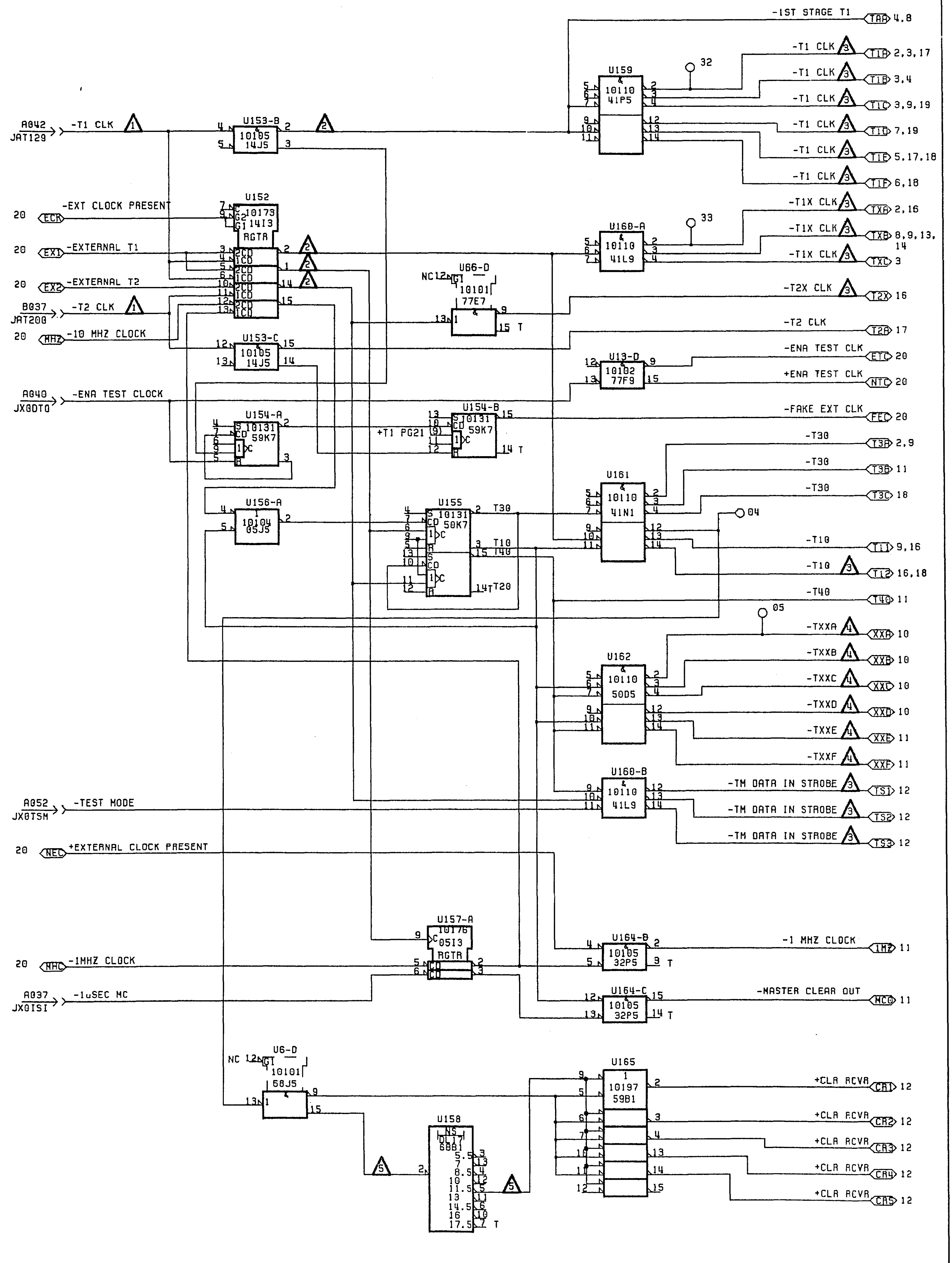
△3 21 TO 23 INCHES

△4 SAME LENGTH

△5 ROUTE FOIL TO 10117 AND THEN 10101

CONTROL DATA	170 DMA CHAN EXT I/F EXTERNAL CLOCK T1/T2 FORMATION, TUNING AND DETECTION NETWORKS TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
		SHEET NO. 20	60462210	PAGE KZ-20	

CLOCK FORMATION AND FANOUT (3.6)



4" MAXMIMUM

7" MAXIMUM

12" MAXIMUM

ALL TXX CLOCKS MUST BE THE SAME LENGTH

NOT TERMINATED

CONTROL DATA

170 DMA CHAN EXT I/F
CLOCK FORMATION AND FANOUT

TYPE 1KZH

B

DWG NO. 22132520

DATE 03/10/87

REV C

SHEET NO. 21

60462210

PAGE KZ-21

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	12	+INACTIVE IN	27	05	-CONV DATA BIT 63
02	12	+EMPTY IN	28	04	+R RGTR BIT 63
03	12	+FULL IN	29	04	-MUX DATA BIT 63
04	21	-T10 EXT CLOCK	30	15	-PP DATA BIT 63
05	21	-TXX CLOCK	31	02	-SEND DATA
06	09	-FUNCTION OUT	32	21	-T1 CLOCK
07	09	-FULL OUT	33	21	-T1 EXT CLOCK
08	09	-INACTIVE OUT	34	20	+CLOCK FAULT
09	20	-EXT CLOCK PRESENT	35	08	-OUTPUT DATA ERROR
10	19	-END TRANSFER	36	02	-BUSY
11	20	+EXTERNAL CLOCK	37	02	-DMA OUTPUT
12	20	-EXT CLOCK TUNED	38	18	+DATA ACCEPTED
13	02	+XMIT ENA A	39	15	-INPUT DATA ERROR
14	07	-OUT RESYNC BIT 63	40	03	-STAGE FULL
15	08	-XMIT RGTR BIT 63	41	02	-FULL IIA
16	12	+INPUT DATA BIT 63	42	18	-EMPTY RESYNC
17	09	+OUTPUT DATA BIT 63	43	18	-EMPTY IN AT T30
18	09	-ACTIVE OUT	44	03	+OUTPUT BUFFER FULL
19	17	-INPUT DATA AVAIL	45	04	-PARCEL CNT BIT 2
20	19	-FORCE DATA AVAIL	46	02	-DMA INPUT
21	09	-EMPTY OUT	47	04	-PARCEL CNT BIT 0
22	19	-FORCE INPUT "1"	48	04	-PARCEL CNT BIT 1
23	02	+MASTER CLEAR	49	19	+KZ BOARD ERROR
24	19	+OUTSTANDING INACT	50	16	+INPUT BUFFER FULL
25	18	-INACTIVE IN RESYNC	51	06	-CONV DATA ERROR
26	02	-FAST TRANSFER			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065, B065,A066,B066,A077,B077,A097,B097,A107,B107, A117,B117,A037,A038,B037,B038,B128
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070
TERM	NONE
UNUSED	SEE WIRE TABS

CONTROL DATA	170 DMA CHAN EXT I/F TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1KZH	B	DWG NO. 22132520	DATE 10/15/86	REV A
	N	SHEET NO. 22	60462210	PAGE KZ-22	

1LXH IPI CHANNEL BOARD BAS I/F

REVISION HISTORY B/M 41655500

DATE	REV	DESCRIPTION OF CHANGE	INIT
11/19/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	DAS
01/30/87	B	ECO#48482 ADDED PUBS INFO TO ALL PAGES	LHJ
08/05/87	C	ECO #48855 PAGES 8, 9, 11 & 12	SLP
04/15/88	D	ECO #49637 PAGES 9 & 10.	DS

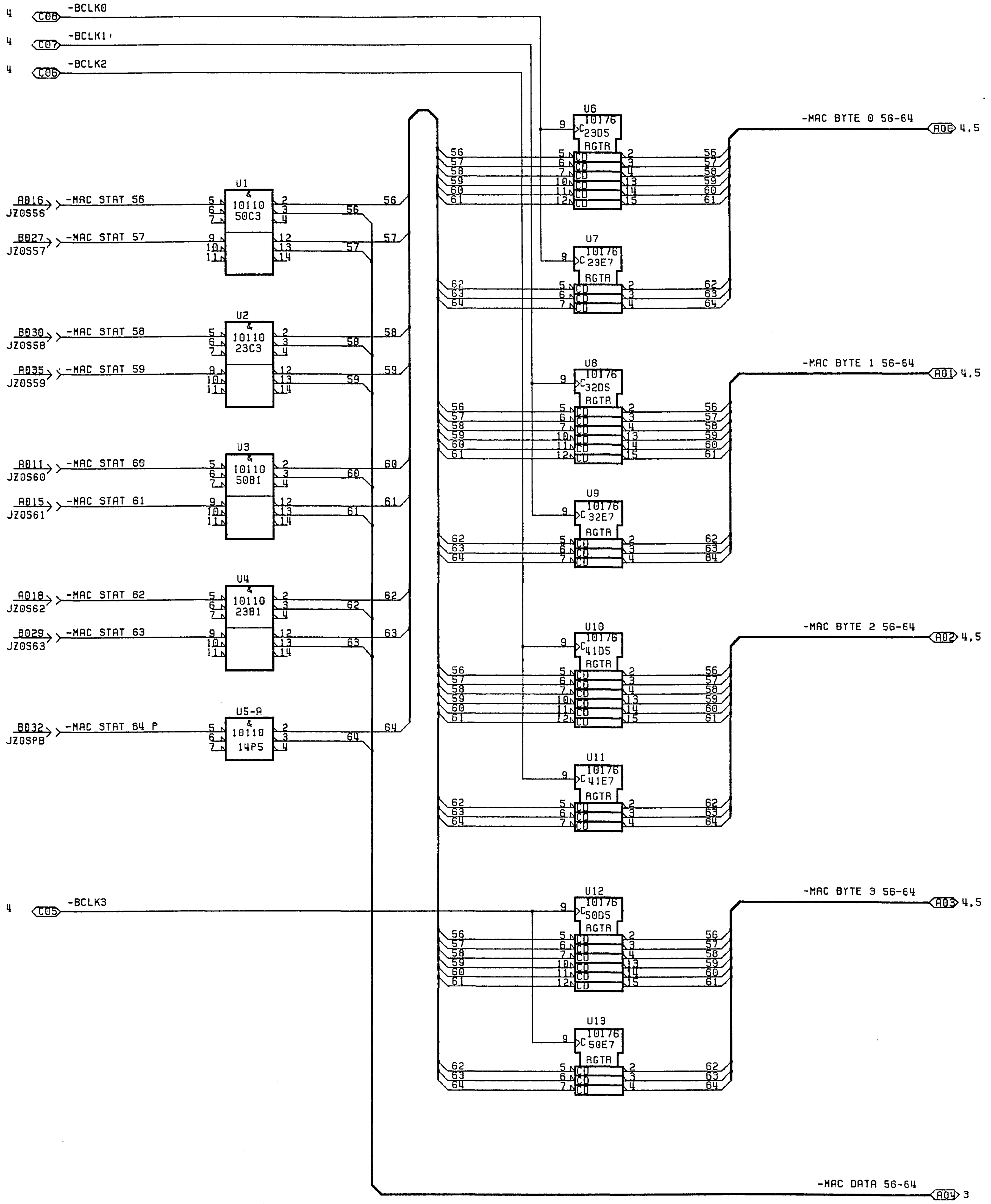
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D11,D14,D17,D20,D23
C11,C14,C17,C20,C23

DWN	L H JOHNSON	11/19/86
CHKD	E PULSHER	1/14/87
ENG	D SCHULTZ	1/14/87
PUBS	N ANDERSON	1/15/87
APP	D SCHULTZ	1/14/87

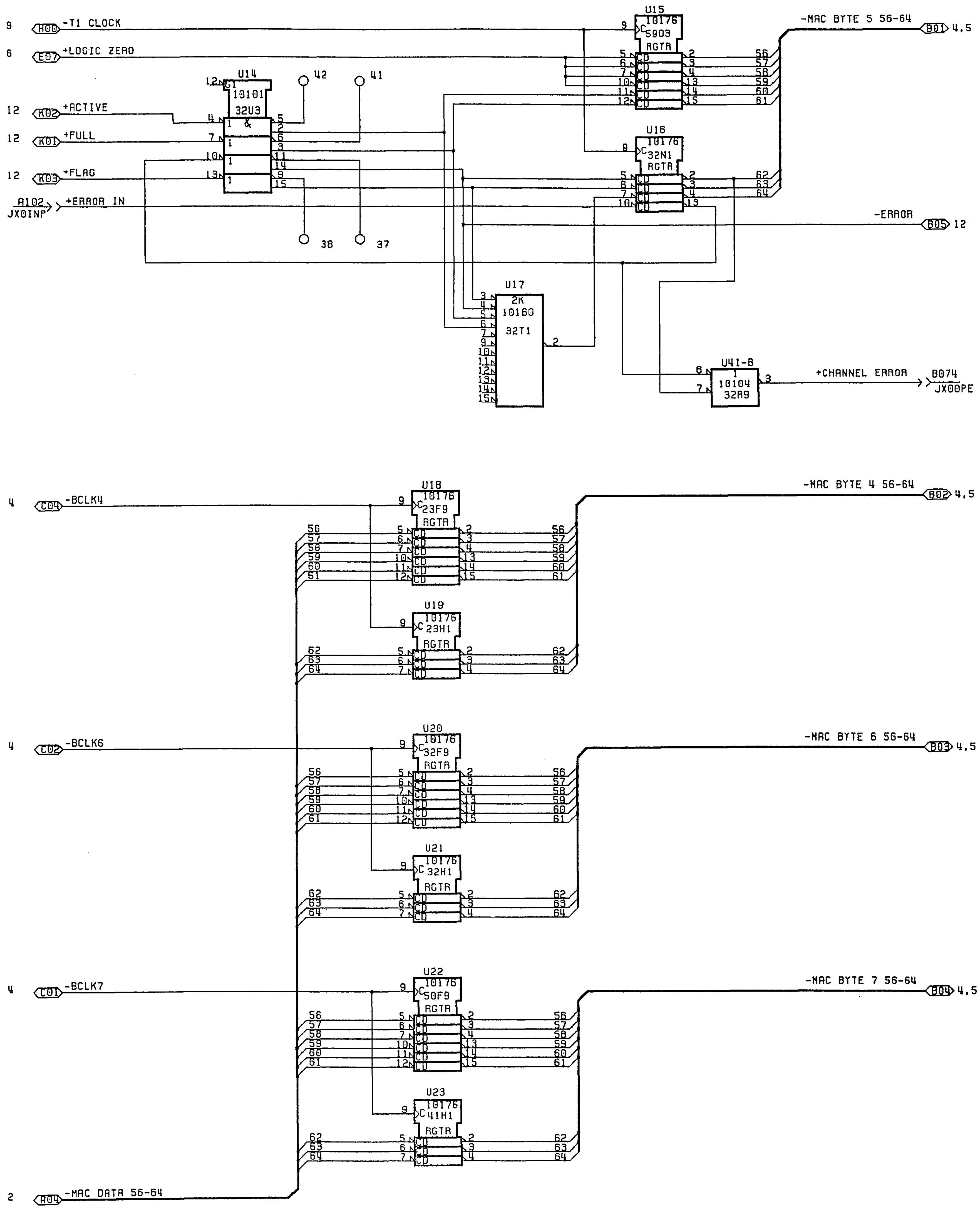
CONTROL DATA	REVISION HISTORY TYPE 1LXH	B	DWG NO. 22132508	DATE 06/16/88	REV D
		N	SHEET NO. 1	60462210	PAGE LX-01

MAC STATUS REG 0-3 (3.1)

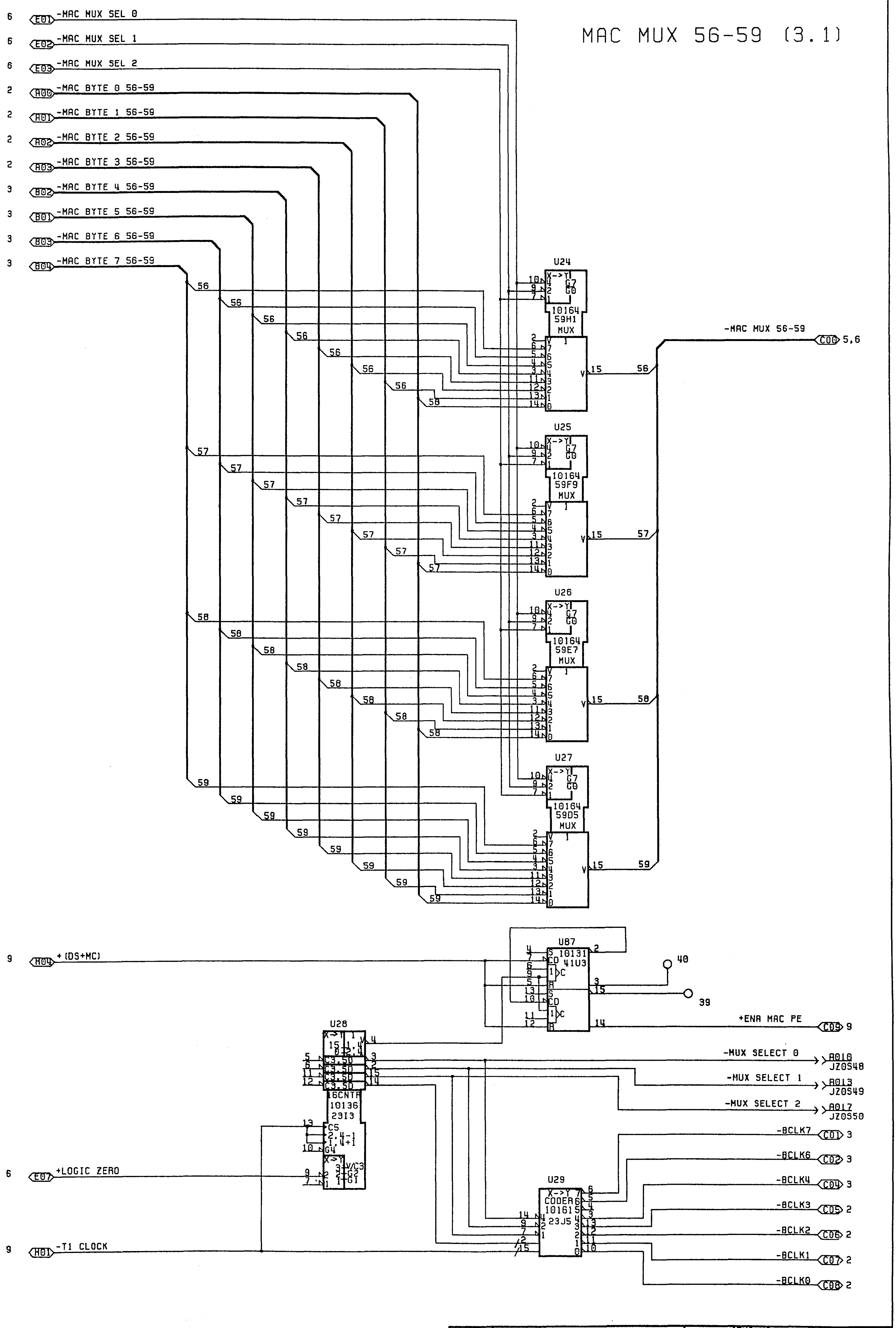


CONTROL DATA	IPI CHANNEL BOARD BAS I/F MAC STATUS REGISTERS FOR BYTES 0-3 TYPE 1LXH	B	DWG NO. 22132508	DATE 01/30/87	REV B
	N	SHEET NO. 2	60462210	PAGE LX-02	

MAC STATUS REG 4-7 (3.1)

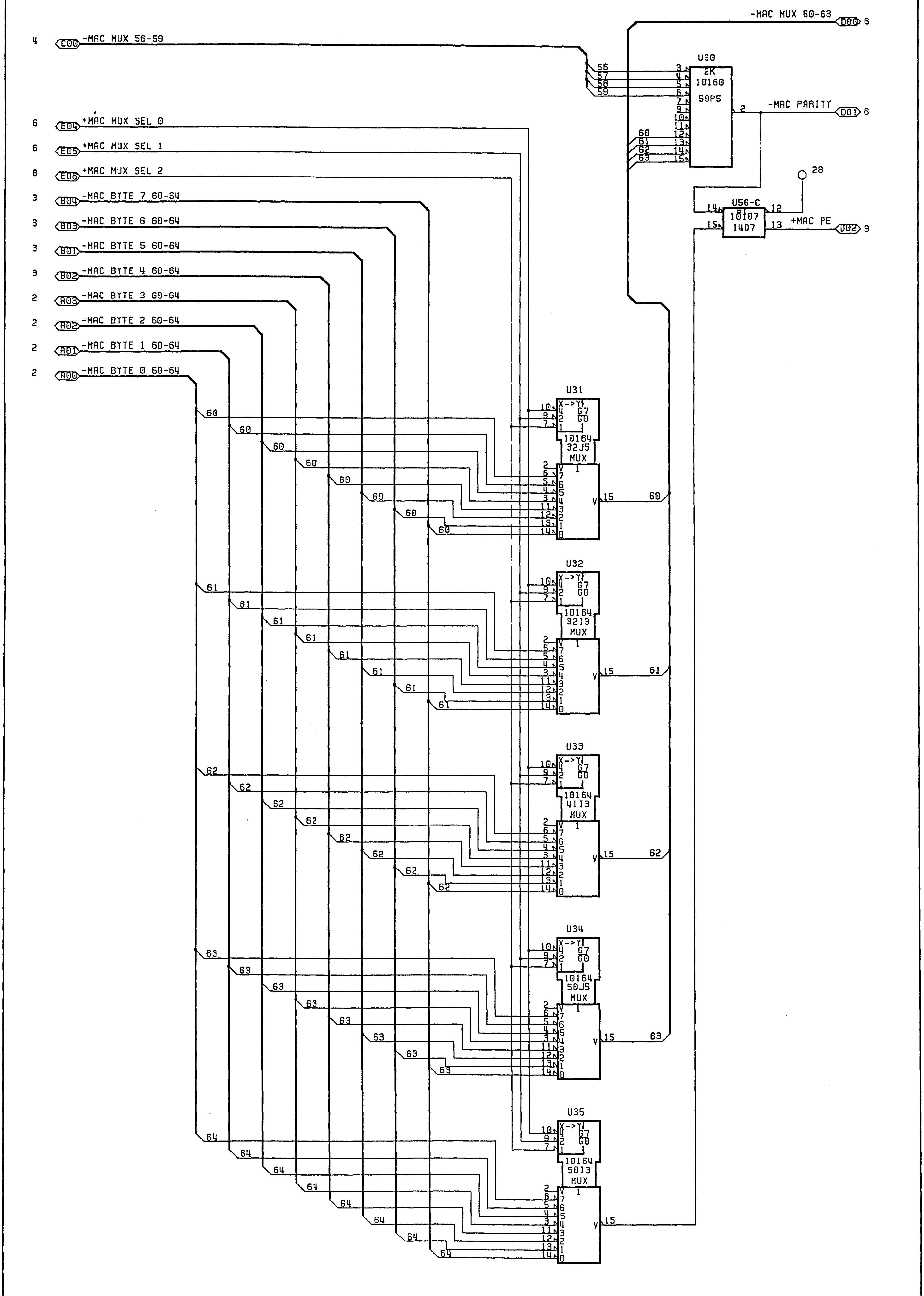


CONTROL DATA	IPI CHANNEL BOARD BAS I/F MAC STATUS REGISTERS FOR BYTES 4-7 TYPE 1LXH	B	DWG NO. 22132508	DATE 01/30/87	REV B
		N	SHEET NO. 3	60462210	PAGE LX-03



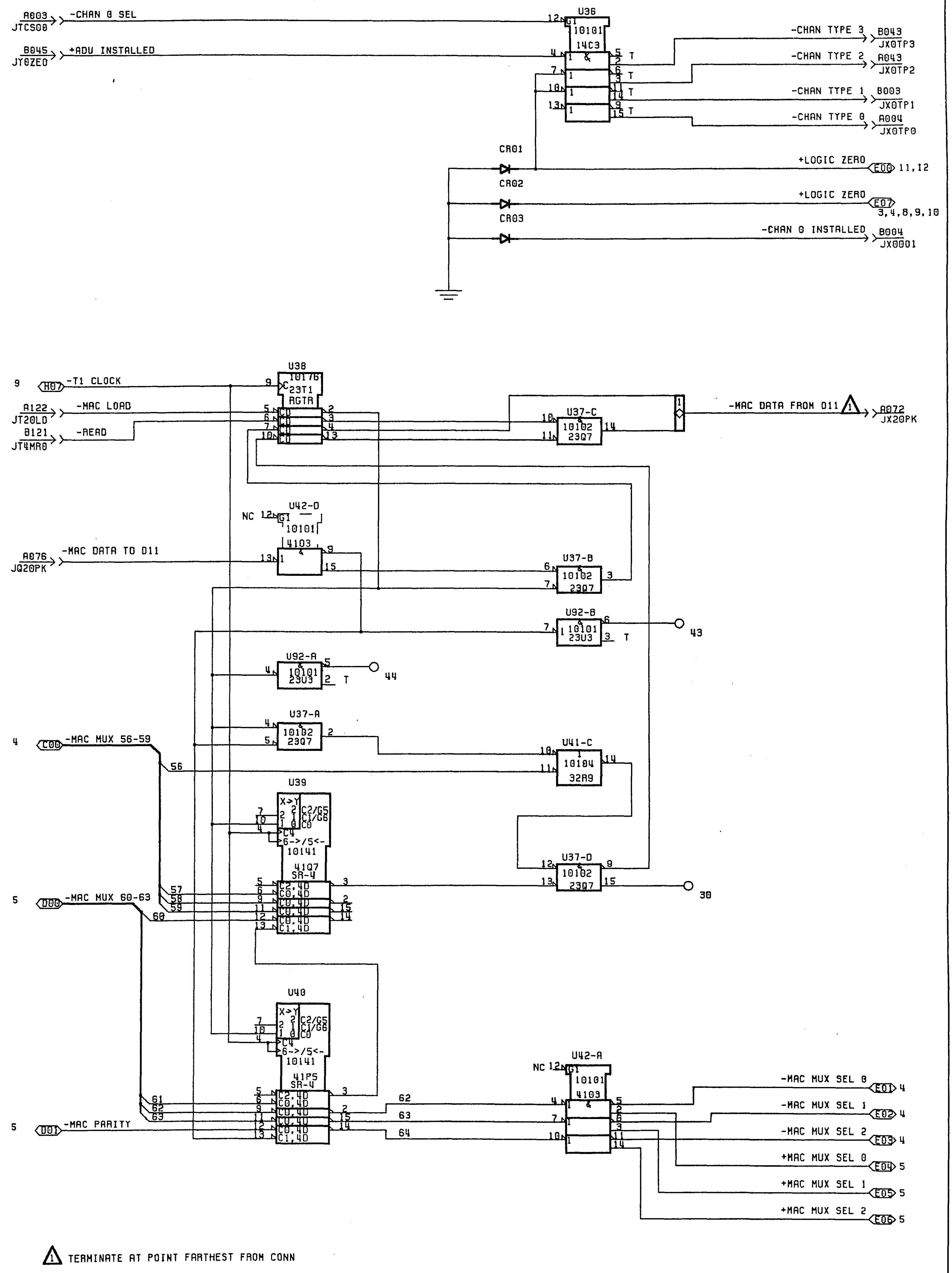
CONTROL DATA	IPI CHANNEL BOARD BAS I/F MAC MUX 56-59 TYPE 1LXH	B	DWG NO. 22132508	DATE 01/30/87	REV B
		N SHEET NO. 4	60462210	PAGE LX-04	

MAC MUX 60-63 (3.1)



CONTROL DATA	IPI CHANNEL BOARD BAS I/F MAC MUX 60 -63 TYPE 1LXH	B	DWG NO. 22132508	DATE 01/30/87	REV B
		N	SHEET NO. 5	60462210	PAGE LX-05

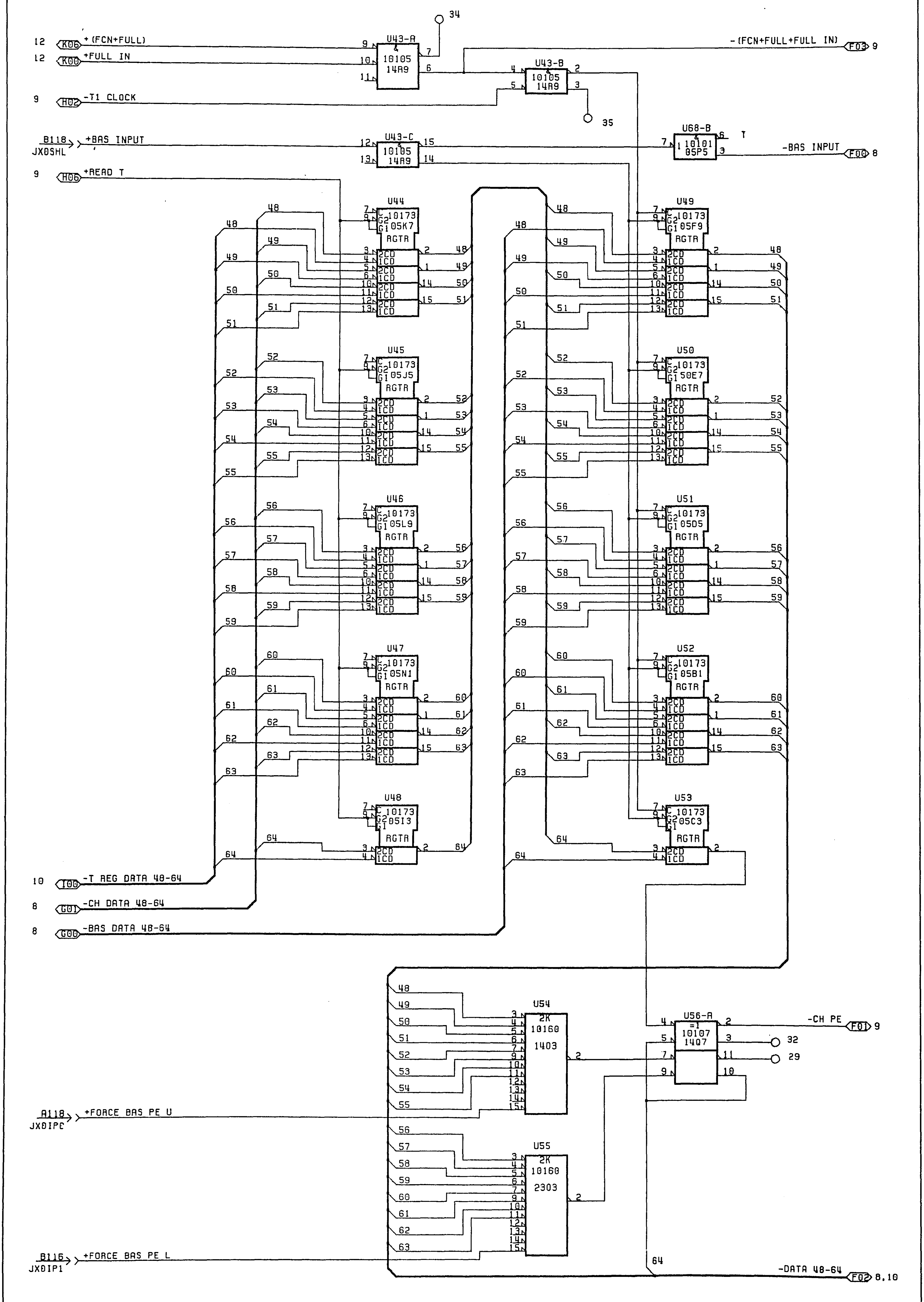
MAC INTERFACE (3.1)



1 TERMINATE AT POINT FARTHEST FROM CONN

CONTROL DATA	IPI CHANNEL BOARD BAS I/F MAC INTERFACE TYPE 1LXH	B	DWG NO. 22132508	DATE 01/30/87	REV B
		N	SHEET NO. 6	60462210	PAGE LX-06

BAS REGISTER (3.0)



CONTROL DATA

IPI CHANNEL BOARD I/F
BAS REGISTER

TYPE 1LXH

B

DWG NO. 22132508

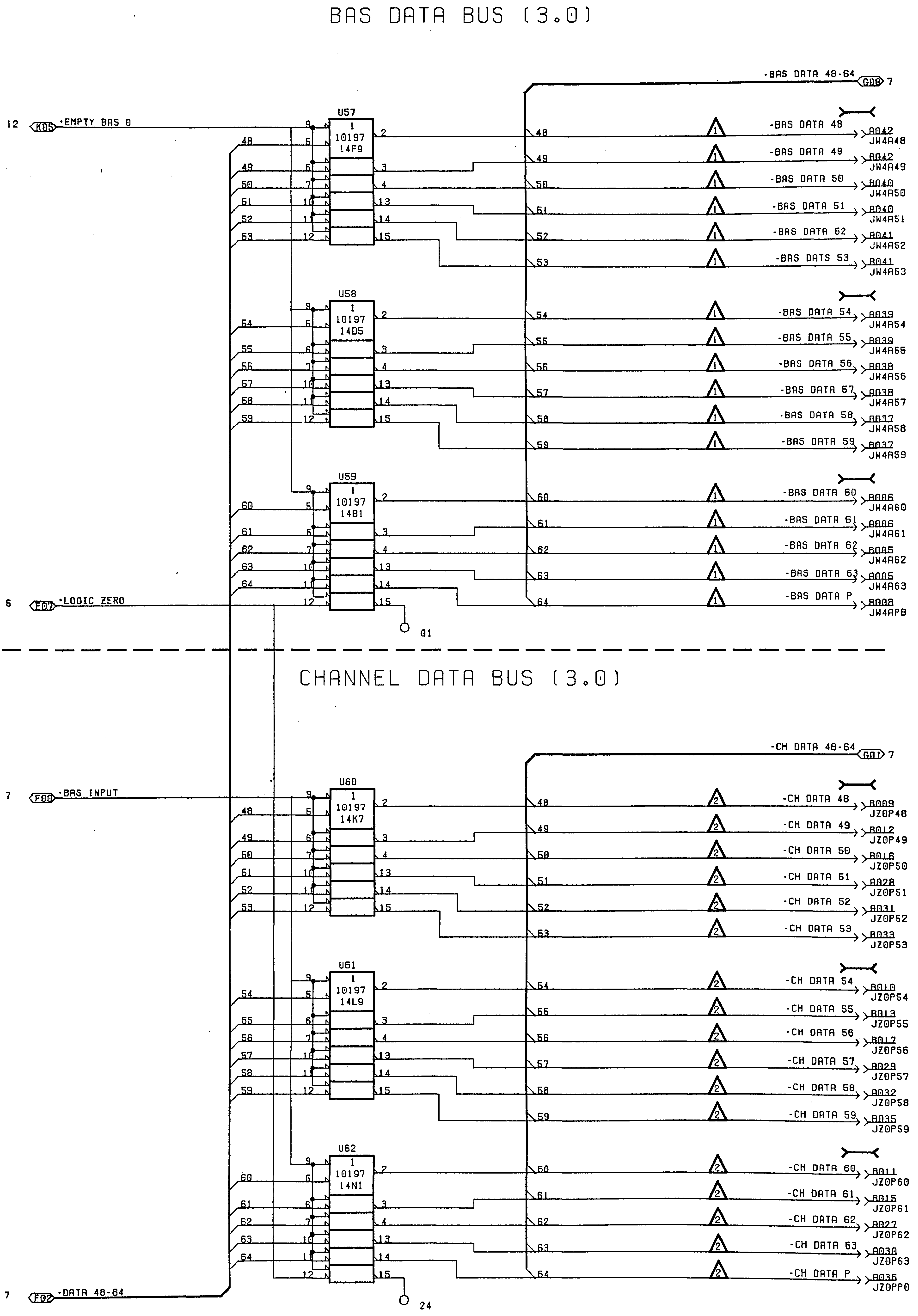
DATE 01/30/87

REV B

SHEET NO. 7

60462210

PAGE LX-07

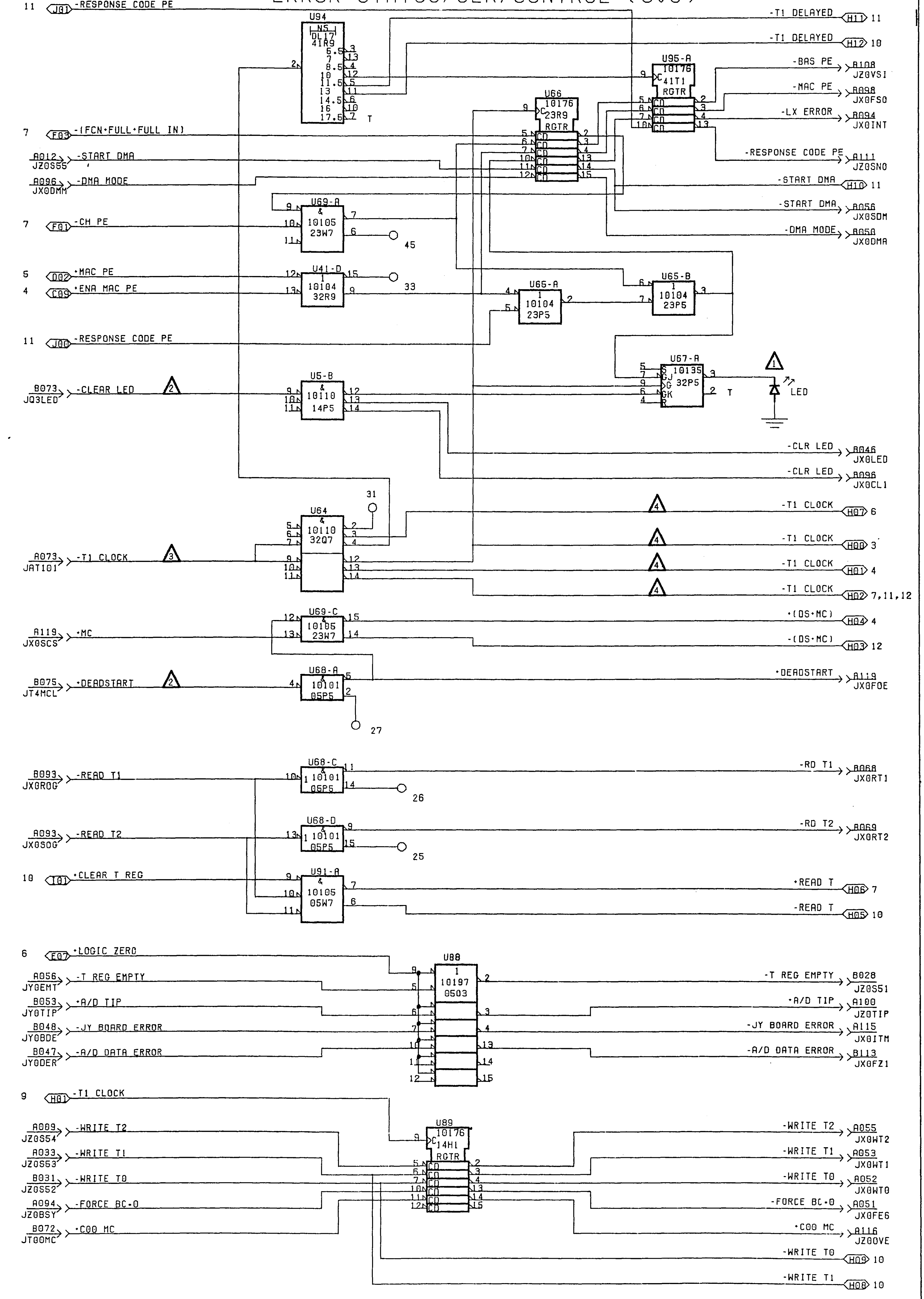


△1 4" MAX LENGTH AND NOT TERMINATED

△2 TERMINATE AT FARTHEST POINT FROM THE CONN PIN

CONTROL DATA	IPI CHANNEL BOARD BAS I/F BAS AND CHANNEL DATA BUS TYPE 1LXH	B	DWG NO. 22132508	DATE 08/05/87	REV C
		SHEET NO. 8	60462210	PAGE LX-08	

ERROR STATUS/CLK/CONTROL (3.0)



1 TERMINATE

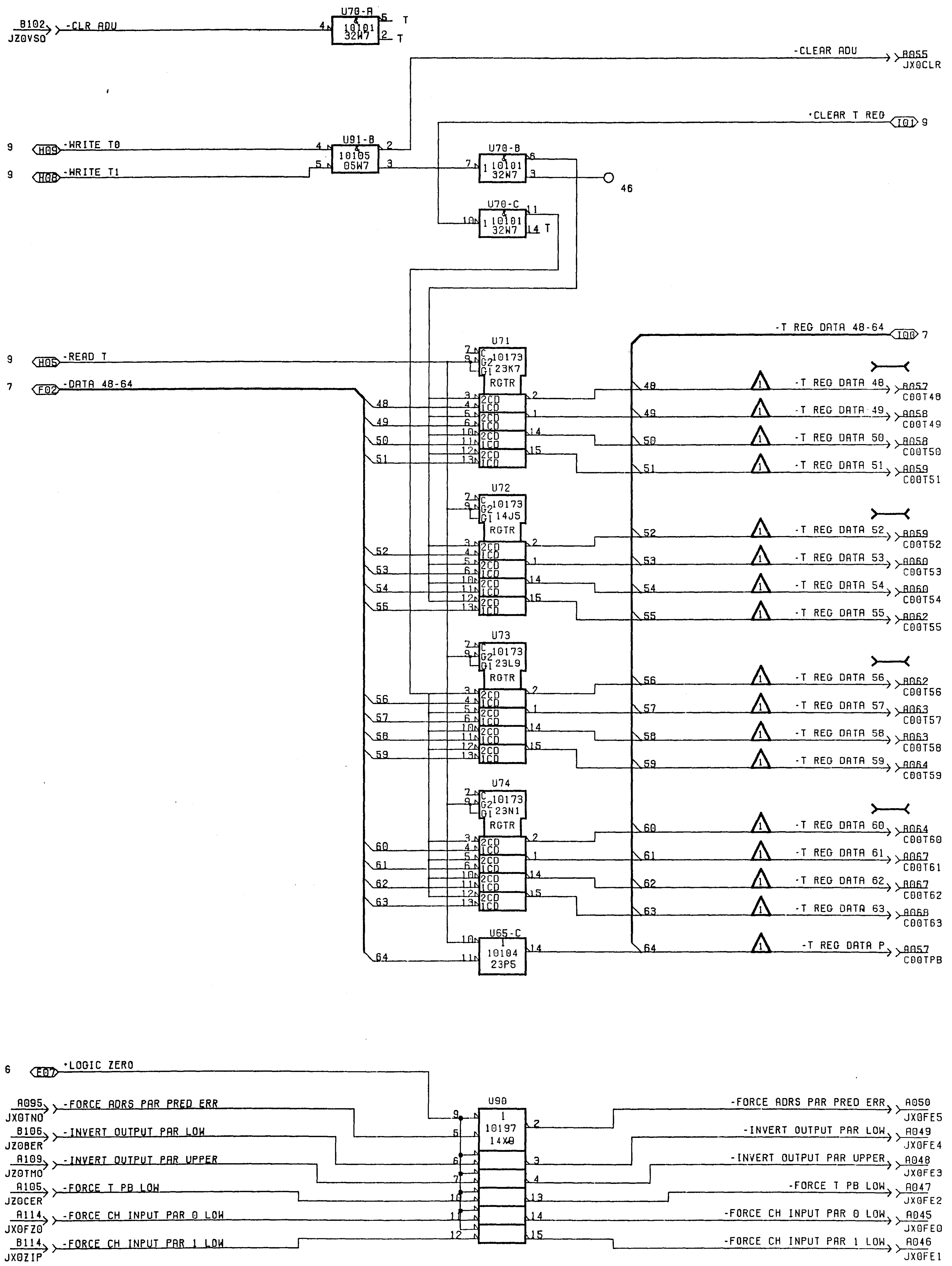
2 3" MAX AND DO NOT TERMINATE

3 7" MAX

4 12" MAX

CONTROL DATA	IPI CHANNEL BOARD BAS I/F ERROR STATUS CLOCK,DEADSTART,MC,READ T TYPE ILXH	B	DWG NO. 22132508	DATE 06/16/88	REV D
		SHEET NO. 9	60462210	PAGE LX-09	

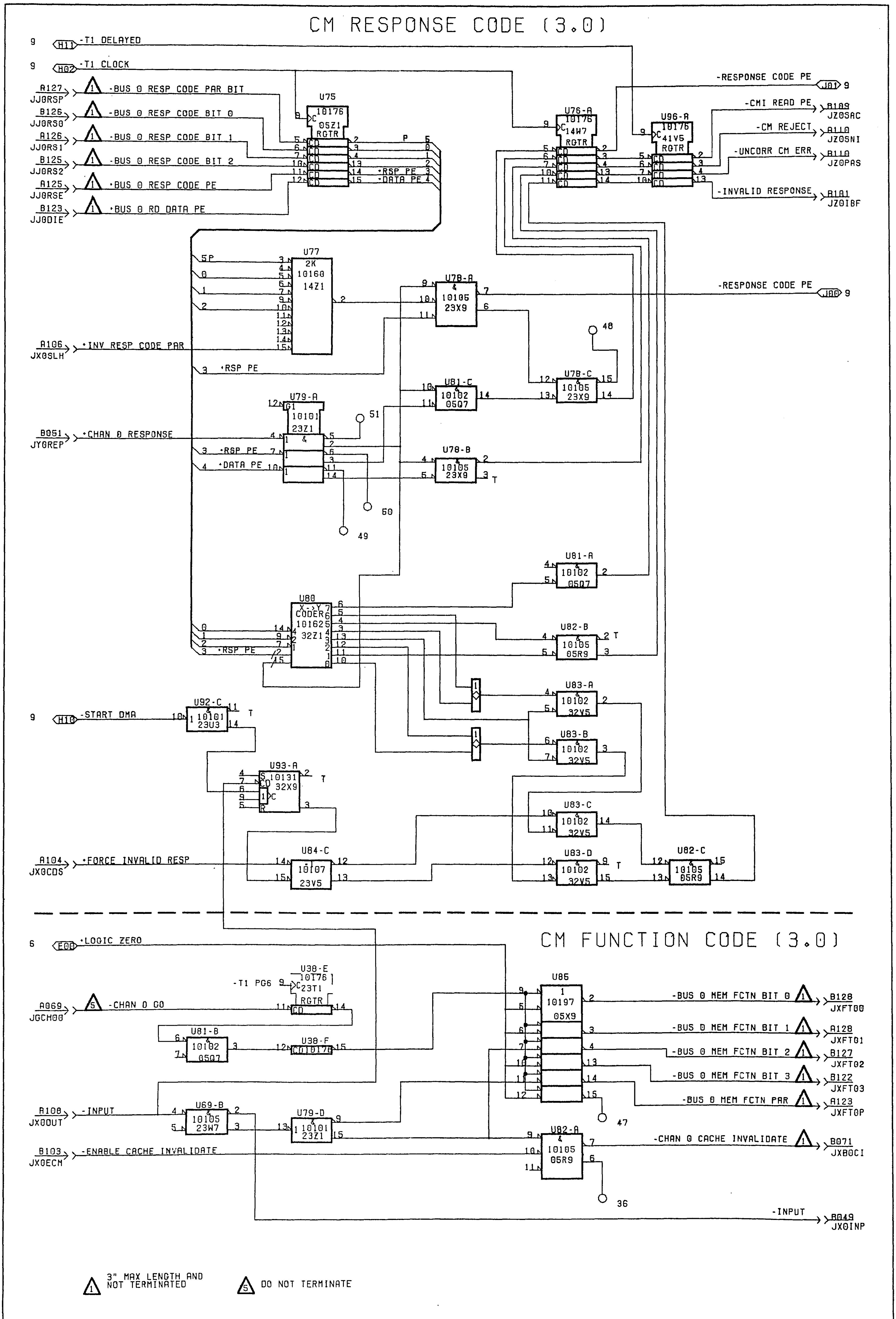
T REG DATA BUS (3.0)


B102 JZ0VS0 -CLR ADV
U70-A 10101 32W7
-CLEAR ADV A055 JX0CLR
-CLEAR T REG I01 9
9 H09 -WRITE T0
9 H08 -WRITE T1
U91-B 10105 05W7
U70-B 10101 32W7
46
U70-C 10101 32W7
-T REG DATA 48-64 I00 7
9 H05 -READ T
7 F02 -DATA 48-64
U71 10173 23K7 RGTR
U72 10173 14J5 RGTR
U73 10173 23L9 RGTR
U74 10173 23N1 RGTR
U65-C 10104 23P5
-T REG DATA 48 A057 C00T48
-T REG DATA 49 A058 C00T49
-T REG DATA 50 A058 C00T50
-T REG DATA 51 A059 C00T51
-T REG DATA 52 A059 C00T52
-T REG DATA 53 A060 C00T53
-T REG DATA 54 A060 C00T54
-T REG DATA 55 A062 C00T55
-T REG DATA 56 A062 C00T56
-T REG DATA 57 A063 C00T57
-T REG DATA 58 A063 C00T58
-T REG DATA 59 A064 C00T59
-T REG DATA 60 A064 C00T60
-T REG DATA 61 A067 C00T61
-T REG DATA 62 A067 C00T62
-T REG DATA 63 A068 C00T63
-T REG DATA P A057 C00TPB
6 E07 ·LOGIC ZERO
U90 10197 14X8
A095 JX0TN0 -FORCE ADRS PAR PRED ERR
B106 JZ0BER -INVERT OUTPUT PAR LOW
A109 JZ0TM0 -INVERT OUTPUT PAR UPPER
A105 JZ0CER -FORCE T PB LOW
A114 JX0FZ0 -FORCE CH INPUT PAR 0 LOW
B114 JX0ZIP -FORCE CH INPUT PAR 1 LOW
-FORCE ADRS PAR PRED ERR A050 JX0FE5
-INVERT OUTPUT PAR LOW A049 JX0FE4
-INVERT OUTPUT PAR UPPER A048 JX0FE3
-FORCE T PB LOW A047 JX0FE2
-FORCE CH INPUT PAR 0 LOW A045 JX0FE0
-FORCE CH INPUT PAR 1 LOW A046 JX0FE1

△1 TERMINATE AT POINT FARTHEST FROM CONN

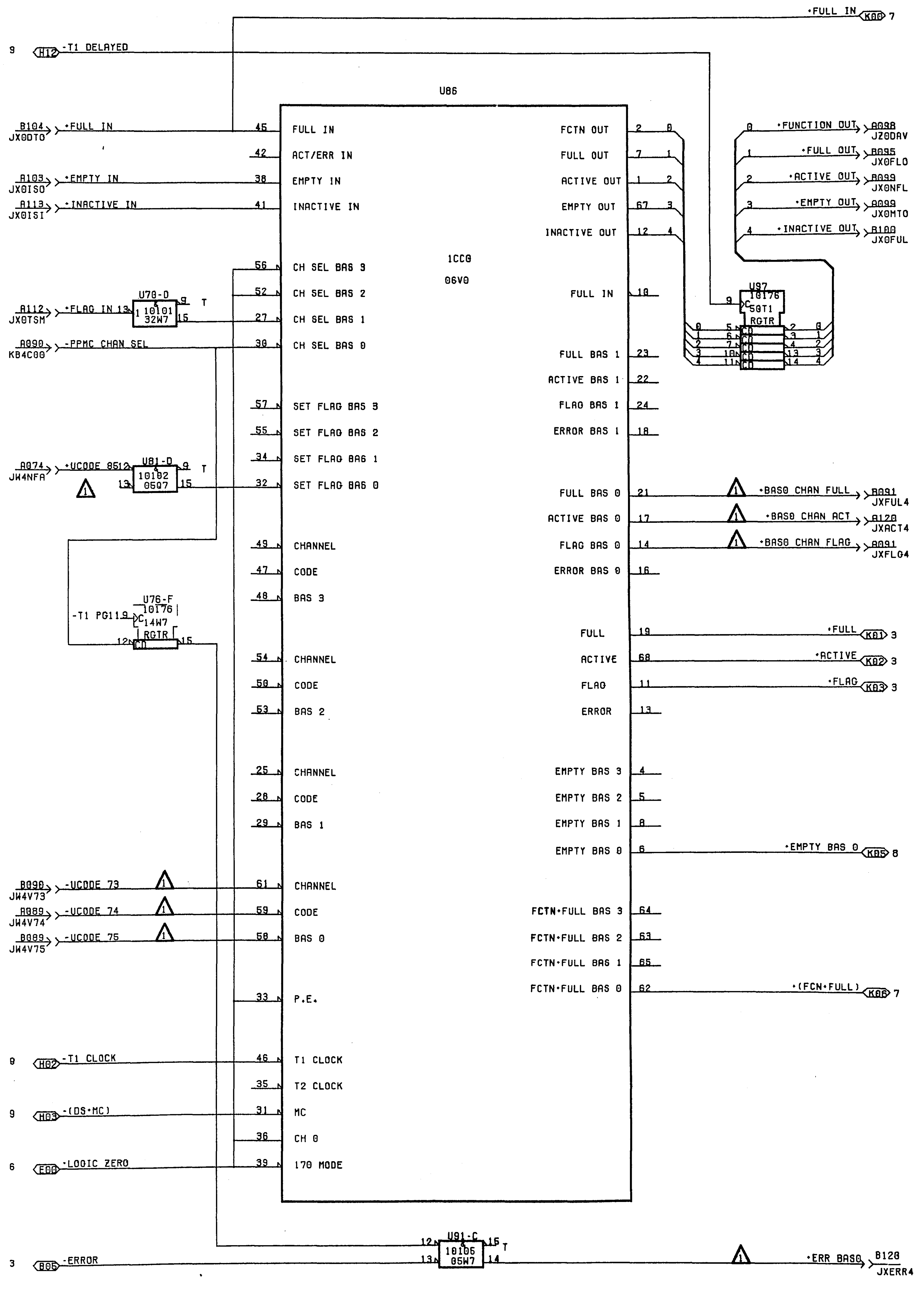
CONTROL DATA	IPI CHANNEL BOARD BAS I/F T REGISTER DATA TYPE 1LXH	B	DWG NO. 22132508	DATE 06/16/88	REV D
		N	SHEET NO. 10	60462210	PAGE LX-10

CM RESPONSE CODE (3.0)



CONTROL DATA	IPI CHANNEL BOARD BAS I/F CM RESPONSE CODE TRANSLATOR CM FUNCTION CODE TYPE 1LXH	B	DWG NO. 22132508	DATE 08/05/87	REV C
		N	SHEET NO. 11	60462210	PAGE LX-11

CHANNEL FLAGS AND MICROCODE TRANSLATOR (3.1)



△1 3" MAX LENGTH AND NOT TERMINATED

CONTROL DATA

IPI CHANNEL BOARD BAS I/F
MACROCELL
TYPE 1LXH

B

DWG NO. 22132608

DATE 08/05/87

REV C

SHEET NO. 12 60462210 PAGE LX-12

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	08	+EMPTY BAS 0	27	09	-DEADSTART
02			28	05	-MAC PARITY ERROR
03			29	07	+BAS RGTR PARITY
04			30	06	+MAC READ DATA
05			31	09	-T1 CLOCK
06			32	07	+CHAN PARITY ERROR
07			33	09	+MAC PARITY ERROR
08			34	07	+FULL IN
09			35	07	+CLOCK BAS RGTR
10			36	11	+INVALIDATE
11			37	03	+ERROR IN
12			38	03	+FLAG
13			39	04	+ENABLE MAC PE
14			40	04	+DS + MC DELAYED
15			41	03	+FULL
16			42	03	+ACTIVE
17			43	06	-MAC DATA TO D11
18			44	06	-MAC LOAD
19			45	09	+CHAN INPUT PE
20			46	10	-CLEAR T RGTR
21			47	11	+CHAN GO
22			48	11	+RESPONSE CODE PE
23			49	11	+DATA PE
24	08	+BAS INPUT	50	11	+RESPONSE PE
25	09	+READ T RGTR 2	51	11	+CHAN 0 RESPONSE
26	09	+READ T RGTR 1			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 (NU)
TERM	NONE
UNUSED	A008,B018,A019,B019,A020,B020,A021,B021,A022,B022,A023,B023,A025,B025,A026,B026,B036,B052,A061,B061,A070,B070,A071,A075,B076,A078,B078,A079,B079,A080,B080,A081,B081,A082,B082,A083,B083,A084,B084,A085,B085,A086,B086,A088,B088,A092,B092,A101,B105,B111,B112,B115,A121

CONTROL DATA	IPI CHANNEL BOARD BAS I/F TESTPOINTS AND SIGNAL NAMES AND CONNECTOR PINS TYPE 1LXH	B	DWG NO. 22132508	DATE 01/30/87	REV B
		N	SHEET NO. 13	60462210	PAGE LX-13

1LZH IPI CHANNEL BOARD

REVISION HISTORY B/M 41655702

DATE	REV	DESCRIPTION OF CHANGE	INIT
12/04/86	A	CLASS A RELEASE OF LOGIC DIAGRAMS	DAZ
11/17/87	B	ECO #48855 PAGE 21	SLP

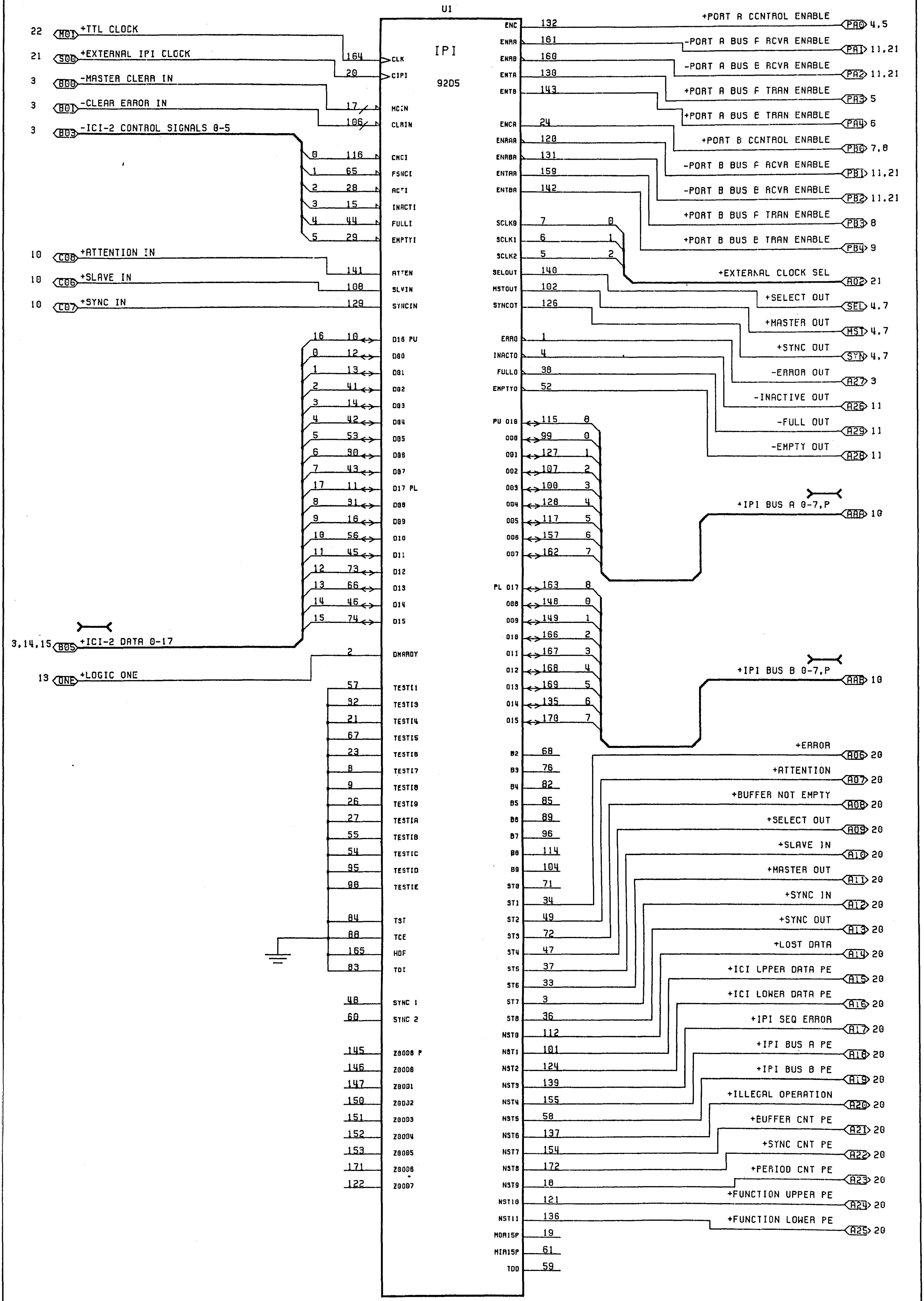
DWN	L H JOHNSON	12/04/86
CHKD	S L PJESCICH	06/03/87
ENG	D A SCHULTZ	06/03/87
PUBS	N J ANDERSON	06/03/87
APP	D A SCHULTZ	06/03/87

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: D09,D12,D15,D18,D21
C09,C12,C15,C18,C21

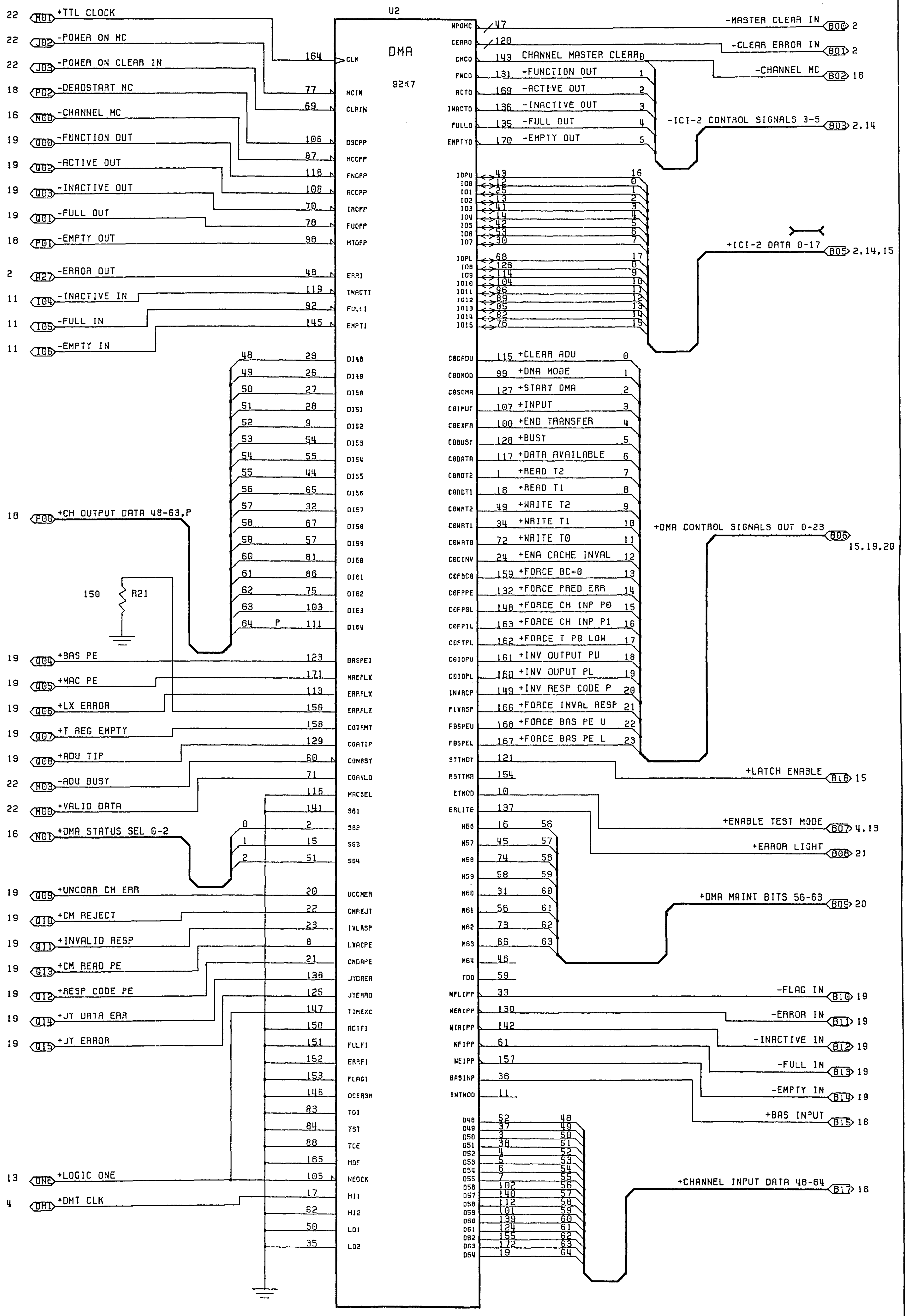
CONTROL DATA	REVISION HISTORY TYPE 1LZH	B	DWG NO. 22132509	DATE 11/17/87	REV B
		SHEET NO. 1	60462210	PAGE 1Z-01	

IPI ARRAY (3.1)


U1
IPI
92D5
22 H01 +TTL CLOCK 164 CLK
21 S00 +EXTERNAL IPI CLOCK 20 CIPI
3 B00 -MASTER CLEAR IN 17 MCIN
3 B01 -CLEAR ERROR IN 106 CLRIN
3 B03 -ICI-2 CONTROL SIGNALS 0-5
0 116 CNCI
1 65 FSNCI
2 28 ACTI
3 15 INACTI
4 44 FULLI
5 29 EMPTYI
10 C08 +ATTENTION IN 141 ATTEN
10 C06 +SLAVE IN 108 SLVIN
10 C07 +SYNC IN 129 SYNCIN
16 10 D16 PU
0 12 D00
1 13 D01
2 41 D02
3 14 D03
4 42 D04
5 53 D05
6 90 D06
7 43 D07
17 11 D17 PL
8 31 D08
9 16 D09
10 56 D10
11 45 D11
12 73 D12
13 66 D13
14 46 D14
15 74 D15
3,14,15 B05 +ICI-2 DATA 0-17
2 DHRDY
13 ONE +LOGIC ONE
57 TESTI1
32 TESTI3
21 TESTI4
67 TESTI5
23 TESTI6
8 TESTI7
9 TESTI8
26 TESTI9
27 TESTIA
55 TESTIB
54 TESTIC
95 TESTID
98 TESTIE
84 TST
88 TCE
165 HDF
83 TDI
48 SYNC 1
60 SYNC 2
145 Z0000 P
146 Z0000
147 Z0001
150 Z0002
151 Z0003
152 Z0004
153 Z0005
171 Z0006
122 Z0007
ENC 132 +PORT A CONTROL ENABLE PA0 4,5
ENAA 161 -PORT A BUS F RCVR ENABLE PA1 11,21
ENAB 160 -PORT A BUS E RCVR ENABLE PA2 11,21
ENTA 130 +PORT A BUS F TRAN ENABLE PA3 5
ENTB 143 +PORT A BUS E TRAN ENABLE PA4 6
ENCA 24 +PORT B CONTROL ENABLE PB0 7,8
ENAAA 120 -PORT B BUS F RCVR ENABLE PB1 11,21
ENABA 131 -PORT B BUS E RCVR ENABLE PB2 11,21
ENTAA 159 +PORT B BUS F TRAN ENABLE PB3 8
ENTBA 142 +PORT B BUS E TRAN ENABLE PB4 9
SCLK0 7 0
SCLK1 6 1
SCLK2 5 2
+EXTERNAL CLOCK SEL A02 21
SELOUT 140 +SELECT OUT SEL 4,7
MSTOUT 102 +MASTER OUT MST 4,7
SYNCOT 126 +SYNC OUT SYN 4,7
ERRO 1 -ERROR OUT A27 3
INACTO 4 -INACTIVE OUT A26 11
FULLO 38 -FULL OUT A29 11
EMPTYO 52 -EMPTY OUT A28 11
PU 016 115 8
000 99 0
001 127 1
002 107 2
003 100 3
004 128 4
005 117 5
006 157 6
007 162 7
+IPI BUS A 0-7,P AAA 10
PL 017 163 8
008 148 0
009 149 1
010 166 2
011 167 3
012 168 4
013 169 5
014 135 6
015 170 7
+IPI BUS B 0-7,P AAB 10
B2 68 +ERROR A06 20
B3 76 +ATTENTION A07 20
B4 82 +BUFFER NOT EMPTY A08 20
B5 85 +SELECT OUT A09 20
B6 89 +SLAVE IN A10 20
B7 96 +MASTER OUT A11 20
B8 114 +SYNC IN A12 20
B9 104 +SYNC OUT A13 20
ST0 71 +LOST DATA A14 20
ST1 34 +ICI UPPER DATA PE A15 20
ST2 49 +ICI LOWER DATA PE A16 20
ST3 72 +IPI SEQ ERROR A17 20
ST4 47 +IPI BUS A PE A18 20
ST5 37 +IPI BUS B PE A19 20
ST6 33 +ILLEGAL OPERATION A20 20
ST7 3 +BUFFER CNT PE A21 20
ST8 36 +SYNC CNT PE A22 20
NST0 112 +PERIOD CNT PE A23 20
NST1 101 +FUNCTION UPPER PE A24 20
NST2 124 +FUNCTION LOWER PE A25 20
NST3 139
NST4 155
NST5 58
NST6 137
NST7 154
NST8 172
NST9 18
NST10 121
NST11 136
MOR15P 19
MIR15P 61
TDO 59

CONTROL DATA	IPI TRANSMITTER BOARD IPI ARRAY TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		SHEET NO. 2	60462210	PAGE LZ-02	

DMA ARRAY (3.0)

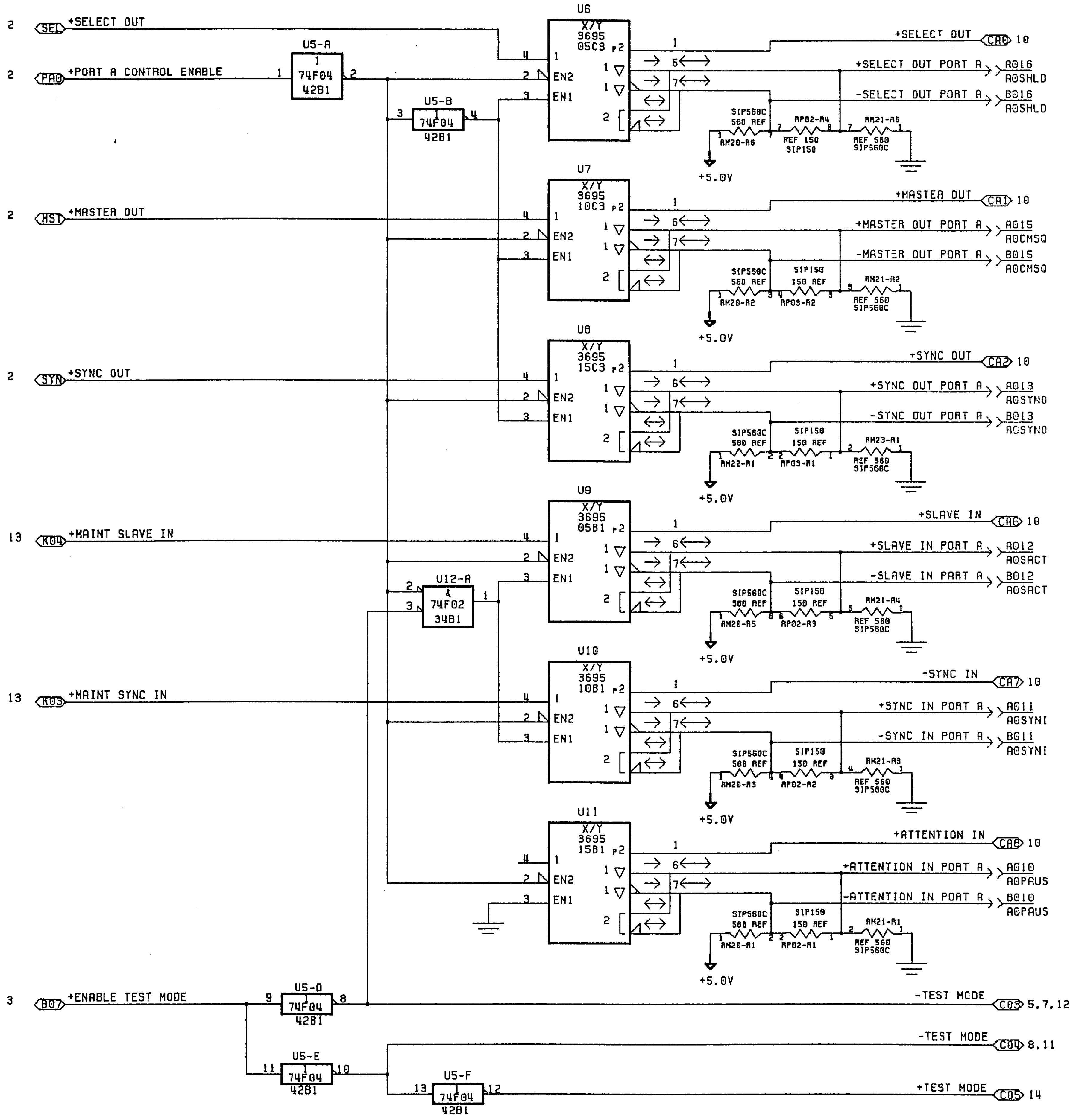


CONTROL DATA

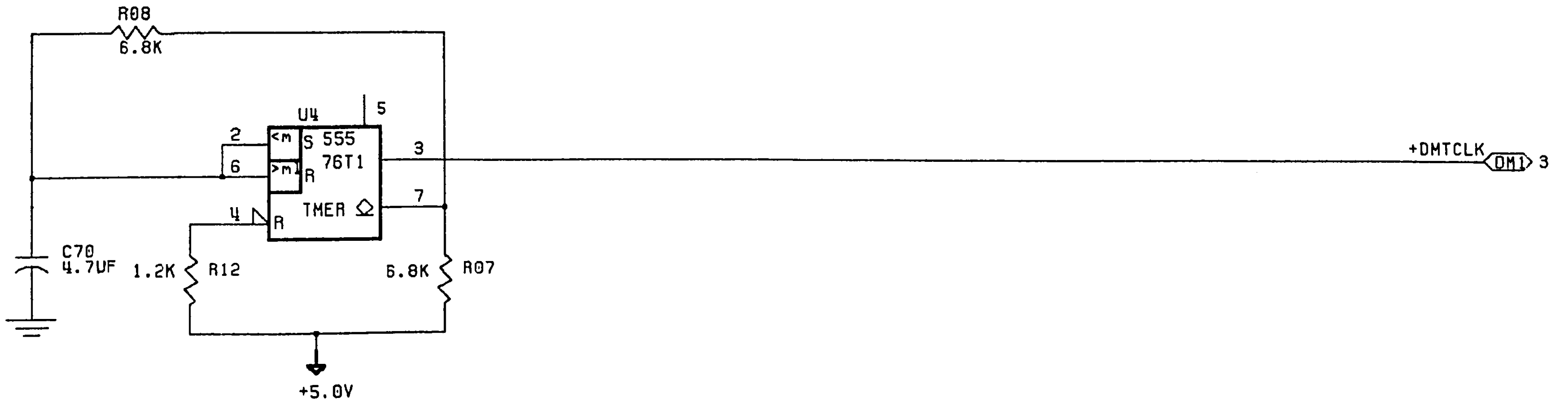
IPI TRANSMITTER BOARD
DMA ARRAY
TYPE 1LZH

B	DWG NO. 22132509		DATE 12/04/86	REV A
	SHEET NO. 3	60462210	PAGE LZ-03	

IPI PORT A CONTROL TX/RX (3.2)

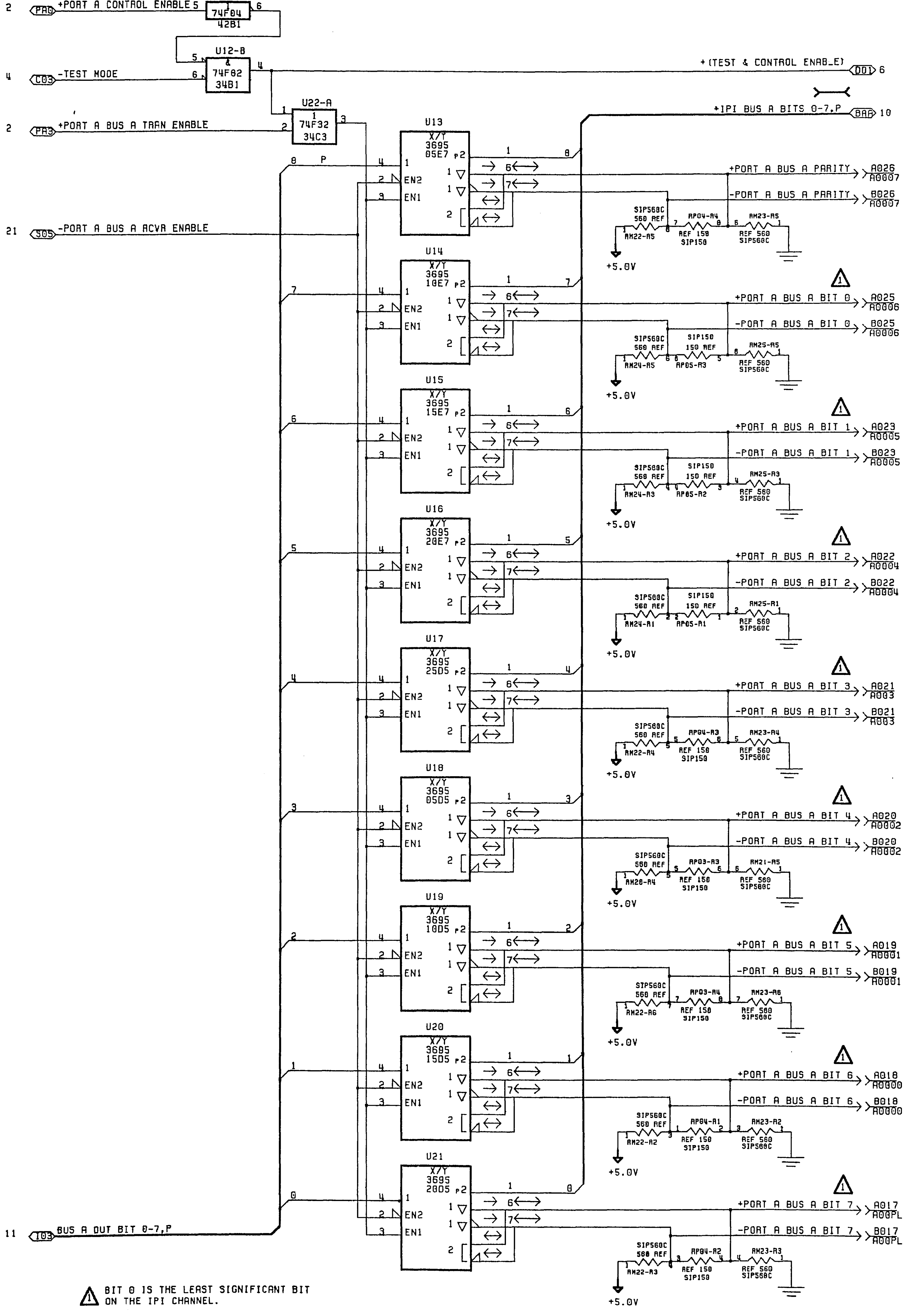


DEADMAN TIMEOUT OSC (3.0)



CONTROL DATA	IPI TRANSMITTER BOARD PORT A CONTROL R&T's TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		N	SHEET NO. 4	60462210	PAGE LZ-04

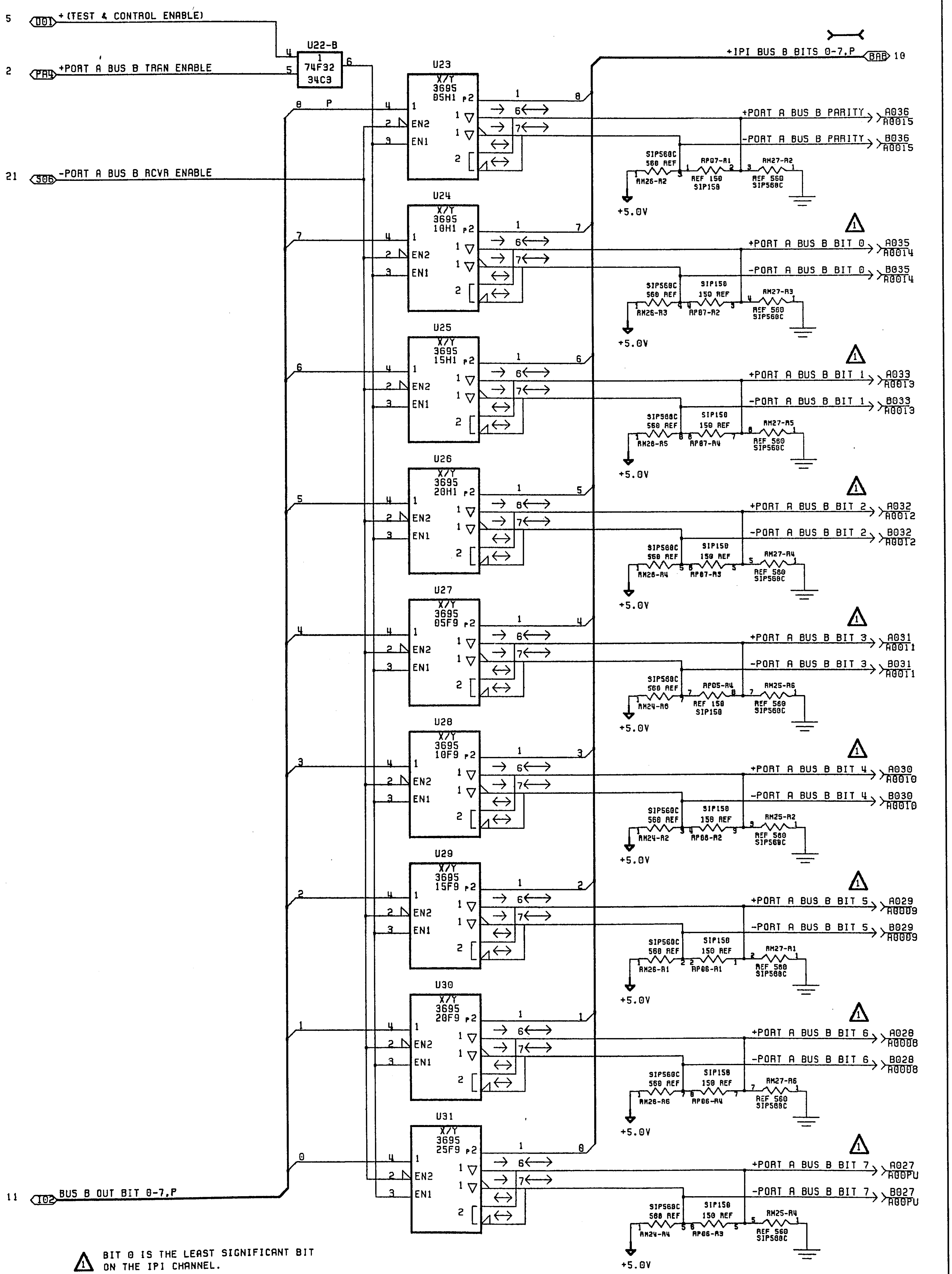
IPI PORT A BUS A TX/RX (3.2)


2 PA0 +PORT A CONTROL ENABLE
U5-C 74F04 42B1
U12-B 74F02 34B1
4 C03 -TEST MODE
+(TEST & CONTROL ENAB_E) D01 6
U22-A 74F32 34C3
2 PA3 +PORT A BUS A TRAN ENABLE
+IPI BUS A BITS 0-7,P BA0 10
21 S05 -PORT A BUS A RCVA ENABLE
U13 X/T 3695 05E7
U14 X/T 3695 10E7
U15 X/T 3695 15E7
U16 X/T 3695 20E7
U17 X/T 3695 25D5
U18 X/T 3695 05D5
U19 X/T 3695 10D5
U20 X/T 3695 15D5
U21 X/T 3695 20D5
EN1
EN2
+PORT A BUS A PARITY A026 A0007
-PORT A BUS A PARITY B026 A0007
+PORT A BUS A BIT 0 A025 A0006
-PORT A BUS A BIT 0 B025 A0006
+PORT A BUS A BIT 1 A023 A0005
-PORT A BUS A BIT 1 B023 A0005
+PORT A BUS A BIT 2 A022 A0004
-PORT A BUS A BIT 2 B022 A0004
+PORT A BUS A BIT 3 A021 A003
-PORT A BUS A BIT 3 B021 A003
+PORT A BUS A BIT 4 A020 A0002
-PORT A BUS A BIT 4 B020 A0002
+PORT A BUS A BIT 5 A019 A0001
-PORT A BUS A BIT 5 B019 A0001
+PORT A BUS A BIT 6 A018 A0000
-PORT A BUS A BIT 6 B018 A0000
+PORT A BUS A BIT 7 A017 A00PL
-PORT A BUS A BIT 7 B017 A00PL
SIP560C 560 REF
REF 150 SIP150
REF 560 SIP560C
+5.0V
11 I03 BUS A OUT BIT 0-7,P

⚠ BIT 0 IS THE LEAST SIGNIFICANT BIT ON THE IPI CHANNEL.

CONTROL DATA	IPI TRANSMITTER BOARD PORT A BUS A R&T's TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
			SHEET NO. 5	60462210	PAGE LZ-85

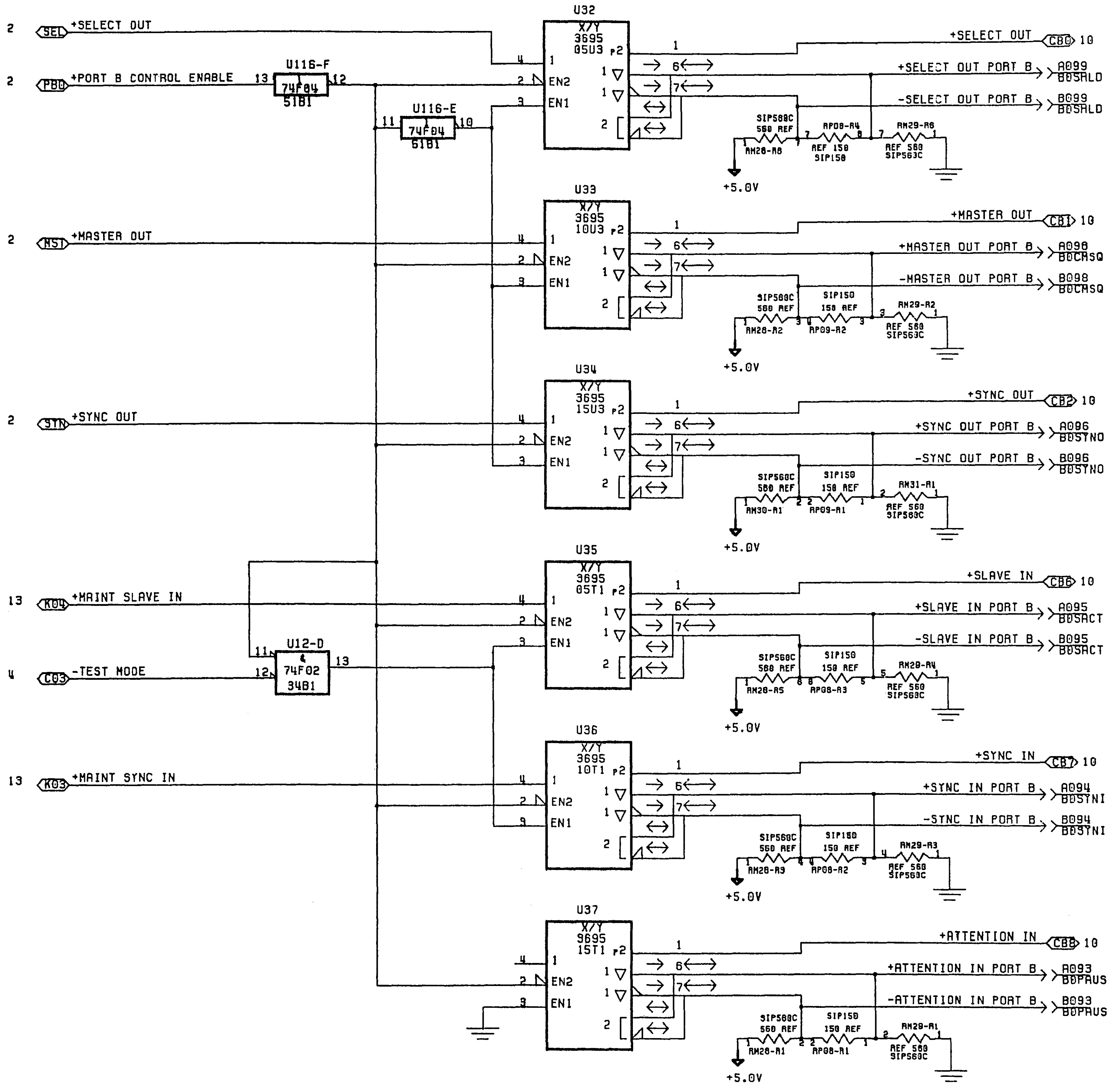
IPI PORT A BUS B TX/RX (3.2)


5 D01 +(TEST & CONTROL ENABLE)
2 PA4 +PORT A BUS B TRAN ENABLE
U22-B 74F32 34C3
21 306 -PORT A BUS B RCVR ENABLE
11 I02 BUS B OUT BIT 0-7,P
+IPI BUS B BITS 0-7,P BAB 10
U23 X/Y 3695 05H1
+PORT A BUS B PARITY A036 A0015
-PORT A BUS B PARITY B036 A0015
U24 X/Y 3695 10H1
+PORT A BUS B BIT 0 A035 A0014
-PORT A BUS B BIT 0 B035 A0014
U25 X/Y 3695 15H1
+PORT A BUS B BIT 1 A033 A0013
-PORT A BUS B BIT 1 B033 A0013
U26 X/Y 3695 20H1
+PORT A BUS B BIT 2 A032 A0012
-PORT A BUS B BIT 2 B032 A0012
U27 X/Y 3695 05F9
+PORT A BUS B BIT 3 A031 A0011
-PORT A BUS B BIT 3 B031 A0011
U28 X/Y 3695 10F9
+PORT A BUS B BIT 4 A030 A0010
-PORT A BUS B BIT 4 B030 A0010
U29 X/Y 3695 15F9
+PORT A BUS B BIT 5 A029 A0009
-PORT A BUS B BIT 5 B029 A0009
U30 X/Y 3695 20F9
+PORT A BUS B BIT 6 A028 A0008
-PORT A BUS B BIT 6 B028 A0008
U31 X/Y 3695 25F9
+PORT A BUS B BIT 7 A027 A00PU
-PORT A BUS B BIT 7 B027 A00PU
EN1
EN2
SIP560C 560 REF
SIP150 150 REF
REF 560 SIP560C
RP07-R1
RM27-R2
RM26-R2
RM27-R3
RM26-R3
RP07-R2
RM27-R5
RM26-R5
RP07-R4
RM27-R4
RM26-R4
RP07-R3
RP05-R4
RM25-R6
RM24-R6
RM25-R2
RM24-R2
RP06-R2
RM27-R1
RM26-R1
RP06-R1
RM27-R6
RM26-R6
RP06-R4
RM25-R4
RM24-R4
RP06-R3
+5.0V

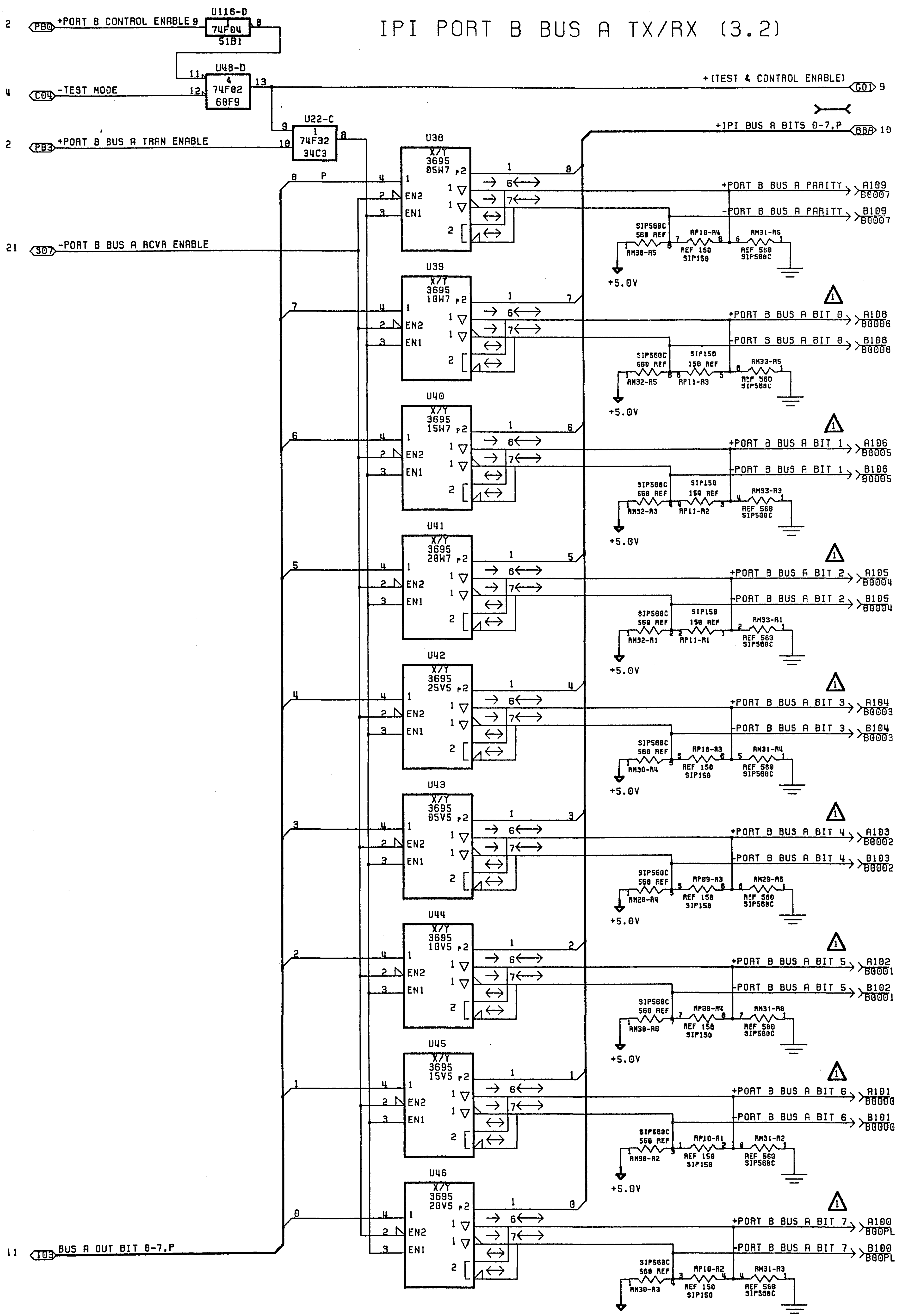
1 BIT 0 IS THE LEAST SIGNIFICANT BIT ON THE IPI CHANNEL.

CONTROL DATA	IPI TRANSMITTER BOARD PORT A BUS B R&T's TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		SHEET NO. 6	60462210	PAGE LZ-06	

IPI PORT B CONTROL TX/RX (3.2)



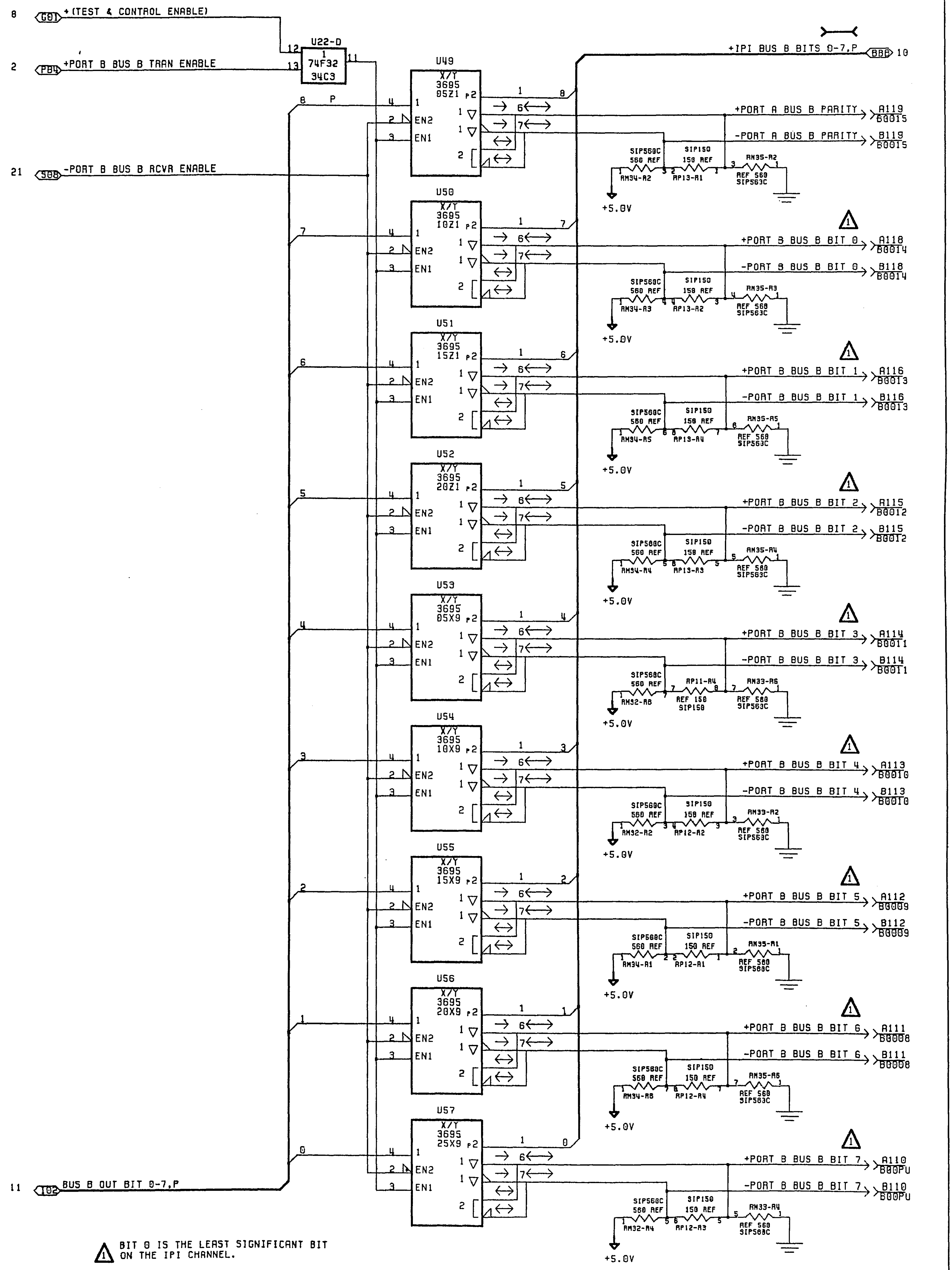
CONTROL DATA	IPI TRANSMITTER BOARD PORT B CONTROL R&T's TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		SHEET NO. 7	60462210	PAGE LZ-07	



BIT 0 IS THE LEAST SIGNIFICANT BIT ON THE IPI CHANNEL.

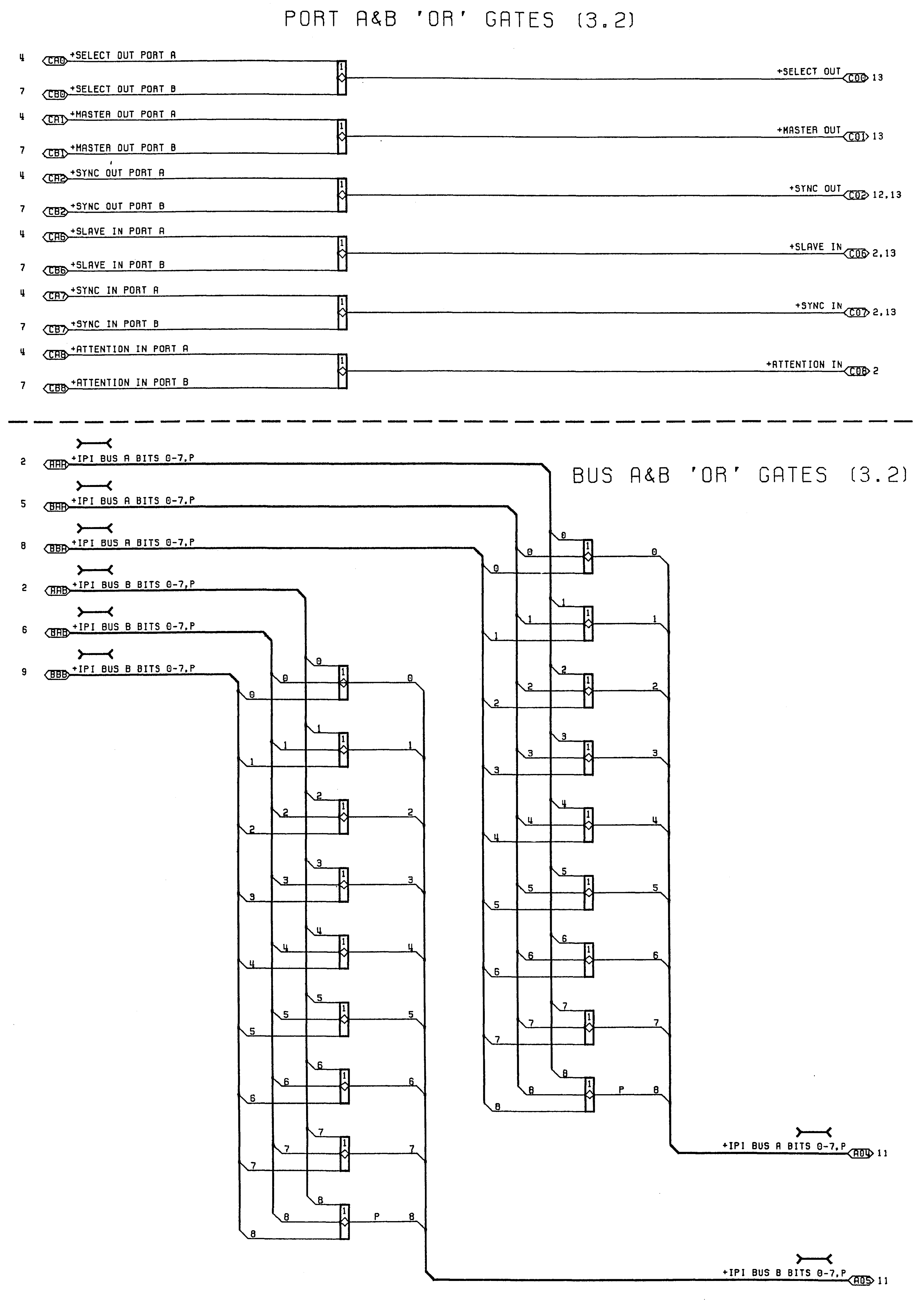
CONTROL DATA	IPI TRANSMITTER BOARD PORT B BUS A R&T's TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		SHEET NO. 8	60462218	PAGE LZ-08	

IPI PORT B BUS B TX/RX (3.2)


8 G01 +(TEST & CONTROL ENABLE)
2 PB4 +PORT B BUS B TRAN ENABLE
21 S08 -PORT B BUS B RCVR ENABLE
11 I02 BUS B OUT BIT 0-7,P
U22-D 74F32 34C3
+IPI BUS B BITS 0-7,P BBB 10
U49 X/Y 3695 05Z1
U50 X/Y 3695 10Z1
U51 X/Y 3695 15Z1
U52 X/Y 3695 20Z1
U53 X/Y 3695 05X9
U54 X/Y 3695 10X9
U55 X/Y 3695 15X9
U56 X/Y 3695 20X9
U57 X/Y 3695 25X9
EN2
EN1
+PORT A BUS B PARITY A119 B0015
-PORT A BUS B PARITY B119 B0015
+PORT B BUS B BIT 0 A118 B0014
-PORT B BUS B BIT 0 B118 B0014
+PORT B BUS B BIT 1 A116 B0013
-PORT B BUS B BIT 1 B116 B0013
+PORT B BUS B BIT 2 A115 B0012
-PORT B BUS B BIT 2 B115 B0012
+PORT B BUS B BIT 3 A114 B0011
-PORT B BUS B BIT 3 B114 B0011
+PORT B BUS B BIT 4 A113 B0010
-PORT B BUS B BIT 4 B113 B0010
+PORT B BUS B BIT 5 A112 B0009
-PORT B BUS B BIT 5 B112 B0009
+PORT B BUS B BIT 6 A111 B0008
-PORT B BUS B BIT 6 B111 B0008
+PORT B BUS B BIT 7 A110 B00PU
-PORT B BUS B BIT 7 B110 B00PU
SIP560C 560 REF
SIP150 150 REF
REF 560 SIP563C
+5.0V

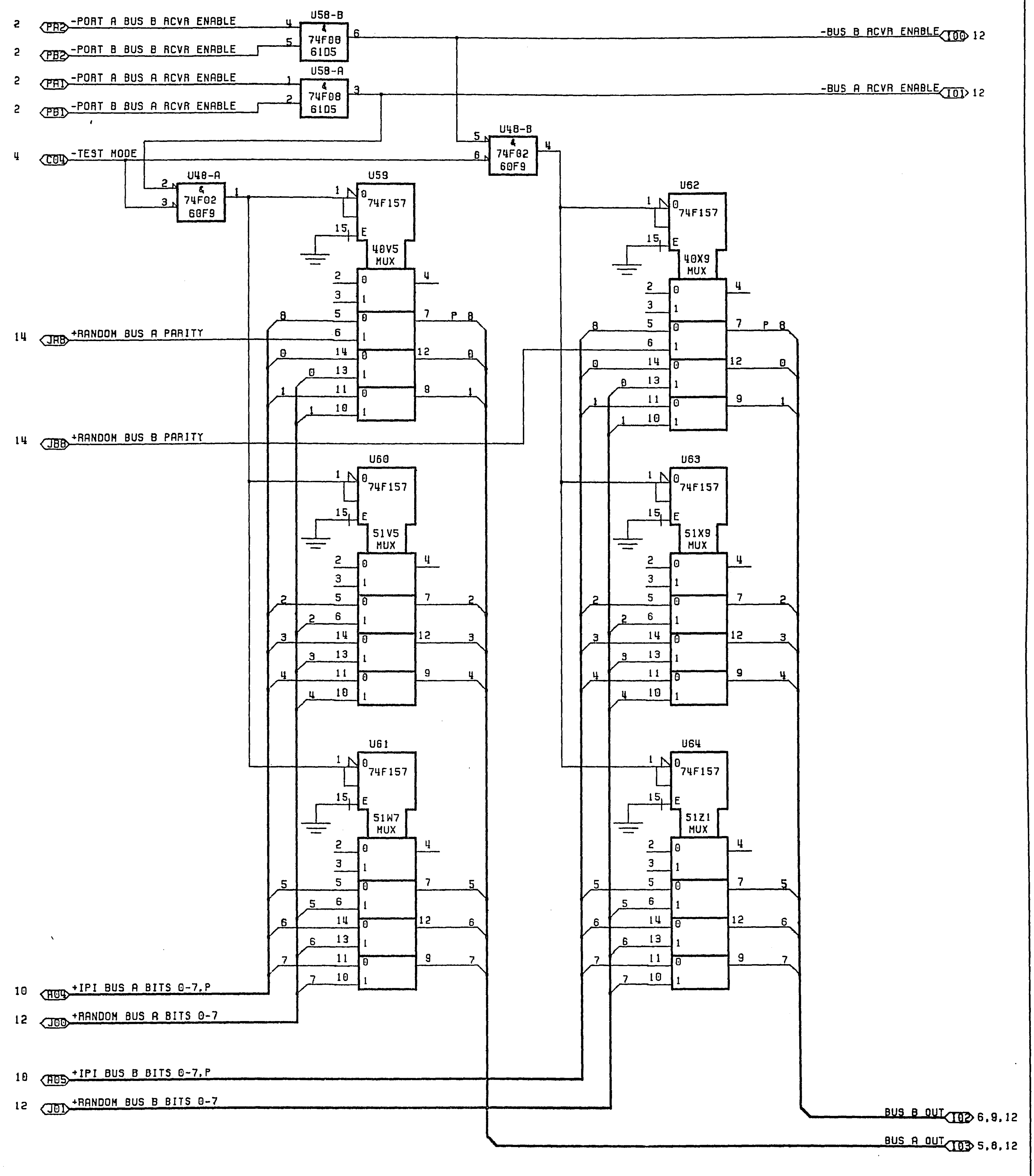
⚠ BIT 0 IS THE LEAST SIGNIFICANT BIT ON THE IPI CHANNEL.

CONTROL DATA	IPI TRANSMITTER BOARD PORT B BUS B R&T's TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
			SHEET NO. 9	60462210	PAGE LZ-09



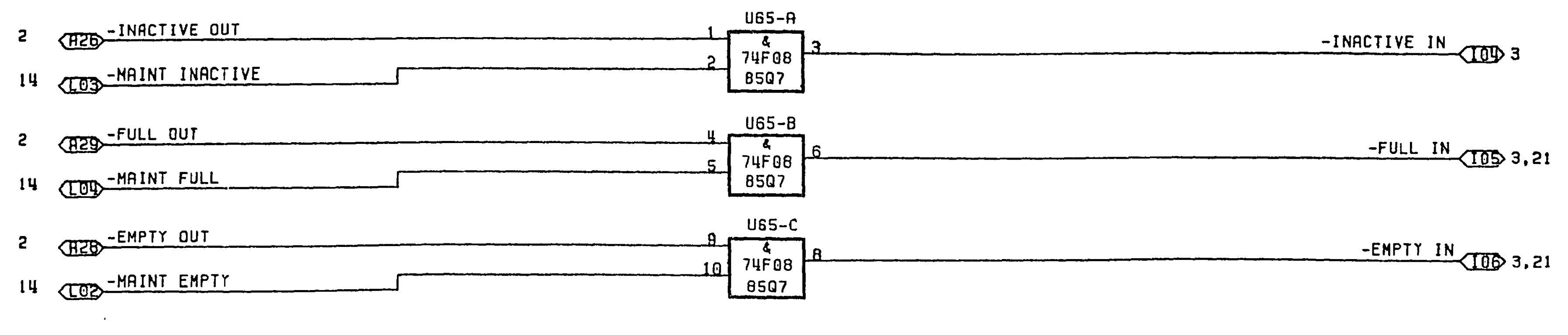
CONTROL DATA	IPI TRANSMITTER BOARD PORT A AND B CONTROL BUS A AND B R&T'S TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		SHEET NO. 10	60462210	PAGE LZ-10	

IPI DATA OUT MUX (3.3)



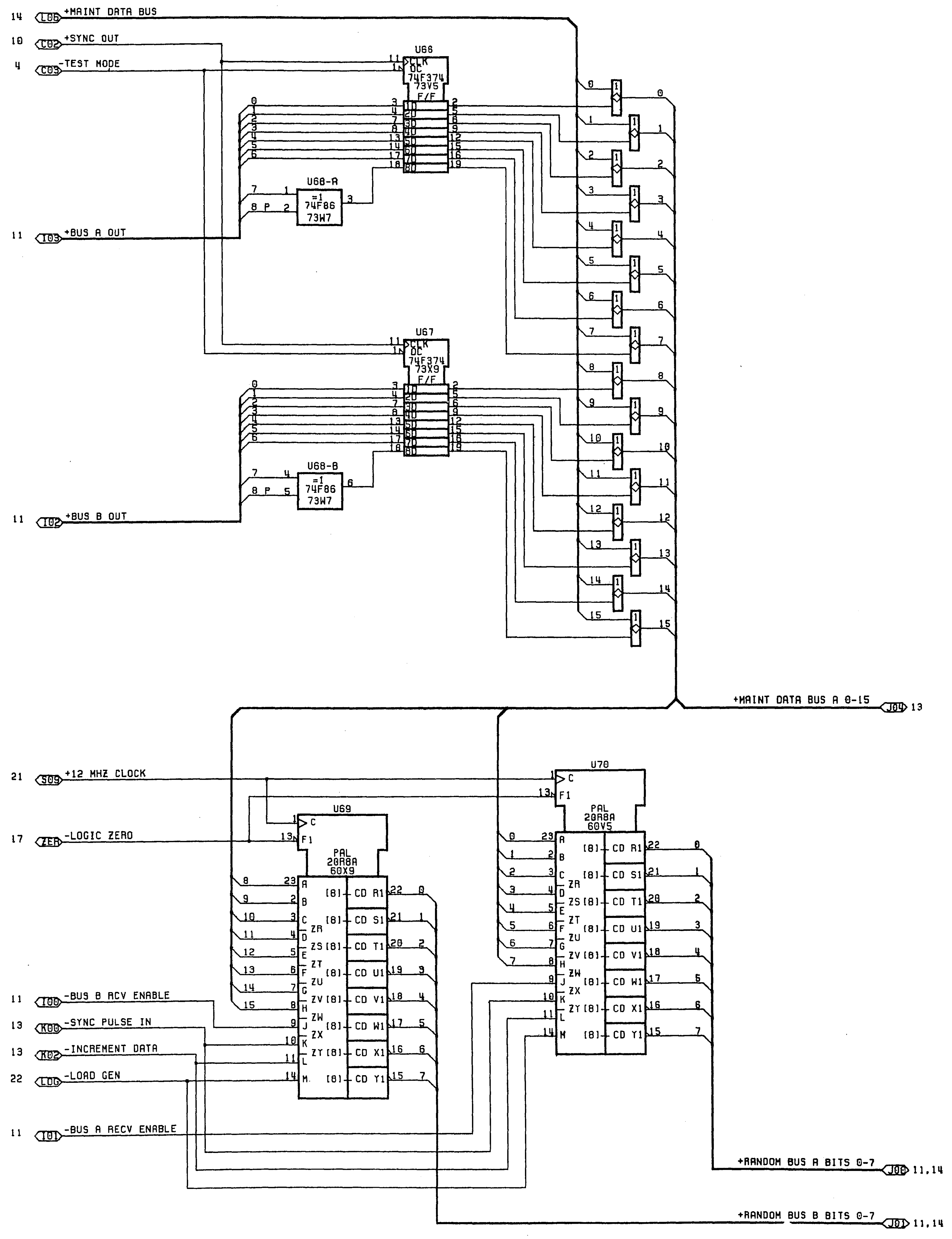
2 PA2 -PORT A BUS B RCVR ENABLE
2 PB2 -PORT B BUS B RCVR ENABLE
2 PA1 -PORT A BUS A RCVR ENABLE
2 PB1 -PORT B BUS A RCVR ENABLE
4 C04 -TEST MODE
U58-B & 74F08 61D5
U58-A & 74F08 61D5
U48-B & 74F02 60F9
U48-A & 74F02 60F9
-BUS B RCVR ENABLE I00 12
-BUS A RCVR ENABLE I01 12
U59 74F157 40V5 MUX
U60 74F157 51V5 MUX
U61 74F157 51W7 MUX
U62 74F157 40X9 MUX
U63 74F157 51X9 MUX
U64 74F157 51Z1 MUX
14 JA8 +RANDOM BUS A PARITY
14 JB8 +RANDOM BUS B PARITY
10 A04 +IPI BUS A BITS 0-7,P
12 J00 +RANDOM BUS A BITS 0-7
10 A05 +IPI BUS B BITS 0-7,P
12 J01 +RANDOM BUS B BITS 0-7
BUS B OUT I02 6,9,12
BUS A OUT I03 5,8,12

ICI-2 CONTROL (3.0)



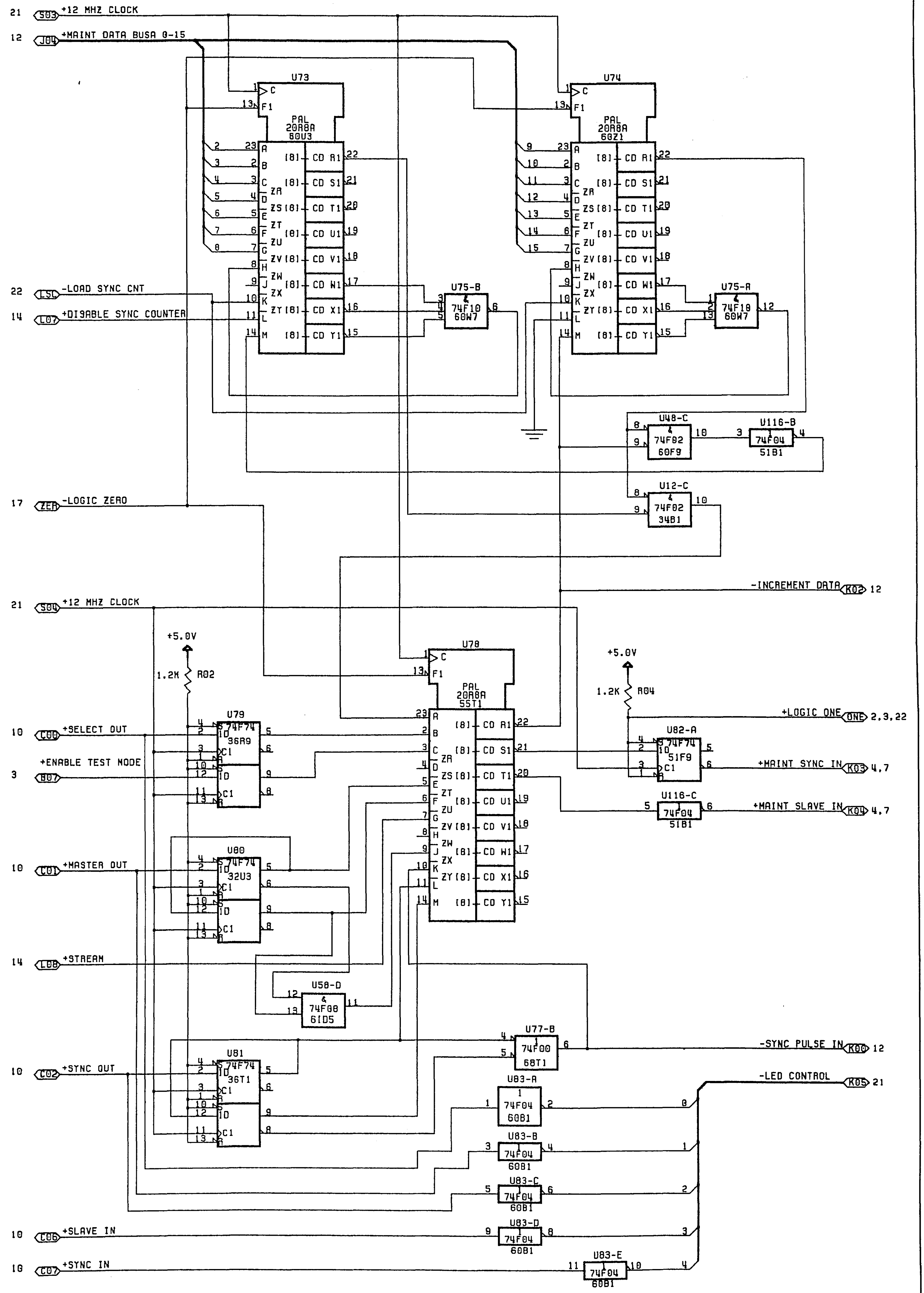
CONTROL DATA	IPI TRANSMITTER BOARD IPI DATA OUT MUX	B	DWG NO. 22132509	DATE 12/04/86	REV A
	TYPE 1LZH	N	SHEET NO. 11	60462210	PAGE LZ-11

RANDOM DATA GENERATOR-1 (3.3)



CONTROL DATA	IPI TRANSMITTER BOARD SUEDO RANDOM DATA GENERATOR TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
			SHEET NO. 12	60462210	PAGE LZ-12

MAINTENANCE TRANSFER CONTROL (3.2)



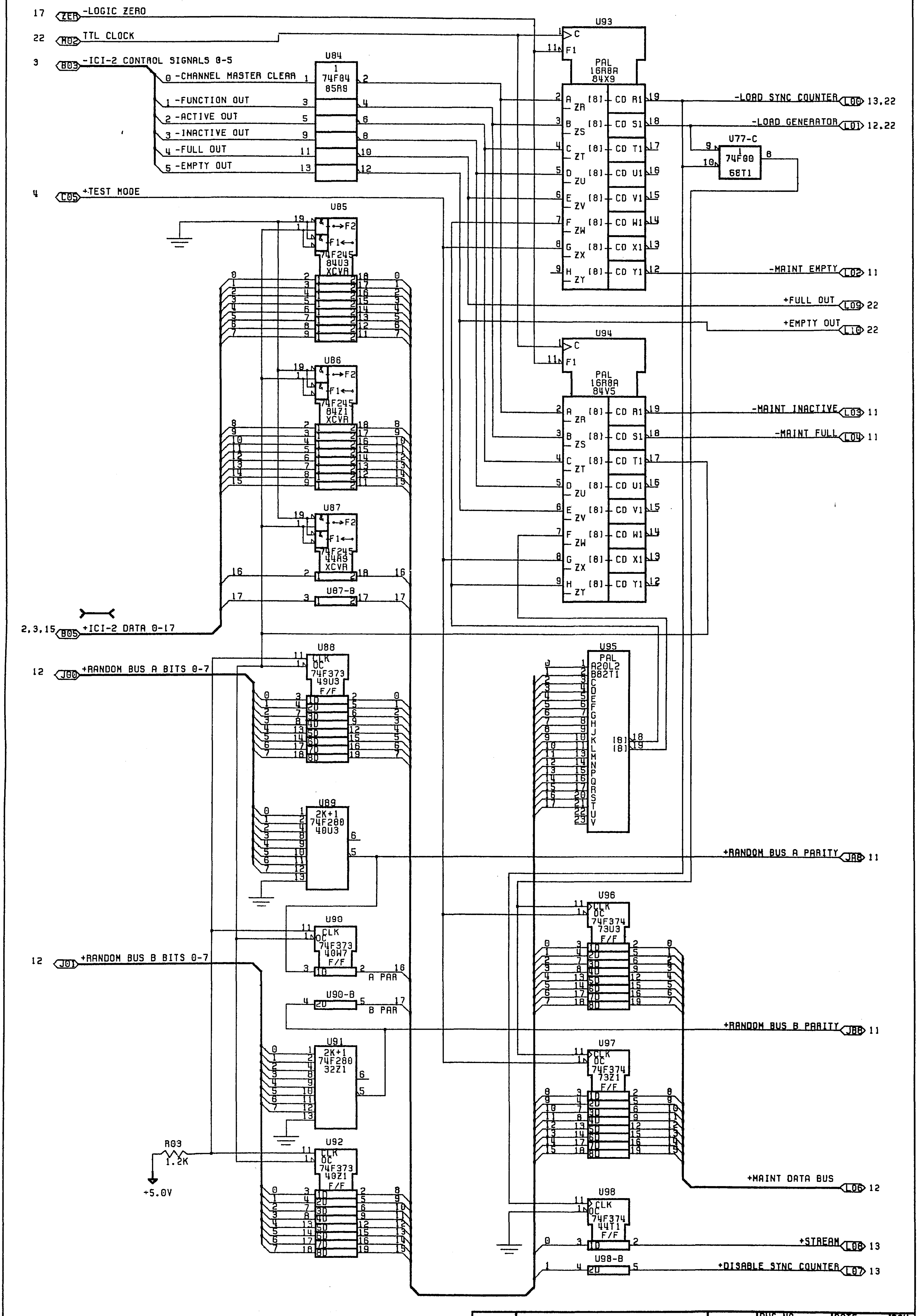
CONTROL DATA

IPI TRANSMITTER BOARD
MAINTENENCE TRANSFER CONTROL

TYPE 1LZH

B	DWG NO.	DATE	REV
	22132509	12/04/86	A
SHEET NO.	13	60462210	PAGE LZ-13

RANDOM DATA GENERATOR-2 (3.3)



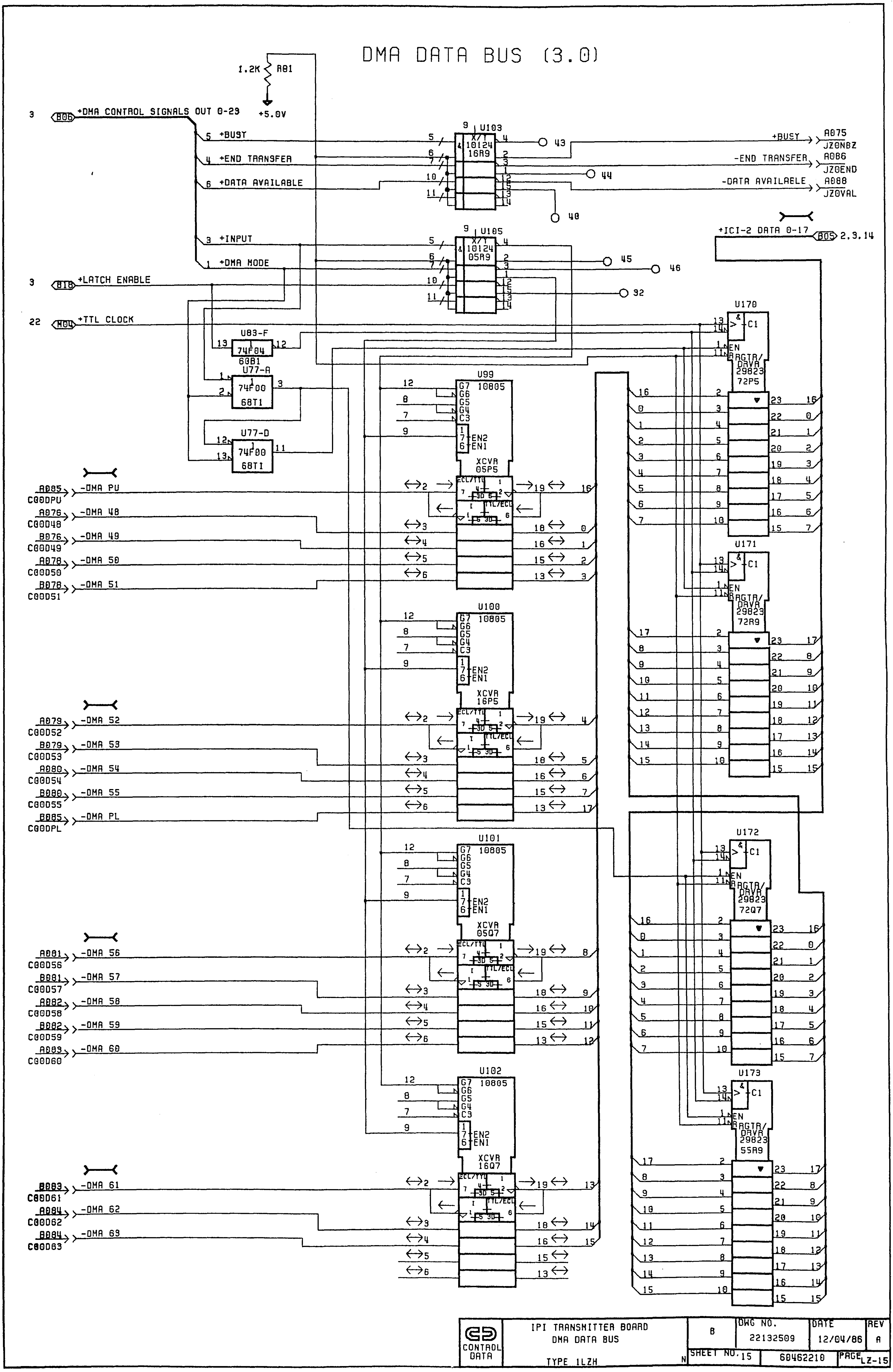
CONTROL DATA

IPI TRANSMITTER BOARD
RANDOM DATA GENERATOR

TYPE 1LZH

B	DWG NO. 22132509	DATE 12/04/86	REV A	
SHEET NO.	14	60462210	PAGE	LZ-14

DMA DATA BUS (3.0)

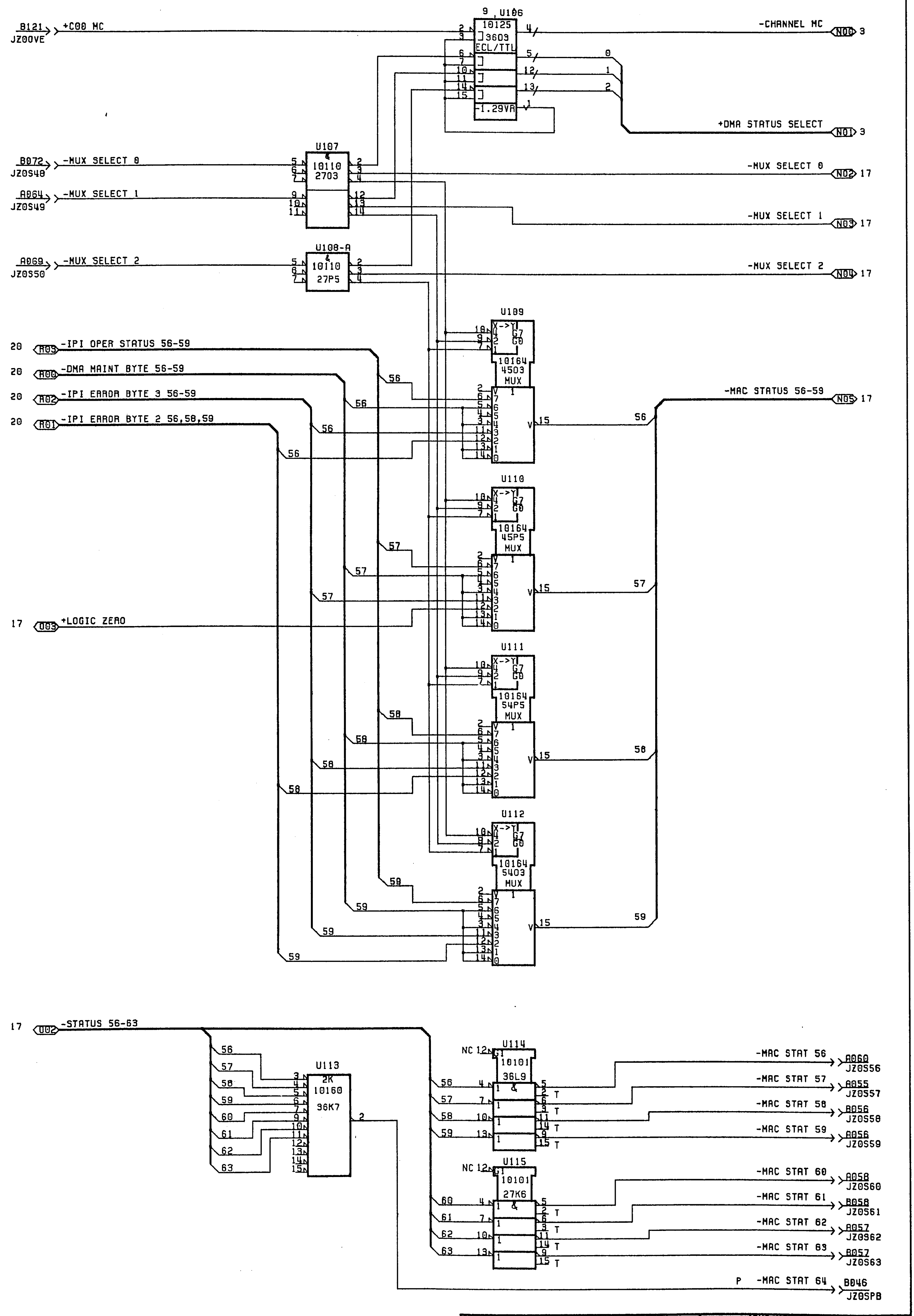


IPI TRANSMITTER BOARD
DMA DATA BUS
TYPE 1LZH

CONTROL DATA

B	DWG NO.	DATE	REV
	22132509	12/04/86	A
SHEET NO. 15	60462210	PAGE LZ-15	

MAC MUX BITS 56-59 (3.1)

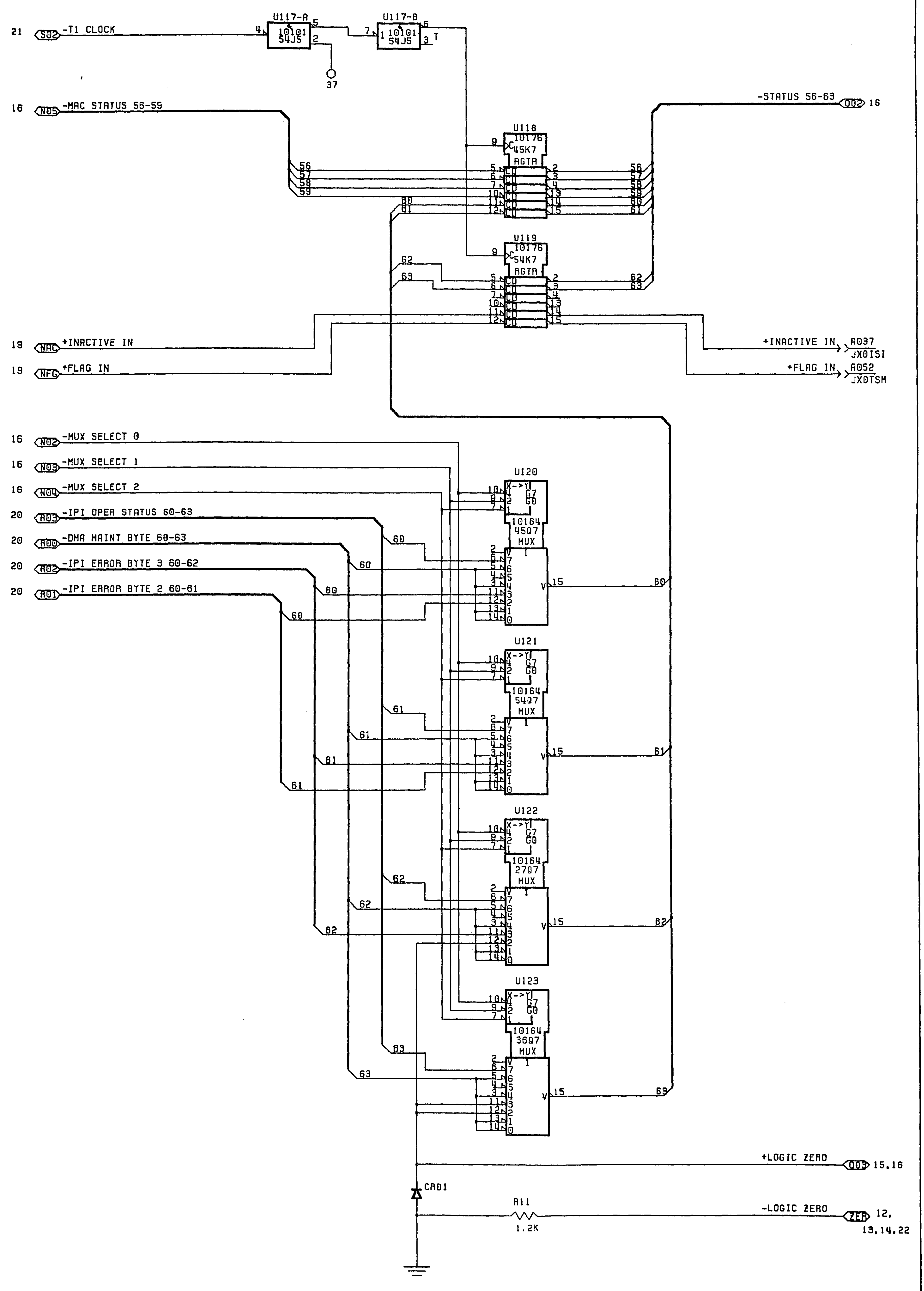


CONTROL DATA

IPI TRANSMITTER BOARD
MAC MUX
TYPE 1LZH

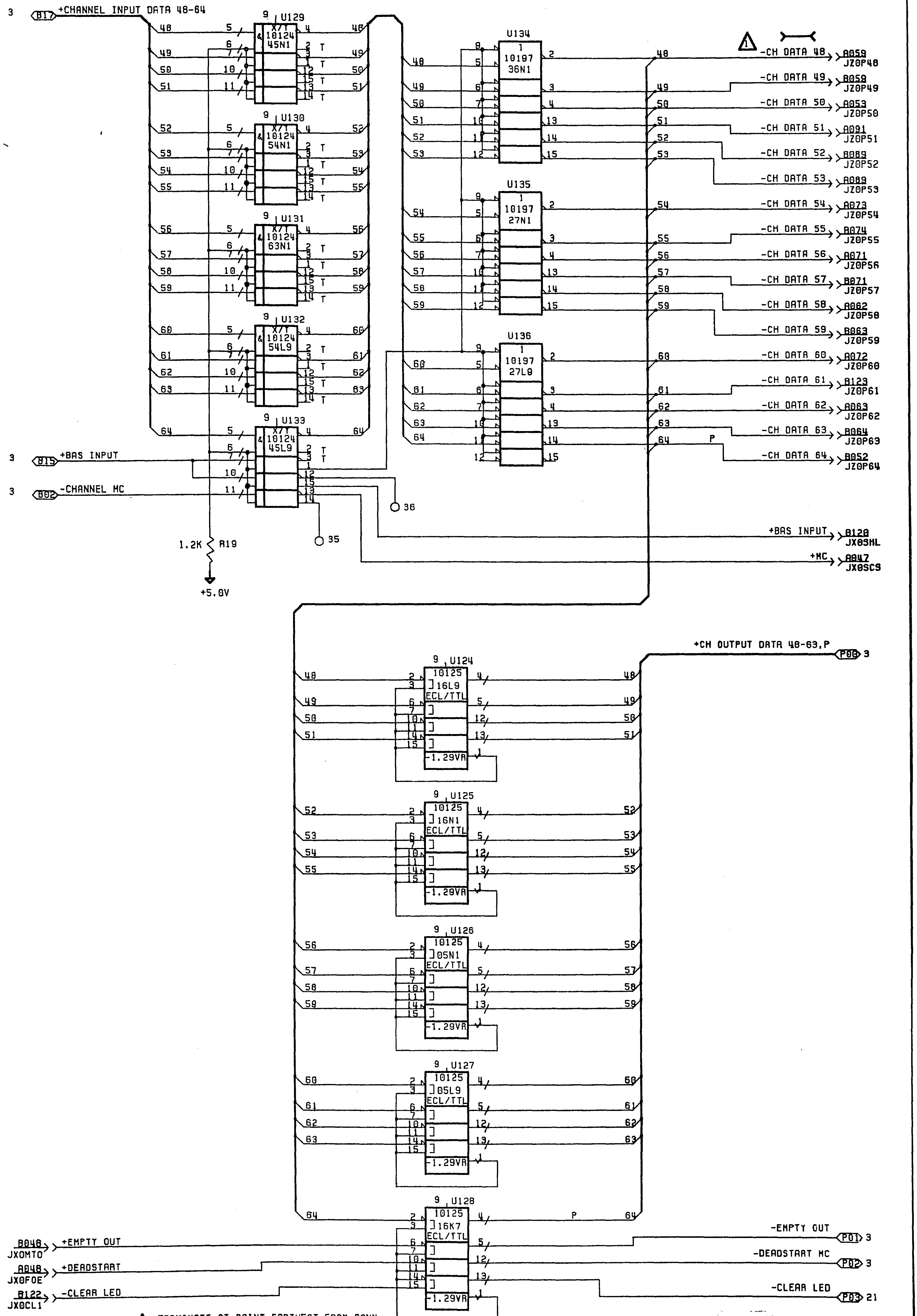
B	DWG NO. 22132509		DATE 12/04/86	REV A
	SHEET NO. 16	60462210	PAGE LZ-16	

MAC MUX BITS 60-63 (3.1)



CONTROL DATA	IPI TRANSMITTER BOARD MAC MUX	B	DWG NO. 22132509	DATE 12/04/86
				REV A
	TYPE 1LZH	N	SHEET NO. 17	60462210
				PAGE LZ-17

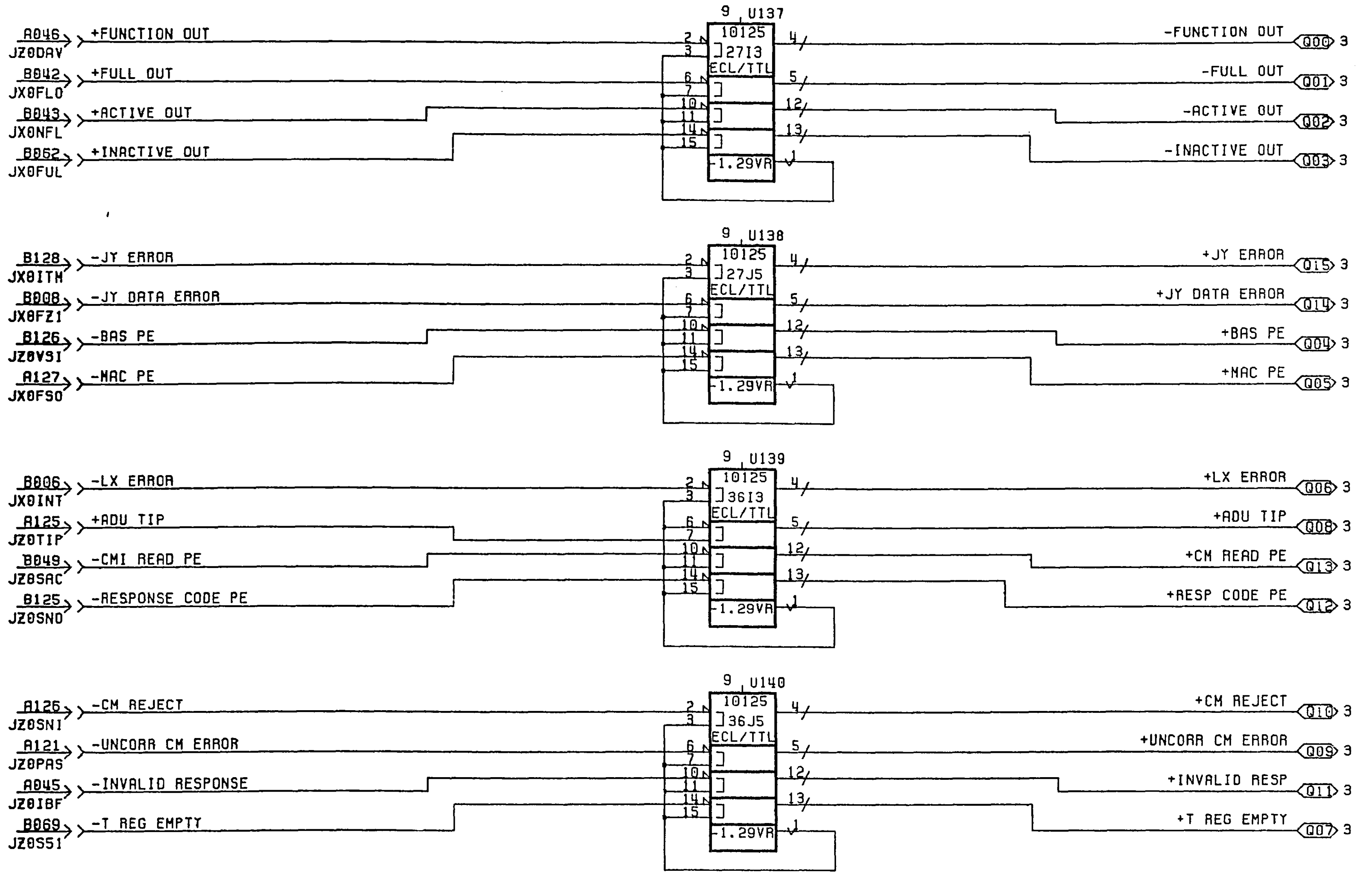
CHANNEL DATA BUS (3.0)



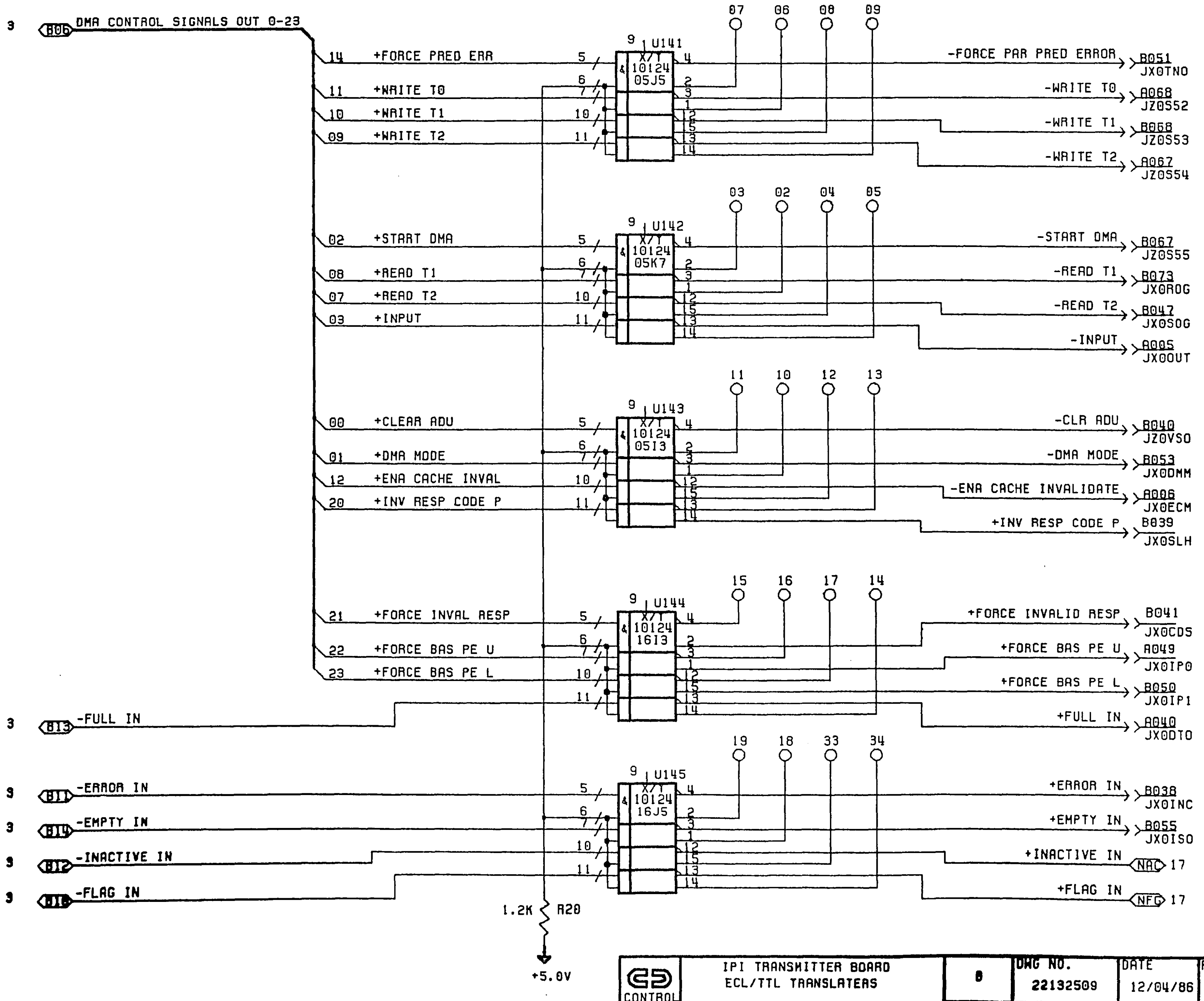
⚠1 TERMINATE AT POINT FARTHEST FROM CONN.

CONTROL DATA	IPI TRANSMITER BOARD CHANNEL DATA BUS TYPE 1LZH	B	DWG NO. 22132500	DATE 12/04/86	REV A
		SHEET NO. 18	60462210	PAGE LZ-18	

ECL/TTL TRANSLATORS (3.0)



TTL/ECL TRANSLATORS (3.0)



CONTROL DATA

IPI TRANSMITTER BOARD
ECL/TTL TRANSLATERS

TYPE 1LZH

B

DWG NO. 22132509

DATE 12/04/86

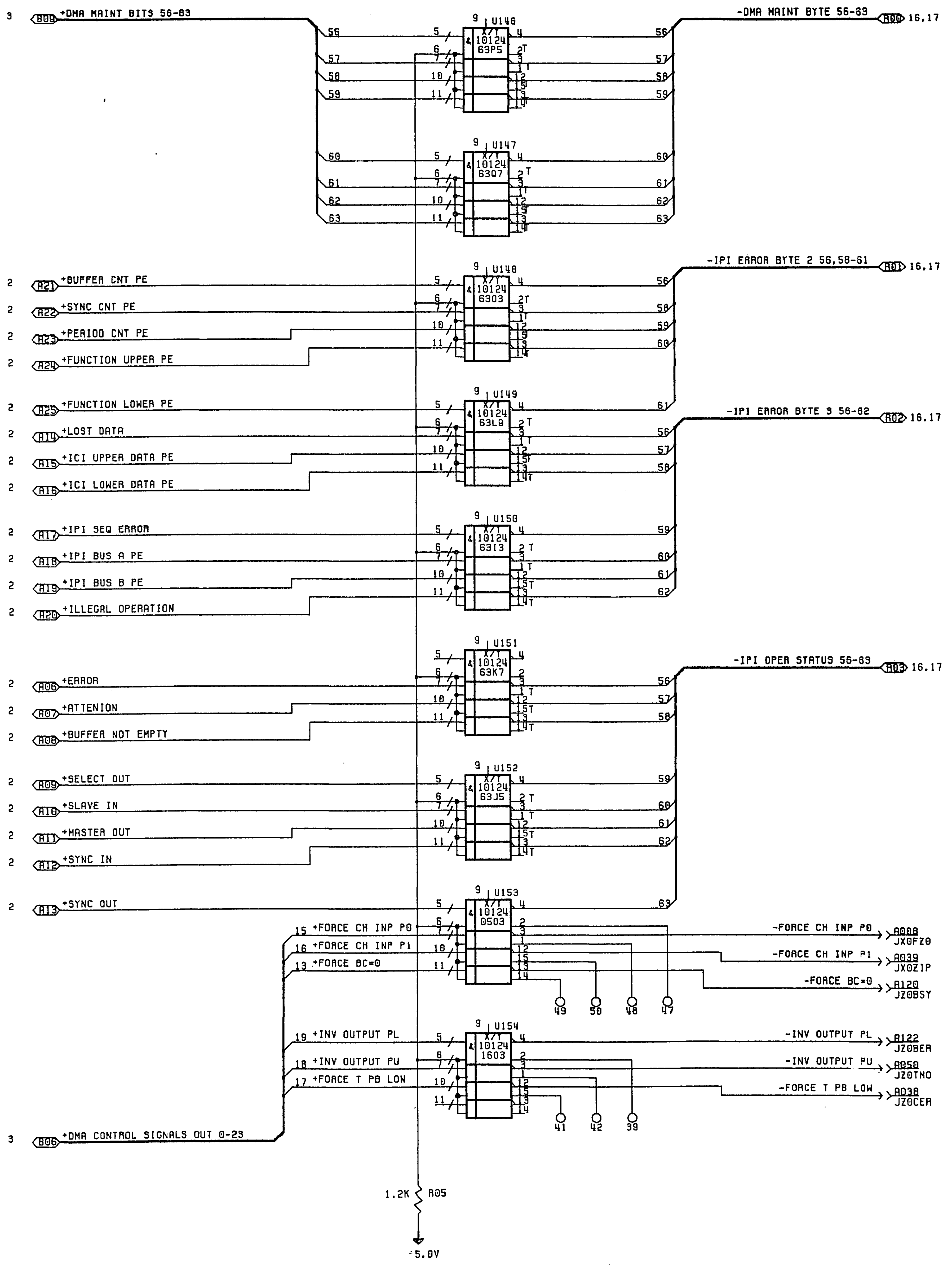
REV A

SHEET NO. 19

60462210

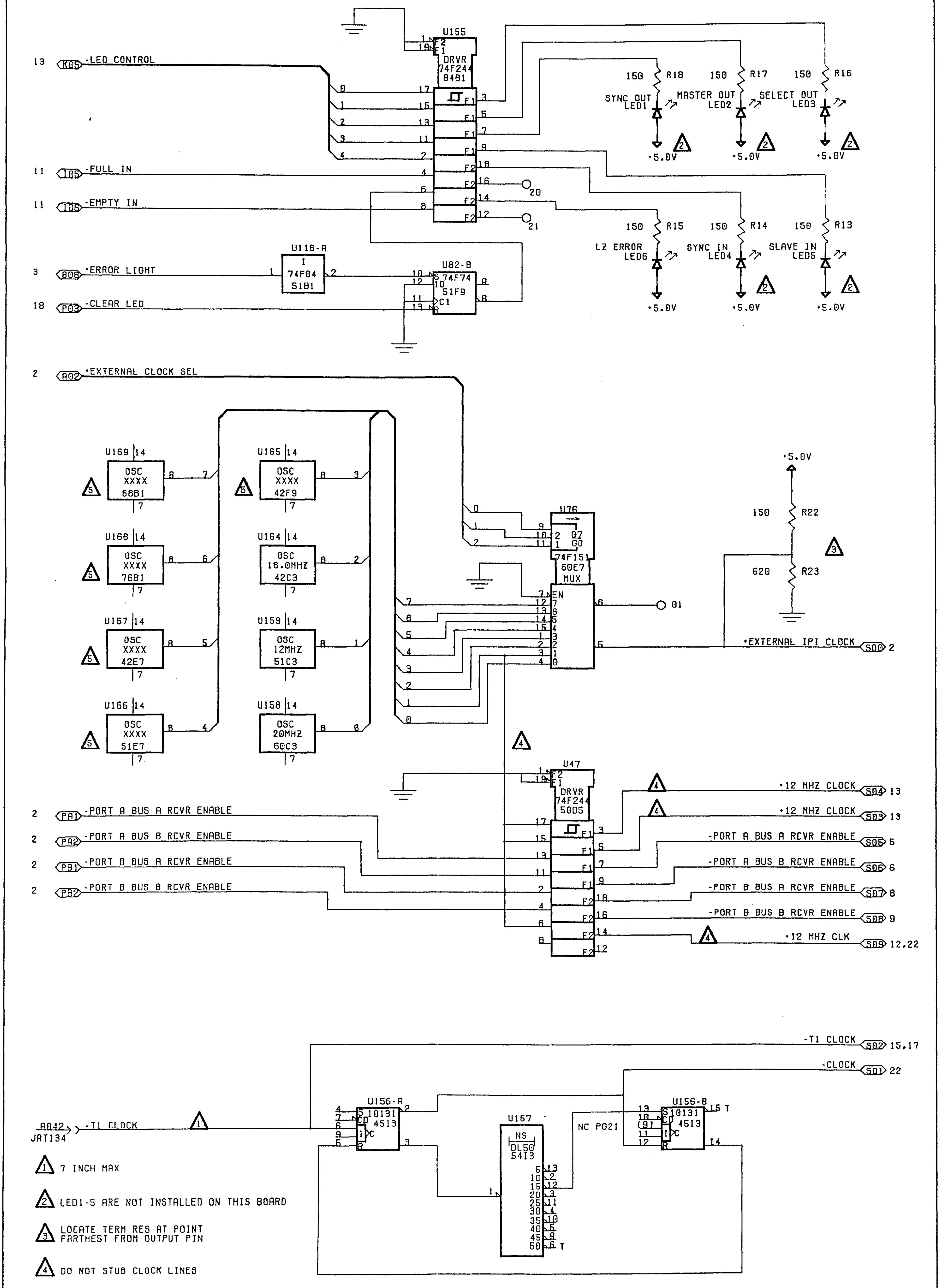
PAGE LZ-19

TTL/ECL TRANSLATORS (3.0,1)



CONTROL DATA	IPI TRANSMITTER BOARD TTL/ECL TRANSLATERS	B	DWG NO. 22132500	DATE 12/04/86	REV A
	TYPE 1LZH		SHEET NO. 20	60462210	PAGE LZ-20

LED/CLOCK/CONTROL (3.0,2)



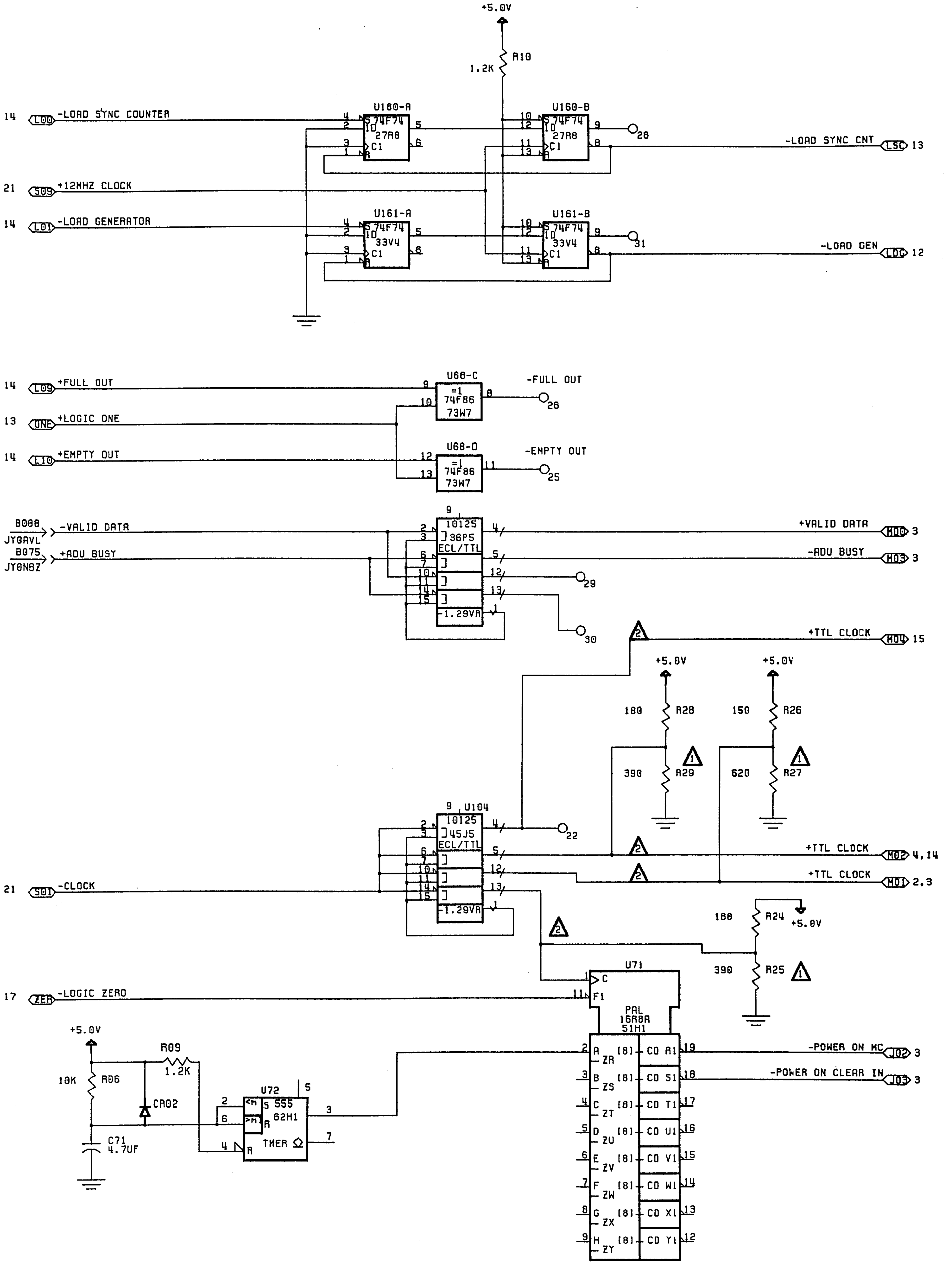
1. 7 INCH MAX
2. LED1-5 ARE NOT INSTALLED ON THIS BOARD
3. LOCATE TERM RES AT POINT FARTHEST FROM OUTPUT PIN
4. DO NOT STUB CLOCK LINES
5. OSC NOT INSTALLED ON THIS BOARD

CONTROL DATA

IPI TRANSMITTER BOARD
LED, CLOCK, AND MISC CONTROL
TYPE 1LZH

B | DWG NO. 22132509 | DATE 11/17/87 | REV B
SHEET NO. 21 | 60462210 | PAGE LZ-21

MISC CONTROL/POWER MC (3.0,2,3)



⚠1 LOCATE TERM RESISTORS AT POINT FARTHEST FROM OUTPUT PIN

⚠2 DO NOT STUB CLOCK LINES

CONTROL DATA	IPI TRANSMITTER BOARD MISC CONTROL CLOCK FANOUT AND POWER ON MC TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
		N	SHEET NO. 22	60462210	PAGE LZ-22

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	21	-EXTERNAL IPI CLOCK	27	15	-REG CLOCK
02	19	+READ T1	28	22	+LOAD SYNC COUNTER
03	19	+START DMA	29	22	+VALID DATA
04	19	+READ T2	30	22	-ADU BUSY
05	19	+INPUT	31	22	+LOAD DATA GEN
06	19	+WRITE T0	32	15	+LATCH ENABLE
07	19	+FORCE PAR PRED ERR	33	19	-INACTIVE IN
08	19	+WRITE T1	34	19	-FLAG IN
09	19	+WRITE T2	35	18	-MASTER CLEAR
10	19	+DMA MODE	36	18	-BAS INPUT
11	19	+CLEAR ADU	37	17	+T1 CLOCK
12	19	+ENABLE CACHE INVAL	38	,	,
13	19	-INV RESP CODE PAR	39	20	+INV OUTPUT PL
14	19	-FULL IN	40	15	+DATA AVAILABLE
15	19	-FORCE INVALID RESP	41	20	+FORCE T PB LOW
16	19	-FORCE BAS PE U	42	20	+INV OUTPUT PU
17	19	-FORCE BAS PE L	43	15	-BUSY
18	19	-EMPTY IN	44	15	+END TRANSFER
19	19	-ERROR IN	45	15	+INPUT
20	21	-FULL IN	46	15	+DMA MODE
21	21	-EMPTY IN	47	20	+IPI OPER STATUS 63
22	22	+TTL CLOCK	48	20	+FORCE CH INP P0
23	,	,	49	20	+FORCE BC=0
24	,	,	50	20	+FORCE CH INP P1
25	22	-EMPTY OUT	51	,	,
26	22	-FULL OUT			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117,A037,A038,B037,B038,B128
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070
TERM	NONE
UNUSED	A003,B003,A004,B004,B005,A009,B009,B037,A041,A043,B045,A051,B060,A061,B061,A070,B070,A074,B086,A090,B090,B091,A092,B092,A123,B127,A128

CONTROL DATA	IPI TRANSMITTER BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1LZH	B	DWG NO. 22132509	DATE 12/04/86	REV A
	N	SHEET NO. 23	60462210	PAGE LZ-23	

PANEL A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1JAH	1JHH	1JHH	1JHH	1JHH	1JJH	1JJH	1JGH	1JUH △1	1JUH	1JCH	1JVH △1	1JVH	1JEH	1JDH	1JFH △1	1JFH	1JFH		1JSH	1JTH	1JQH	1JRH OR IHRH △2					
CLK	CMI							ADU											NIO MRA	NIO MRB	MAC	RI 1-3					
	DATA				ADRS			CM ADRS			ADU WRITE				ADU READ												
	BITS 0-15	BITS 16-31	BITS 32-47	BITS 48-63	CHAN 5-11	CHAN 0-4	CONT	BASC 0,1	BAS 2,3	BAS 0,1	BASC 0,1	BAS 2,3	BAS 0,1	CONT	BASC 0,1	BAS 2,3	BAS 0,1										

PANEL B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1JMH	1JLH	1JLH	1JLH	1JLH	1JLH	1JLH	1JWH	1KRH	1JWH	1KRH	1JWH	1KRH	1JWH	1KRH	1JLH	1JLH	1JLH	1JLH	1JLH	1JLH	1CQO	1JKH		1KBH	1KBH	1KBH	1KBH
UTILITY CHAN 14,15,17	NIO CHAN 20-33						NIO BAS 0-3								NIO CHAN 0-13						DISPLAY CONT	TPM		NIO PPM 0-3			
	32,33	30,31	26,27	24,25	22,23	20,21	3	3	2	2	1	1	0	0	12,13	10,11	6,7	4,5	2,3	0,1				3	2	1	0

NOTES:

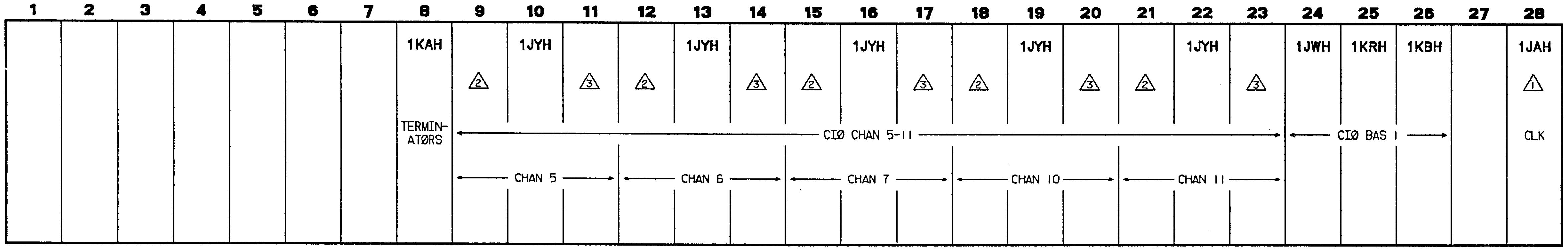
△1 THESE IJFH, IJUH, AND IJVH BOARDS ARE PART OF FIRST CONCURRENT PP INCREMENT (PANEL D).

△2 IJRH IS AT THIS LOCATION IF AT478-A OR AT510-A IS INSTALLED. IHRH IS AT THIS LOCATION IF AT509-A IS INSTALLED.

CONTROL DATA
DEVELOPMENT DIVISION
PANEL A AND B MAPS
NIO CABINET
CODE IDENT
DWG NO 60462210
REV P
SHEET NIO CABINET
PAGE

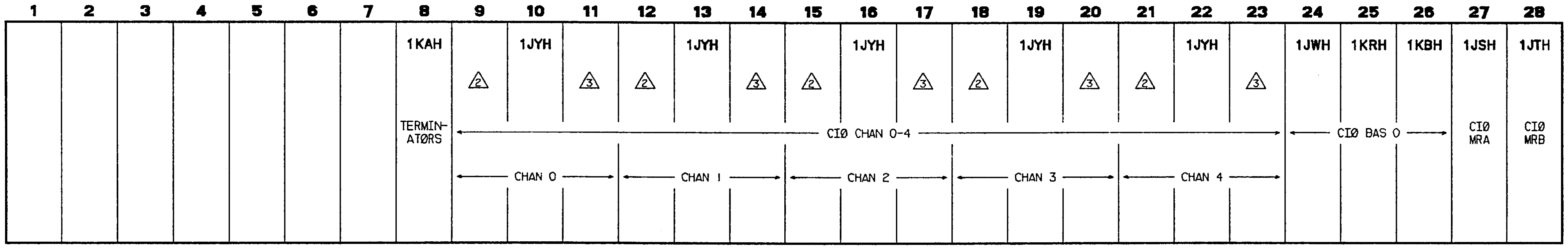
SECOND CONCURRENT PP INCREMENT

PANEL C



FIRST CONCURRENT PP INCREMENT

PANEL D



NOTES:

1. 1JAH BOARD IS PART OF FIRST CONCURRENT PP INCREMENT (PANEL D).
2. DMA CHANNEL ADAPTER BOARD TYPES:
   ISI = 1JZH
   170 = 1KZH
   IPI = 1LZH
3. DMA CHANNEL ADAPTER BOARD TYPES:
   ISI = 1JXH
   170 = 1KXH
   IPI = 1LXH

CONTROL DATA	PANEL C AND D MAPS CIO CABINET	CODE IDENT	DWG NO 60462210	REV P
DEVELOPMENT DIVISION		SHEET CIO CABINET	PAGE	

Comments (continued from other side)

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COMMENT SHEET

MANUAL TITLE: AT478-A/B, AT481-A/B IOU and Associated Equipment Hardware Maintenance Manual, Volume 2, Book 3 of 3

PUBLICATION NO.: 60462210 **REVISION:** P

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